FET DATABOOK

NATIONAL SEMICONDUCTOR

FET
DATABOOK

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Section 1

Introduction

1

Introduction

This is National Semiconductor's first Field Effect Transistor/Analog Switches Data Book. It is the direct result of the designer's desire to have a complete, concise, up to date handbook for discrete FETs and FET analog switches.

There are over 1000 Junction FETs and analog switches available from at least 8 major suppliers and many smaller ones. In order to ease the designer's task, National has selected approximately 350 types as representative of a product that reflects the best available current technology. Certain of these products have been designated preferred parts. To qualify as a preferred part, a product must offer the latest technology, the best performance, excellent deliverability and competitive prices. These preferred parts should be considered first in all applications.

If you are a first-time user of FETs and FET analog switches, you will find this catalog invaluable in making your selection. Old hands will appreciate the concise selector guides and accurate process curves. Whatever your experience, you will find National's Sales Representatives, Field Application Engineers and Factory Personnel willing and able to help with any application problems or questions.

Product Profile

Field Effect Transistors. National offers 17 JFET processes which cover the full range of possible products. Devices with leakage currents as low as 0.1 pA are available along with devices suitable for operation at VHF frequencies. Low noise FETs for audio and subaudio applications are available along with the industry's broadest line of monolithic dual FETs. National invented the monolithic dual JFET and consistently wins praise for consistent performance to the tightest offset and drift specifications. National's cascode dual JFETs (Process 84, 94) offer superior CMRR and low leakage currents even at extended voltages.

Analog Switches. National Semiconductor has for many years supplied a full line of analog switches which served the designer's needs for high quality, competitively priced products. Recognizing the need for improved reliability and lower cost as industry usage increased, National developed the BI-FET™ technology and other monolithic FET structures which have become the industry standard for analog switches. The preferred parts shown in this data book utilize these processes. Most are function, pin and specification compatible with earlier products available in the market place.

High Reliability Product. National Semiconductor is committed to supplying the military/aerospace markets with the highest quality product available. Presently, National is qualified to supply 85% of all FETs on the MIL-S-19500 QPL—more than any other supplier. Our capability covers a wide range of standard and special testing and processing to levels as specified in MIL-S-19500, MIL-STD-750, MIL-STD-883, MIL-M-38510. Contact your local representative or regional office for information concerning your specific requirements.

How to Use This Catalog

The Field Effect Transistor/Analog Switch Data Book is divided into 7 sections. The following information is contained in each.

Section 1	Alpha-numeric parts lists and cross reference guides
Section 2	FET selector guides including a complete guide by application to all part types offered by National. This is the complete guide to National FET specifications and is indexed in Section 1. Preferred parts are shown with gray overprinting.
Section 3	FET process characteristics giving complete information on all processes, including all parts manufactured from a particular process by package type.
Section 4	FET preferred parts data sheets.
Section 5	Analog switch selector guides and data sheets.
Section 6	Applications notes on FETs and analog switches.
Section 7	Physical Dimensions

The following suggested procedure will help you find the device you need.

Part Number Known: Go to section 1. If alternate type found in cross reference guide, then compare alternate specification in section 2 against desired part type for compatibility.

Specification Known: Refer to "FET Process Comparison Chart" in section 2 to find the most compatible process. Then turn to the specific process in section 3 for a listing of specific device type numbers available in that process. Take special note of preferred part types. Full data sheets are available in section 4.

Application Known: For FETs, turn to "Choose the Proper FET" and "FET Application Guide" in section 2. Refer also to "Important Parameters by Application" as needed. Once a process is selected, refer to section 3 and to the proper preferred part type. For analog switches, refer to section 5 "Analog Switch Selector Guide".

None of the Above: Contact local representative or regional office for assistance.

FET Parts List

DEVICE	PROCESS/PACKAGE	SELECTION GUIDE	PREFERRED PARTS DATA SHEET	PROCESS PAGE
• 2N2608	89/11	2-19		3-23
2N2609	88/11	2-19		3-21
2N3069	52/02	2-13		3-8
2N3070	52/02	2-13		3-8
2N3329	89/23	2-19		3-23
2N3330	89/23	2-19		3-23
2N3331	89/23	2-19		3-23
2N3332	89/23	2-19		3-23
2N3368	52/02	2-13		3-8
2N3369	52/02	2-13		3-8
2N3370	52/02	2-13		3-8
2N3382	88/23	2-19		3-21
2N3384	88/23	2-19		3-21
2N3386	88/23	2-19		3-21
2N3436	55/02	2-13		3-12
2N3437	55/02	2-13		3-12
2N3438	55/02	2-13		3-12
2N3458	52/02	2-13		3-8
2N3459	52/02	2-13		3-8
2N3460	52/02	2-13		3-8
2N3684	52/25	2-13	4-3	3-8
2N3685	52/25	2-13	4-3	3-8
2N3686	52/25	2-13	4-3	3-8
2N3687	52/25	2-13	4-3	3-8
2N3819	50/74	2-11		3-3
2N3821	55/25	2-13		3-12
2N3822	55/25	2-13		3-12
• 2N3823	50/25	2-11		3-3
2N3824	55/25	2-9		3-12
2N3921	83/12	2-15		3-16
2N3922	83/12	2-15		3-16
2N3954	83/12	2-15	4-4	3-16
2N3954A	83/12	2-15	4-4	3-16
2N3955	83/12	2-15	4-4	3-16
2N3955A	83/12	2-15	4-4	3-16
2N3956	83/12	2-15	4-5	3-16
2N3957	83/12	2-15	4-5	3-16
2N3958	83/12	2-15	4-5	3-16
2N3966	50/25	2-9		3-3
2N3967	52/25	2-13		3-8
2N3967A	52/25	2-13		3-8
2N3968	52/25	2-13		3-8
2N3968A	52/25	2-13		3-8
2N3969	52/25	2-13		3-8
2N3969A	52/25	2-13		3-8
2N3970	51/02	2-9		3-6
2N3971	51/02	2-9		3-6
2N3972	51/02	2-9		3-6

• Denotes JAN qualified type

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DEVICE	PROCESS/PACKAGE	SELECTION GUIDE	PREFERRED PARTS DATA SHEET	PROCESS PAGE
2N3993	88/23	2-19		3-21
2N3993A	88/23	2-19		3-21
2N3994	88/23	2-19		3-21
2N3994A	88/23	2-19		3-21
2N4084	83/12	2-15		3-16
2N4085	83/12	2-15		3-16
• 2N4091	51/02	2-9	4-6	3-6
• 2N4092	51/02	2-9	4-6	3-6
• 2N4093	51/02	2-9	4-6	3-6
2N4117	53/25	2-13		3-10
2N4117A	53/25	2-13	4-7	3-10
2N4118	53/25	2-13		3-10
2N4118A	53/25	2-13	4-7	3-10
2N4119	53/25	2-13		3-10
2N4119A	53/25	2-13	4-7	3-10
2N4220	55/25	2-14		3-12
2N4220A	55/25	2-14		3-12
2N4221	55/25	2-14		3-12
2N4221A	55/25	2-14		3-12
2N4222	55/25	2-14		3-12
2N4222A	55/25	2-14		3-12
2N4223	50/25	2-11		3-3
2N4224	50/25	2-11		3-3
2N4338	52/02	2-14	4-8	3-8
2N4339	52/02	2-14	4-8	3-8
2N4340	52/02	2-14	4-8	3-8
2N4341	52/02	2-14	4-8	3-8
2N4381	89/11	2-19		3-23
2N4382	88/11	2-19		3-21
2N4391	51/02	2-9	4-9	3-6
2N4392	51/02	2-9	4-9	3-6
2N4393	51/02	2-9	4-9	3-6
2N4416	50/25	2-11	4-10	3-3
• 2N4416A	50/25	2-11	4-10	3-3
• 2N4856	51/02	2-9	4-11	3-6
2N4856A	51/02	2-9		3-6
• 2N4857	51/02	2-9	4-11	3-6
2N4857A	51/02	2-9		3-6
• 2N4858	51/02	2-9	4-11	3-6
2N4858A	51/02	2-9		3-6
• 2N4859	51/02	2-9		3-6
2N4859A	51/02	2-9		3-6
• 2N4860	51/02	2-9		3-6
2N4860A	51/02	2-9		3-6
• 2N4861	51/02	2-9		3-6
2N4861A	51/02	2-9		3-6
2N5018	88/11	2-19		3-21
2N5019	88/11	2-19		3-21

• Denotes JAN qualified type

FET Parts List (Continued)

DEVICE	PROCESS/PACKAGE	SELECTION GUIDE	PREFERRED PARTS DATA SHEET	PROCESS PAGE
2N5020	89/11	2-20		3-23
2N5021	89/11	2-20		3-23
2N5045	83/12	2-16		3-16
2N5046	83/12	2-16		3-16
2N5047	83/12	2-16		3-16
2N5078	50/25	2-11		3-3
2N5103	50/25	2-14		3-3
2N5104	50/25	2-14		3-3
2N5105	50/25	2-14		3-3
• 2N5114	88/11	2-19	4-12	3-21
• 2N5115	88/11	2-19	4-12	3-21
• 2N5116	88/11	2-19	4-12	3-21
2N5196	83/12	2-16	4-13	3-16
2N5197	83/12	2-16	4-13	3-16
2N5198	83/12	2-16	4-13	3-16
2N5199	83/12	2-16	4-13	3-16
2N5245	90/77	2-11	4-14	3-25
2N5246	90/77	2-11	4-14	3-25
2N5247	90/77	2-11	4-14	3-25
2N5248	50/74	2-11		3-3
2N5358	55/25	2-14	4-15	3-12
2N5359	55/25	2-14	4-15	3-12
2N5360	55/25	2-14	4-15	3-12
2N5361	55/25	2-14	4-16	3-12
2N5362	55/25	2-14	4-16	3-12
2N5363	55/25	2-14	4-16	3-12
2N5364	55/25	2-14	4-16	3-12
2N5397	90/25	2-11	4-17	3-25
2N5398	90/25	2-11		3-25
2N5432	58/07	2-9	4-18	3-14
2N5433	58/07	2-9	4-18	3-14
2N5434	58/07	2-9	4-18	3-14
2N5452	83/12	2-16		3-16
2N5453	83/12	2-16		3-16
2N5454	83/12	2-16		3-16
2N5457	55/72	2-14	4-19	3-12
2N5458	55/72	2-14	4-19	3-12
2N5459	55/72	2-14	4-19	3-12
2N5460	89/71	2-20	4-20	3-23
2N5461	89/71	2-20	4-20	3-23
2N5462	89/71	2-20	4-20	3-23
2N5484	50/72	2-11	4-21	3-3
2N5485	50/72	2-11	4-21	3-3
2N5486	50/72	2-11	4-21	3-3
2N5515	95/12	2-17		3-33
2N5516	95/12	2-17		3-33
2N5517	95/12	2-17		3-33
2N5518	95/12	2-17		3-33

• Denotes JAN qualified type

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DEVICE	PROCESS/PACKAGE	SELECTION GUIDE	PREFERRED PARTS DATA SHEET	PROCESS PAGE
2N5519	95/12	2-17		3-33
2N5520	95/12	2-17	4-22	3-33
2N5521	95/12	2-17	4-22	3-33
2N5522	95/12	2-17	4-22	3-33
2N5523	95/12	2-17	4-22	3-33
2N5524	95/12	2-17	4-22	3-33
2N5545	*83/12	2-16	4-23	3-16
2N5546	*83/12	2-16	4-23	3-16
2N5547	*83/12	2-16	4-23	3-16
2N5555	50/72	2-9		3-3
2N5556	50/25	2-14		3-3
2N5557	50/25	2-14		3-3
2N5558	50/25	2-14		3-3
2N5561	†98/12	2-16		3-37
2N5562	†98/12	2-16		3-37
2N5563	†98/12	2-16		3-37
2N5564	96/12	2-17	4-24	3-35
2N5565	96/12	2-17	4-24	3-35
2N5566	96/12	2-17	4-24	3-35
2N5638	51/72	2-10	4-25	3-6
2N5639	51/72	2-10	4-25	3-6
2N5640	51/72	2-10	4-25	3-6
2N5653	51/72	2-10		3-6
2N5654	51/72	2-10		3-6
2N5668	50/72	2-11		3-3
2N5659	50/72	2-11		3-3
2N5670	50/72	2-11		3-3
2N5902	84/24	2-18		3-18
2N5903	84/24	2-18		3-18
2N5904	84/24	2-18		3-18
2N5905	84/24	2-18		3-18
2N5906	84/24	2-18	4-26	3-18
2N5907	84/24	2-18	4-26	3-18
2N5908	84/24	2-18	4-26	3-18
2N5909	84/24	2-18	4-26	3-18
2N5911	93/24	2-17	4-27	3-29
2N5912	93/24	2-17	4-27	3-29
2N5949	50/77	2-11		3-3
2N5950	50/77	2-11		3-3
2N5951	50/77	2-11		3-3
2N5952	50/77	2-11		3-3
2N5953	50/77	2-11		3-3
2N6483	95/12	2-17	4-29	3-33
2N6484	95/12	2-17	4-29	3-33
2N6485	95/12	2-17	4-29	3-33
BC264A	50/77	2-20		3-3
BC264B	50/77	2-20		3-3
BC264C	50/77	2-20		3-3

*JAN qualification pending. Consult factory.
†Process in development

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BC264D	50/77	2-20		3-3
BF244A	50/74	2-20		3-3
BF244B	50/74	2-20		3-3
BF244C	50/74	2-20		3-3
BF245A	50/77	2-20		3-3
BF245B	50/77	2-20		3-3
BF245C	50/77	2-20		3-3
BF246A	51/74	2-20		3-6
BF246B	51/74	2-20		3-6
BF246C	51/74	2-20		3-6
BF247A	51/77	2-20		3-6
BF247B	51/77	2-20		3-6
BF247C	51/77	2-20		3-6
BF256A	50/77	2-20		3-3
BF256B	50/77	2-20		3-3
BF256C	50/77	2-20		3-3
J108	58/72	2-10	4-30	3-14
J109	58/72	2-10	4-30	3-14
J110	58/72	2-10	4-30	3-14
J111	51/72	2-10	4-31	3-6
J112	51/72	2-10	4-31	3-6
J113	51/72	2-10	4-31	3-6
J114	90/72	2-10		3-25
J174	88/74	2-19	4-32	3-21
J175	88/74	2-19	4-32	3-21
J176	88/74	2-19	4-32	3-21
J177	88/74	2-19	4-32	3-21
J201	52/72	2-14	4-33	3-8
J202	52/72	2-14	4-33	3-8
J203	52/72	2-14	4-33	3-8
J210	90/72	2-14	4-34	3-25
J211	90/72	2-14	4-34	3-25
J212	90/72	2-14	4-34	3-25
J270	88/74	2-20	4-35	3-21
J271	88/74	2-20	4-35	3-21
J300	90/72	2-11	4-36	3-25
J304	50/72	2-11	4-37	3-3
J305	50/72	2-11	4-37	3-3
J308	92/72	2-11		3-27
J309	92/72	2-11	4-38	3-27
J310	92/72	2-11	4-38	3-27
J401	†98/60	2-16		3-37
J402	†98/60	2-16		3-37
J403	†98/60	2-16		3-37
J404	†98/60	2-16		3-37
J405	†98/60	2-16		3-37
J406	†98/60	2-16		3-37
J410	83/60	2-16		3-16

†Process in development

FET Parts List (Continued)

DEVICE	PROCESS/PACKAGE	SELECTION GUIDE	PREFERRED PARTS DATA SHEET	PROCESS PAGE
J411	83/60	2-16		3-16
J412	83/60	2-16		3-16
MPF102	50/72	2-12		3-3
MPF103	55/72	2-14		3-12
MPF104	55/72	2-14		3-12
MPF105	55/72	2-14		3-12
MPF106	50/72	2-12		3-3
MPF107	50/72	2-12		3-3
MPF108	55/72	2-12		3-12
MPF109	55/72	2-14		3-12
MPF111	50/72	2-15		3-3
MPF112	55/72	2-15		3-12
NDF9401	94/24	2-18		3-31
NDF9402	94/24	2-18		3-31
NDF9403	94/24	2-18		3-31
NDF9404	94/24	2-18		3-31
NDF9405	94/24	2-18		3-31
NDF9406	94/12	2-18	4-39	3-31
NDF9407	94/12	2-18	4-39	3-31
NDF9408	94/12	2-18	4-39	3-31
NDF9409	94/12	2-18	4-39	3-31
NDF9410	94/12	2-18	4-39	3-31
NF5101	51/25	2-12	4-40	3-6
NF5102	51/25	2-12	4-40	3-6
NF5103	51/25	2-12	4-40	3-6
NPD5564	96/67	2-17	4-24	3-35
NPD5565	96/67	2-17	4-24	3-35
NPD5566	96/67	2-17	4-24	3-35
NPD8301	83/67	2-16	4-41	3-16
NPD8302	83/67	2-16	4-41	3-16
NPD8303	83/67	2-16	4-41	3-16
NPD9801	†98/67	2-16		
NPD9802	†98/67	2-16		
NPD9803	†98/67	2-16		
P1086E	88/71	2-19		3-21
P1087E	88/71	2-19		3-21
PF5101	51/72	2-12	4-40	3-6
PF5102	51/72	2-12	4-40	3-6
PF5103	51/72	2-12	4-40	3-6
PN3684	52/72	2-15	4-3	3-8
PN3685	52/72	2-15	4-3	3-8
PN3686	52/72	2-15	4-3	3-8
PN3687	52/72	2-15	4-3	3-8
PN4091	51/72	2-10	4-6	3-6
PN4092	51/72	2-10	4-6	3-6
PN4093	51/72	2-10	4-6	3-6
PN4220	55/72	2-15		3-12
PN4221	55/72	2-15		3-12

†Process in development

FET Parts List (Continued)

DEVICE	PROCESS/PACKAGE	SELECTION GUIDE	PREFERRED PARTS DATA SHEET	PROCESS PAGE
PN4222	55/72	2-15		3-12
PN4223	50/72	2-12		3-3
PN4224	50/72	2-12		3-3
PN4302	52/72	2-15		3-8
PN4303	52/72	2-15		3-8
PN4304	52/72	2-15		3-8
PN4342	89/71	2-20		3-23
PN4343	88/71	2-20		3-21
PN4360	89/71	2-20		3-23
PN4391	51/72	2-10	4-9	3-6
PN4392	51/72	2-10	4-9	3-6
PN4393	51/72	2-10	4-9	3-6
PN4416	50/72	2-12		3-3
PN4856	51/72	2-10	4-11	3-6
PN4857	51/72	2-10	4-11	3-6
PN4858	51/72	2-10	4-11	3-6
PN4859	51/72	2-10		3-6
PN4860	51/72	2-10		3-6
PN4861	51/72	2-10		3-6
PN5033	89/71	2-20		3-23
PN5163	50/72	2-15		3-3
TIS58	50/74	2-15		3-3
TIS59	50/74	2-15		3-3
TIS73	51/77	2-10		3-6
TIS74	51/77	2-10		3-6
TIS75	51/77	2-10		3-6
U1897E	51/72	2-10		3-6
U1898E	51/72	2-10		3-6
U1899E	51/72	2-10		3-6
U231	83/12	2-16		3-16
U232	83/12	2-16		3-16
U233	83/12	2-16		3-16
U234	83/12	2-16		3-16
U235	83/12	2-16		3-16
U257	93/24	2-17		3-29
U300	88/11	2-20		3-21
U301	88/11	2-20		3-21
U304	88/11	2-19		3-21
U305	88/11	2-19		3-21
U306	88/11	2-19		3-21
U308	92/07	2-12		3-27
U309	92/07	2-12	4-42	3-27
U310	92/07	2-12	4-42	3-27
U312	90/07	2-12		3-25
U320	58/09	2-12		3-14
U321	58/09	2-12		3-14
U322	58/09	2-12		3-14
U401	†98/12	2-16		3-37

†Process in development

FET Parts List (Continued)

DEVICE	PROCESS/PACKAGE	SELECTION GUIDE	PREFERRED PARTS DATA SHEET	PROCESS PAGE
U402	†98/12	2-16		3-37
U403	†98/12	2-16		3-37
U404	†98/12	2-16		3-37
U405	†98/12	2-16		3-37
U406	†98/12	2-16		3-37
U421	†86/24	2-18		3-20
U422	†86/24	2-18		3-20
U423	†86/24	2-18		3-20
U424	†86/24	2-18		3-20
U425	†86/24	2-18		3-20
U426	†86/24	2-18		3-20
U430	92/24	2-17		3-27
U431	92/24	2-17		3-27

†Process in development

JFET Cross Reference Guide

This guide contains cross reference information to more than 850 Junction FETs, including many obsolete or otherwise unavailable types. Every effort has been made to recommend a replacement FET which will plug into an existing socket and work as well as the part it replaces. Let the replacement code be your guide. If you do not find a particular part in this guide and you know its specification, you should refer to "How To Use This Catalog" in this section.

REPLACEMENT CODE

* Identical specification and pin configuration

● Equal or better specification, identical pin configuration

■ Similar specification acceptable for all but the most critical applications, similar pin configuration

CF Consult Factory or Local Sales Representative, available on special order

N No equivalent process

INDUSTRY TYPE NUMBER	REPLACEMENT CODE	NATIONAL PART NUMBER
2N2386	■	2N2608
2N2386A	■	2N4381
2N2497	■	2N5021
2N2498	■	2N5021
2N2499	■	2N4381
2N2500	■	2N4381
2N2606	N	
2N2607	N	
2N2608	*	2N2608
2N2609	*	2N2609
2N2841	N	
2N2842	N	
2N2843	■	2N5020
2N2844	■	2N5020
2N3066	●	2N4340
2N3067	●	2N4338
2N3068	■	2N4338
2N3069	*	2N3069
2N3070	*	2N3070
2N3071	*	2N3071
2N3084	■	2N4340
2N3085	●	2N4340
2N3086	■	2N4340
2N3087	●	2N4340
2N3088	■	2N4339
2N3088A	■	2N4339
2N3089	●	2N4339
2N3089A	●	2N4339
2N3277	N	
2N3278	N	
2N3328	●	2N3330
2N3329	*	2N3329
2N3330	*	2N3330
2N3331	*	2N3331
2N3332	*	2N3332
2N3365	■	2N4340
2N3366	■	2N4338
2N3367	■	2N4338
2N3368	*	2N3368
2N3369	*	2N3369
2N3370	*	2N3370
2N3376	●	2N3329
2N3378	■	2N3330
2N3380	●	2N3331
2N3382	*	2N3382
2N3384	*	2N3384
2N3386	*	2N3386
2N3436	*	2N3436
2N3437	*	2N3437
2N3438	*	2N3438
2N3452	■	2N3685
2N3453	■	2N4118
2N3454	■	2N4119
2N3455	■	2N3685
2N3456	■	2N4118
2N3457	■	2N4119
2N3458	*	2N3458
2N3459	*	2N3459
2N3460	*	2N3460
2N3574	■	2N3329
2N3575	■	2N3329
2N3578	●	2N2608
2N3684	*	2N3684
2N3684A	●	2N3684
2N3685	*	2N3685
2N3685A	●	2N3685
2N3686	*	2N3686
2N3686A	●	2N3686
2N3687	*	2N3687
2N3687A	●	2N3687
2N3819	*	2N3819
2N3820	*	2N3820
2N3821	*	2N3821
2N3822	*	2N3822
2N3823	*	2N3823
2N3824	*	2N3824
2N3909	●	2N3331
2N3909A	●	2N3331
2N3921	*	2N3921
2N3922	*	2N3922
2N3954	*	2N3954
2N3954A	*	2N3954A
2N3955	*	2N3955
2N3955A	*	2N3955A
2N3956	*	2N3956
2N3957	*	2N3957
2N3958	*	2N3958
2N3966	*	2N3966

JFET Cross Reference Guide (Continued)

INDUSTRY TYPE NUMBER	REPLACEMENT CODE	NATIONAL PART NUMBER
2N3967	*	2N3967
2N3967A	*	2N3967A
2N3968	*	2N3968
2N3968A	*	2N3968A
2N3969	*	2N3969
2N3969A	*	2N3969A
2N3970	*	2N3970
2N3971	*	2N3971
2N3972	*	2N3972
2N3993	*	2N3993
2N3993A	*	2N3993A
2N3994	*	2N3994
2N3994A	*	2N3994A
2N4082	CF	
2N4083	CF	
2N4084	*	2N4084
2N4085	*	2N4085
2N4091	*	2N4091
2N4092	*	2N4092
2N4093	*	2N4093
2N4117	*	2N4117
2N4117A	*	2N4117A
2N4118	*	2N4118
2N4118A	*	2N4118A
2N4119	*	2N4119
2N4119A	*	2N4119A
2N4139	CF	
2N4220	*	2N4220
2N4220A	*	2N4220A
2N4221	*	2N4221
2N4221A	*	2N4221A
2N4222	*	2N4222
2N4222A	*	2N4222A
2N4223	*	2N4223
2N4224	*	2N4224
2N4302	●	PN4302
2N4303	●	PN4303
2N4304	●	PN4304
2N4338	*	2N4338
2N4339	*	2N4339
2N4340	*	2N4340
2N4341	*	2N4341
2N4342	●	PN4342
2N4343	●	PN4343
2N4360	●	PN4360
2N4381	*	2N4381
2N4382	*	2N4382
2N4391	*	2N4391
2N4392	*	2N4392
2N4393	*	2N4393
2N4416	*	2N4416
2N4416A	*	2N4416A
2N4417	N	
2N4445	●	2N5432
2N4446	●	2N5433
2N4447	●	2N5432
2N4448	●	2N5433

INDUSTRY TYPE NUMBER	REPLACEMENT CODE	NATIONAL PART NUMBER
2N4856	*	2N4856
2N4856A	*	2N4856A
2N4857	*	2N4857
2N4857A	*	2N4857A
2N4858	*	2N4858
2N4858A	*	2N4858A
2N4859	*	2N4859
2N4859A	*	2N4859A
2N4860	*	2N4860
2N4860A	*	2N4860A
2N4861	*	2N4861
2N4861A	*	2N4861A
2N4867	CF	
2N4867A	CF	
2N4868	CF	
2N4868A	CF	
2N4869	CF	
2N4869A	CF	
2N4881	N	
2N4882	N	
2N4883	N	
2N4884	N	
2N4885	N	
2N4886	N	
2N4977	■	2N5432
2N4978	■	2N5433
2N4979	■	2N5434
2N5018	*	2N5018
2N5019	*	2N5019
2N5020	*	2N5020
2N5021	*	2N5021
2N5033	●	PN5033
2N5045	*	2N5045
2N5046	*	2N5046
2N5047	*	2N5047
2N5078	*	2N5078
2N5103	*	2N5103
2N5104	*	2N5104
2N5105	*	2N5105
2N5114	*	2N5114
2N5115	*	2N5115
2N5116	*	2N5116
2N5163	*	2N5163
2N5196	*	2N5196
2N5197	*	2N5197
2N5198	*	2N5198
2N5199	*	2N5199
2N5245	*	2N5245
2N5246	*	2N5246
2N5247	*	2N5247
2N5248	*	2N5248
2N5265	CF	
2N5266	CF	
2N5267	CF	
2N5268	CF	
2N5269	CF	
2N5270	CF	

JFET Cross Reference Guide (Continued)

INDUSTRY TYPE NUMBER	REPLACEMENT CODE	NATIONAL PART NUMBER
2N5277	N	
2N5278	N	
2N5358	*	2N5358
2N5359	*	2N5359
2N5360	*	2N5360
2N5361	*	2N5361
2N5362	*	2N5362
2N5363	*	2N5363
2N5364	*	2N5364
2N5391	CF	
2N5392	CF	
2N5393	CF	
2N5394	CF	
2N5395	CF	
2N5396	CF	
2N5397	*	2N5397
2N5398	*	2N5398
2N5432	*	2N5432
2N5433	*	2N5433
2N5434	*	2N5434
2N5452	*	2N5452
2N5453	*	2N5453
2N5454	*	2N5454
2N5457	*	2N5457
2N5458	*	2N5458
2N5459	*	2N5459
2N5460	*	2N5460
2N5461	*	2N5461
2N5462	*	2N5462
2N5463	N	
2N5464	N	
2N5465	N	
2N5471	■	2N5020
2N5472	■	2N5020
2N5473	■	2N5020
2N5474	■	2N5020
2N5475	■	2N5020
2N5476	■	2N5020
2N5484	*	2N5484
2N5485	*	2N5485
2N5486	*	2N5486
2N5515	*	2N5515
2N5516	*	2N5516
2N5517	*	2N5517
2N5518	*	2N5518
2N5519	*	2N5519
2N5520	*	2N5520
2N5521	*	2N5521
2N5522	*	2N5522
2N5523	*	2N5523
2N5524	*	2N5524
2N5543	N	
2N5544	N	
2N5545	*	2N5545
2N5546	*	2N5546
2N5547	*	2N5547
2N5549	●	2N5397

INDUSTRY TYPE NUMBER	REPLACEMENT CODE	NATIONAL PART NUMBER
2N5555	*	2N5555
2N5556	*	2N5556
2N5557	*	2N5557
2N5558	*	2N5558
2N5561	*	2N5561
2N5562	*	2N5562
2N5563	*	2N5563
2N5564	*	2N5564
2N5565	*	2N5565
2N5566	*	2N5566
2N5638	*	2N5638
2N5639	*	2N5639
2N5640	*	2N5640
2N5647	■	2N3686
2N5648	■	2N3686
2N5649	■	2N3685
2N5653	*	2N5653
2N5654	*	2N5654
2N5668	*	2N5668
2N5669	*	2N5669
2N5670	*	2N5670
2N5902	*	2N5902
2N5903	*	2N5903
2N5904	*	2N5904
2N5905	*	2N5905
2N5906	*	2N5906
2N5907	*	2N5907
2N5908	*	2N5908
2N5909	*	2N5909
2N5911	*	2N5911
2N5912	*	2N5912
2N5949	*	2N5949
2N5950	*	2N5950
2N5951	*	2N5951
2N5952	*	2N5952
2N5953	*	2N5953
2N6449	N	
2N6450	N	
2N6451	CF	
2N6452	CF	
2N6453	CF	
2N6454	CF	
2N6483	*	2N6483
2N6484	*	2N6484
2N6485	*	2N6485
A5T6449	N	
A5T6450	N	
AD3954	●	2N3954
AD3954A	●	2N3954A
AD3955	●	2N3955
AD3955A	●	2N3955A
AD3956	●	2N3956
AD3957	●	2N3957
AD3958	●	2N3958
AD5905	●	2N5905
AD5906	●	2N5906
AD5907	●	2N5907

JFET Cross Reference Guide (Continued)

INDUSTRY TYPE NUMBER	REPLACEMENT CODE	NATIONAL PART NUMBER
AD5908	●	2N5908
AD5909	●	2N5909
AD830	■	2N5906
AD831	■	2N5907
AD832	■	2N5908
AD833	■	2N5909
AD833A	■	2N5909
AD835	■	NDF9407
AD836	■	NDF9408
AD837	■	NDF9408
AD838	■	NDF9409
AD839	■	NDF9410
AD840	■	2N5520
AD841	■	2N5521
AD842	■	2N5523
AD845	■	2N5911
AD846	■	2N5912
BF244A	*	BF244A
BF244B	*	BF244B
BF244C	*	BF244C
BF245A	*	BF245A
BF245B	*	BF245B
BF245C	*	BF245C
BF246A	*	BF246A
BF246B	*	BF246B
BF246C	*	BF246C
BF247A	*	BF247A
BF247B	*	BF247B
BF247C	*	BF247C
BF256A	*	BF256A
BF256B	*	BF256B
BF256C	*	BF256C
BF264A	*	BF264A
BF264B	*	BF264B
BF264C	*	BF264C
BF264D	*	BF264D
C413N	●	2N4859
C681	■	2N4338
C681A	■	2N4338
C683	■	2N4339
C683A	■	2N4339
C685	■	2N4220
C685A	■	2N4220
CM640	■	2N4391
CM641	■	2N4391
CM642	■	2N4392
CM643	■	2N4391
CM644	■	2N4393
CM645	■	2N4392
CM646	■	2N4392
CM647	■	
CP640	●	U322
CP643	■	2N4391
CP650	●	U322
CP651	●	U320
CP652	●	U322
CP653	●	U320

INDUSTRY TYPE NUMBER	REPLACEMENT CODE	NATIONAL PART NUMBER
E100	●	J202
E101	●	J201
E102	●	J202
E103	●	J203
E105	N	
E106	N	
E107	N	
E108	●	J108
E109	●	J109
E110	●	J110
E111	●	J111
E112	●	J112
E113	●	J113
E114	●	J114
E174	●	J174
E175	●	J175
E176	●	J176
E177	●	J177
E201	●	J201
E202	●	J202
E203	●	J203
E210	●	J210
E211	●	J211
E212	●	J212
E230	■	PN3685
E231	■	PN3684
E232	■	PN368
E270	●	J270
E271	●	J271
E300	●	J300
E304	●	J304
E305	●	J305
E308	●	J308
E309	●	J309
E310	●	J310
E311	●	J309
E312	●	J310
E400	CF	
E401	CF	
E402	CF	
E410	CF	
E411	CF	
E412	CF	
E420	■	U257
E421	■	U257
FEO654A	●	PN4416
FEO654B	●	PN4303
FE3819	●	2N3819
FE5245	●	2N5245
FE5246	●	2N5246
FE5247	●	2N5247
FE5457	●	2N5457
FE5458	●	2N5458
FE5459	●	2N5459
FE5484	●	2N5484
FE5485	●	2N5485
FE5486	●	2N5486

JFET Cross Reference Guide (Continued)

INDUSTRY TYPE NUMBER	REPLACEMENT CODE	NATIONAL PART NUMBER
FM1100A	■	2N5906
FM1101A	■	2N5906
FM1102A	■	2N5907
FM1103A	■	2N5908
FM1104A	■	2N5909
FM105A	■	NDF9401
FM1106A	■	NDF9401
FM1107A	■	NDF9402
FM1108A	■	NDF9403
FM1109A	■	NDF9405
FM1110A	■	2N3957
FM1111A	■	2N3958
FM3954	●	2N3954
FM3954A	●	2N3954A
FM3955	●	2N3955
FM3955A	●	2N3955A
FM3956	●	2N3956
FM3957	●	2N3957
FM3958	●	2N3958
FT0654A	■	2N3824
FT0654B	■	2N3824
FT0654C	■	2N4221
FT3820	●	2N3820
IMF3954	●	2N3954
IMF3954A	●	2N3954A
IMF3955	●	2N3955
IMF3955A	●	2N3955A
IMF3956	●	2N3956
IMF3957	●	2N3957
IMF3958	●	2N3958
IT100	■	2N5115
IT101	■	2N5116
IT108	●	2N5486
IT109	●	2N5397
ITE3066	■	2N4340
ITE3067	■	2N4338
ITE3068	■	2N4338
ITE4117	●	2N4117
ITE4118	●	2N4118
ITE4119	●	2N4119
ITE4338	●	2N4338
ITE4339	●	2N4339
ITE4340	●	2N4340
ITE4341	●	2N4391
ITE4391	*	PN4391
ITE4392	*	PN4392
ITE4393	●	PN4393
ITE4416	●	PN4416
ITE4867	■	PN3686
ITE4868	■	PN3685
ITE4869	■	PN3684
J108	*	J108
J109	*	J109
J110	*	J110
J111	*	J111
J112	*	J112
J113	*	J113

INDUSTRY TYPE NUMBER	REPLACEMENT CODE	NATIONAL PART NUMBER
J114	*	J114
J174	*	J174
J175	*	J175
J176	*	J176
J177	*	J177
J201	*	J201
J202	*	J202
J203	*	J203
J270	*	J270
J271	*	J271
J300	*	J300
J304	*	J304
J305	*	J305
J401	*	J401
J402	*	J402
J403	*	J403
J404	*	J404
J405	*	J405
J406	*	J406
J410	*	J410
J411	*	J411
J412	*	J412
J1401	*	J1401
J1402	*	J1402
J1403	*	J1403
J1404	*	J1404
J1405	*	J1405
J1406	*	J1406
KE3684	●	PN3684
KE3685	●	PN3685
KE3686	●	PN3686
KE3970	●	PN4391
KE3971	●	PN4392
KE3972	●	PN4393
KE4091	●	PN4091
KE4092	●	PN4092
KE4093	●	PN4093
KE4220	●	PN4220
KE4221	●	PN4221
KE4222	●	PN4222
KE4223	●	PN4223
KE4224	●	PN4224
KE4391	●	PN4391
KE4392	●	PN4392
KE4393	●	PN4393
KE4416	●	PN4416
KE4856	●	PN4856
KE4857	●	PN4857
KE4858	●	PN4858
KE4859	●	PN4859
KE4860	●	PN4860
KE4861	●	PN4861
KE5103	●	2N5952
KE5104	●	2N5953
KE5105	■	PN4416
MFE2000	■	2N4416
MFE2001	■	2N4416

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INDUSTRY TYPE NUMBER	REPLACEMENT CODE	NATIONAL PART NUMBER
MFE2004	■	2N4393
MFE2005	■	2N4392
MFE2006	■	2N4391
MFE2007	■	2N4857
MFE2008	■	2N4391
MFE2009	■	2N4856
MFE2010	■	2N4856
MFE2011	■	2N5433
MFE2012	■	2N5433
MFE2093	■	2N3687
MFE2094	■	2N3686
MFE2095	■	2N3685
MFE2133	■	2N4392
MFE4007	■	2N2608
MFE4008	■	2N2608
MFE4009	■	2N3329
MFE4010	■	2N3330
MFE4011	■	2N3330
MFE4012	■	2N3331
MPF102	*	MPF102
MPF103	*	MPF103
MPF104	*	MPF104
MPF105	*	MPF105
MPF106	*	MPF106
MPF107	*	MPF107
MPF108	*	MPF108
MPF109	*	MPF109
MPF111	*	MPF111
MPF112	*	MPF112
MPF161	●	2N5461
MPF256	●	J211
MPF820	■	J309
MPF970	●	P1086E
MPF971	●	P1087E
MPF4391	*	PN4391
MPF4392	*	PN4392
MPF4393	*	PN4393
NDF9401	*	NDF9401
NDF9402	*	NDF9402
NDF9403	*	NDF9403
NDF9404	*	NDF9404
NDF9405	*	NDF9405
NDF9406	*	NDF9406
NDF9407	*	NDF9407
NDF9408	*	NDF9408
NDF9409	*	NDF9409
NDF9410	*	NDF9410
NF500	●	2N4224
NF501	●	2N4224
NF506	●	2N3823
NF510	●	2N4092
NF520	●	2N4224
NF521	●	2N4220
NF522	●	2N4224
NF523	●	2N4220
NF530	●	2N3822
NF531	●	2N3821

INDUSTRY TYPE NUMBER	REPLACEMENT CODE	NATIONAL PART NUMBER
NF532	●	2N3822
NF533	●	2N3821
NF580	●	2N5432
NF581	●	2N5432
NF582	●	2N5434
NF583	●	2N5434
NF584	●	2N5432
NF585	●	2N5433
NF4302	●	PN4302
NF4303	●	PN4303
NF4304	●	PN4304
NF4445	●	2N5432
NF4446	●	2N5433
NF4447	●	2N5432
NF4448	●	2N5433
NF5101	*	NF5101
NF5102	*	NF5102
NF5103	*	NF5103
NF5163	●	2N5163
NF5457	●	2N5457
NF5458	●	2N5458
NF5459	●	2N5459
NF5485	●	2N5485
NF5486	●	2N5486
NF5555	●	2N5555
NF5638	●	2N5638
NF5639	●	2N5639
NF5640	●	2N5640
NF5653	●	2N5653
NF5654	●	2N5654
NPD5564	*	NPD5564
NPD5565	*	NPD5565
NPD5566	*	NPD5566
NPD8301	*	NPD8301
NPD8302	*	NPD8302
NPD8303	*	NPD8303
NPD9801	*	NPD9801
NPD9802	*	NPD9802
NPD9803	*	NPD9803
P1069E		
P1086E	*	P1086E
P1087E	*	P1087E
P1117E	CF	
P1118E	CF	
P1119E	CF	
PF510	●	PN4392
PF511	●	PN4392
PF5101	*	PF5101
PF5102	*	PF5102
PF5103	*	PF5103
PN3684	*	PN3684
PN3685	*	PN3685
PN3686	*	PN3686
PN3687	*	PN3687
PN4091	*	PN4091
PN4092	*	PN4092
PN4093	*	PN4093

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INDUSTRY TYPE NUMBER	REPLACEMENT CODE	NATIONAL PART NUMBER
PN4220	*	PN4220
PN4221	*	PN4221
PN4222	*	PN4222
PN4223	*	PN4223
PN4224	*	PN4224
PN4302	*	PN4302
PN4303	*	PN4303
PN4304	*	PN4304
PN4342	*	PN4342
PN4343	*	PN4343
PN4360	*	PN4360
PN4391	*	PN4391
PN4392	*	PN4392
PN4393	*	PN4393
PN4416	*	PN4416
PN4856	*	PN4856
PN4857	*	PN4857
PN4858	*	PN4858
PN4859	*	PN4859
PN4860	*	PN4860
PN4861	*	PN4861
PN5033	*	PN5033
PN5163	*	PN5163
SU2078	●	2N3955
SU2079	●	2N3956
SU2080		
SU2081		
SU2098	●	2N3954
SU2098A	●	2N3954
SU2098B	●	2N3954A
SU2099	●	2N3955A
SU2099A	●	2N3955A
SU2365	●	U401
SU2365A	●	U401
SU2366	●	U402
SU2366A	●	U402
SU2367	●	U403
SU2367A	●	U403
SU2368	●	U404
SU2368A	●	U404
SU2369	●	U405
SU2369A	●	U405
SU2410	■	U424
SU2411	■	U425
SU2412	■	U426
TD5452	■	2N5452
TD5453	■	2N5453
TD5454	■	2N5454
TD5902	■	2N5902
TD5902A	■	2N5902
TD5903	■	2N5903
TD5903A	■	2N5903
TD5904	■	2N5904
TD5904A	■	2N5904
TD5905	■	2N5905
TD5905A	■	2N5905
TD5906	■	2N5906

INDUSTRY TYPE NUMBER	REPLACEMENT CODE	NATIONAL PART NUMBER
TD5906A	■	2N5906
TD5907	■	2N5907
TD5907A	■	2N5907
TD5908	■	2N5908
TD5908A	■	2N5908
TD5909	■	2N5909
TD5909A	■	2N5909
TD5911	■	2N5911
TD5911A	■	2N5911
TD5912	■	2N5912
TD5912A	■	2N5912
TIS25	N	
TIS26	N	
TIS27	N	
TIS34	●	2N5486
TIS41	■	2N4859
TIS42	■	PN4392
TIS58	*	TIS58
TIS59	*	TIS59
TIS68	N	
TIS69	N	
TIS70	N	
TIS73	*	TIS73
TIS74	*	TIS74
TIS75	*	TIS75
TIS78	N	
TIS79	N	
TIS88A	●	2N5486
U110	■	2N5020
U112	●	2N4381
U114	■	2N5020
U133	■	2N5020
U146	●	2N5020
U147	●	2N5020
U148	●	2N2608
U149	●	2N2609
U168	●	2N2608
U182	●	2N4857
U183	●	2N3823
U184	●	2N4416
U197	●	2N4338
U198	●	2N4340
U199	●	2N4341
U200	●	2N4393
U201	●	2N4392
U202	●	2N4391
U231	*	U231
U232	*	U232
U233	*	U233
U234	*	U234
U235	*	U235
U240	●	2N5432
U241	●	2N5433
U242	●	2N5432
U243	●	2N5433
U244	N	
U248	*	2N5902

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INDUSTRY TYPE NUMBER	REPLACEMENT CODE	NATIONAL PART NUMBER
U248A	*	2N5906
U249	*	2N5903
U249A	*	2N5907
U250	*	2N5904
U250A	*	2N5908
U251	*	2N5905
U251A	*	2N5909
U252	*	2N5911
U253	*	2N5912
U254	*	2N4859
U255	*	2N4860
U256	*	2N4861
U257	●	U257
U266	N	
U280	●	2N3954
U281	●	2N3954
U282	●	2N3955
U283	●	2N3955
U284	●	2N3956
U285	●	2N3957
U290	N	
U291	N	
U300	*	U300
U301	*	U301
U304	●	2N5114
U305	●	2N5116
U306	●	2N5117
U308	*	U308
U309	*	U309
U310	*	U310
U311	●	U311
U312	*	U312
U320	*	U320
U321	*	U321
U322	*	U322
U328	N	
U329	N	
U330	N	
U331	N	
U350	*	U350
U401	*	U401
U402	*	U402
U403	*	U403
U404	*	U404
U405	*	U405
U406	*	U406
U421	*	U421
U422	*	U422
U423	*	U423
U424	*	U424
U425	*	U425
U426	*	U426
U430	*	U430
U431	*	U431
U1714	●	2N4340
U1715	N	
U1837E	●	2N5486

INDUSTRY TYPE NUMBER	REPLACEMENT CODE	NATIONAL PART NUMBER
U1897E	●	U1897E
U1898E	●	U1898E
U1899E	●	U1899E
U1994E	●	PN4416
U2047	●	PN4416
UC155	■	2N4416
UC200	■	2N4393
UC201	■	2N4416
UC210	■	2N3822
UC220	■	2N4220
UC241	■	2N3822
UC250	●	2N4391
UC251	●	2N4392
UC400	■	2N2609
UC401	■	2N5019
UC410	■	2N2609
UC420	■	2N3329
UC588	■	2N4416
UC703	■	2N3822
UC705	■	2N3824
UC707	■	2N4391
UC714	■	2N4416
UC734	■	2N4416
UC734E	■	PN4416
UC755	■	2N4391
UC756	■	2N4224
UC805	■	2N3331
UC807	■	2N4861
UC814	■	2N3331
UC851	■	2N2608
UC854	CF	
UC855	CF	
UC2139	CF	
UC2147	CF	
UC2148	CF	
UC2149	CF	
VCR2N	■	2N4092
VCR3P	■	2N5115
VCR4N	■	2N4341
VCR5P	■	2N3331
VCR7N	■	2N4119

DEVICE NUMBER	TYPE/R_{ON}/V_A/V_S	NATIONAL PIN-FOR-PIN	FUNCTIONAL EQUIVALENT
Analog Devices			
AD7516	4-SPST/280Ω/±7.5V/±7.5V	CD4066	
Fairchild			
F4016	4-SPST/800Ω/±7.5V/±7.5V	CD4016	
F4051	8-Ch. MUX/280Ω/±7.5V/±7.5V	CD4051	
F4052	4-Ch. MUX/280Ω/±7.5V/±7.5V	CD4052	
F4053	3-SPDT/280Ω/±7.5V/±7.5V	CD4053	
F4066	4-SPST/280Ω/±7.5V/±7.5V	CD4066	
Harris			
HD4051	8-Ch MUX/280Ω/±7.5V/±7.5V	CD4051	
HD4052	4-Ch MUX/280Ω/±7.5V/±7.5V	CD4052	
HD4053	3 SPDT/280Ω/±7.5V/±7.5V	CD4053	
HD4066	4-SPST/280Ω/±7.5V/±7.5V	CD4066	
Intersil			
DG111	2-SPST/100–450Ω/±10V/–20V, 10V,5V		AM182
DG112	2-SPST/100–450Ω/±10V/–20V, 10V,5V		AM182
DG116	4-SPST/100–450Ω/±10V/–20V, 10V,5V		AH0015
DG118	4-SPST/100–450Ω/±10V/–20V, 10V,5V		AH0015
DG126/DG426	2-DPST/80Ω/±10V/–18V,12V	AH0126	
DG129/DG429	2-DPST/30Ω/±10V/–18V,12V	AH0129	
DG133/DG433	2-SPST/30Ω/±10V/–18V,12V	AH0133	
DG134/DG434	2-SPST/80Ω/±10V/–18V,12V	AH0134	
DG139/DG439	DPDT/30Ω/±10V/±15V	AH0139	
DG140/DG440	2-DPST/10Ω/±10V/–18V,12V	AH0140	
DG141/DG441	2-SPST/10Ω/±10V/–18V,12V	AH0141	
DG142/DG442	DPDT/80Ω/±10V/–18V,12V	AH0142	
DG143/DG443	SPDT/80Ω/±10V/–18V,12V	AH0143	
DG144/DG444	SPDT/30Ω/±10V/–18V,12V	AH0144	
DG145/DG445	2-DPST/10Ω/±10V/–18V,12V	AH0145	
DG146/DG446	SPDT/10Ω/±10V/–18V,12V	AH0146	
DG151/DG451	2-SPST/15Ω/±7.5V/±15V	AH0151	
DG152/DG452	2-SPST/50Ω/±7.5V/±15V	AH0152	
DG153/DG453	2-DPST/10Ω/±7.5V/±15V	AH0153	
DG154/DG454	2-DPST/50Ω/±7.5V/±15V	AH0154	
DG161/DG461	SPDT/15Ω/±7.5V/±15V	AH0161	
DG162/DG462	SPDT/50Ω/±7.5V/±15V	AH0162	
DG163/DG463	DPDT/15Ω/±7.5V/±15V	AH0163	
DG164/DG464	DPDT/50Ω/±7.5V/±15V	AH0164	
DG172	4-SPST/200–600Ω/±10V/–20V, 10V, 5V		AH0015
DG181	2-SPST/30Ω/–7.5V,15V/±15V,5V	AM181	
DG182	2-SPST/75Ω/–10V,15V/±15V,5V	AM182	
DG184	2-DPST/30Ω/–7.5V, 15V/±15V,5V	AM184	
DG185	2-DPST/75Ω/–10V,15V/±15V,5V	AM185	
DG187	SPDT/30Ω/–7.5V,15V/±15V,5V	AM187	
DG188	SPDT/75Ω/–10V,15V/±15V,5V	AM188	
DG190	2-SPDT/30Ω/–7.5V,15V/±15V,5V	AM190	
DG191	2-SPDT/75Ω/–10V,15V/±15V,5V	AM191	
IH5001	SPST/30Ω/±8V/–18V,12V		1/2AH0133
IH5002	SPST/50Ω/±8V/–18V,12V		1/2AH0133
IH5003	2-SPST/30Ω/±10V/–18V,12V		AH0133
IH5004	2-SPST/50Ω/±10V/–18V,12V		AH0134
IH5005	2-SPST/10Ω/±10V/–18V,12V		AH0141
IH5006	2-SPST/30Ω/±10V/–18V,12V		AH0133
IH5007	2-SPST/80Ω/±10V/–18V,12V		AH0134
IH5009	4-Ch. MUX/100Ω/±0.2V	AH5009/AM9709	
IH5010	4-Ch. MUX/150Ω/±0.2V	AH5010/AM9710	
IH5011	4-SPST/100Ω/±0.2V	AH5011/AM9711	
IH5012	4-SPST/150Ω/±0.2V	AH5012/AM9712	
IH5013	3-SPST/100Ω/±0.2V	AH5013	
IH5014	3-SPST/150Ω/±0.2V	AH5014	
IH5015	3-SPST/100Ω/±0.2V	AH5015	
IH5016	3-SPST/150Ω/±0.2V	AH5016	
MM450/MM550	2-DPDT/200–600Ω/±10V	MM450/MM550	
MM451/MM551	4-Ch. MUX/200–600Ω/±10V	MM451/MM551	
MM452/MM552	4-SPST/200–600Ω/±10V	MM452/MM552	
MM455/MM555	3-SPST/200–600Ω/±10V	MM455/MM555	
DG508	8-Ch. MUX/450Ω/*/±15V	LF11508	
DG509	4-Ch. Diff. MUX/450Ω/*/±15V	LF11509	
IH5060	16-Ch. MUX/400Ω/*/±15V	LF11506	
IH5070	8-Ch. Diff. MUX/400Ω/*/±15V	LF11507	
Motorola			
MC14016	4-SPST/400Ω/±7.5V/±7.5V	CD4016	
MC14051	8-Ch. MUX/280Ω/±7.5V/±7.5V	CD4051	
MC14052	4-Ch. MUX/280Ω/±7.5V/±7.5V	CD4052	
MC14053	3-SPDT/280Ω/±7.5V/±7.5V	CD4053	
MC14066	4-SPDT/280Ω/±7.5V/±7.5V	CD4066	
MC14529	4-Ch. MUX/270Ω/±7.5V/±7.5V		CD4051

*Denotes items which have a maximum analog voltage of ±15V, the National equivalent devices have ±10V maximum analog voltage.

Analog Switch Cross Reference Guide

DEVICE NUMBER	TYPE/R_{ON}/V_A/V_S	NATIONAL PIN-FOR-PIN	FUNCTIONAL EQUIVALENT
RCA			
CD4016	4-SPST/850Ω/±7.5V/±7.5V	CD4016	
CD4051	8-Ch. MUX/280Ω/±7.5V/±7.5V	CD4051	
CD4052	4-Ch. MUX/280Ω/±7.5V/±7.5V	CD4052	
CD4053	3-SPDT/280Ω/±7.5V/±7.5V	CD4053	
CD4066	4-SPST/280Ω/±7.5V/±7.5V	CD4066	
Siliconix			
DG111	2-SPST/100–450Ω/±10V/–20V, –10V, –5V	AM0182	
DG126	2-DPST/80Ω/±10V/–18V,12V	AH0126	
DG129	2-DPST/30Ω/±10V/–18V,12V	AH0129	
DG133	2-SPST/30Ω/±10V/–18V,12V	AH0133	
DG134	2-SPST/80Ω/±10V/–18V,12V	AH0134	
DG139	DPDT/30Ω/±10V/±15V	AH0139	
DG140	2-DPST/10Ω/±10V/–18V,12V	AH0140	
DG141	2-SPST/10Ω/±10V/–18V,12V	AH0141	
DG142	DPDT/80Ω/±10V/–18V,12V	AH0142	
DG143	SPDT/80Ω/±10V/–18V,12V	AH0143	
DG144	SPDT/30Ω/±10V/–18V,12V	AH0144	
DG145	2-DPST/10Ω/±10V/–18V,12V	AH0145	
DG146	SPDT/10Ω/±10V/–18V,12V	AH0146	
DG151	2-SPST/15Ω/±7.5V/±15V	AH0151	
DG152	2-SPST/50Ω/±7.5V/±15V	AH0152	
DG153	2-DPST/10Ω/±7.5V/±15V	AH0153	
DG154	2-DPST/50Ω/±7.5V/±15V	AH0154	
DG161	SPDT/15Ω/±7.5V/±15V	AH0161	
DG162	SPDT/50Ω/±7.5V/±15V	AH0162	
DG163	DPDT/15Ω/±7.5V/±15V	AH0163	
DG164	DPDT/50Ω/±7.5V/±15V	AH0164	
DG172	4-SPST/200–600Ω/±10V/–20V, 10V,5V		AH0015
DG173	DPDT/150–500Ω/±10V/–20V 10V,5V	AH0014	
DG181	2-SPST/30Ω/–7.5V,15V/±15V,5V	AM181	
DG182	2-SPST/75Ω/–10V,15V/±15V,5V	AM182	
DG184	2-DPST/30Ω/7.5V,15V/±15V,5V	AM184	
DG185	2-DPST/75Ω/–10V,15V/±15V,5V	AM185	
DG187	SPDT/30Ω/–7.5V,15V/±15V,5V	AM187	
DG188	SPDT/75Ω/–10V,15V/±15V,5V	AM188	
DG190	2-SPDT/30Ω/–7.5V,15V/±15V,5V	AM190	
DG191	2-SPDT/75Ω/–10V,15V/±15V,5V	AM0191	
DG201	4-SPST/100Ω/*/±15V	LF11201	
DG501	8-Ch. MUX/200–800Ω/±5V/–15V,5V		AM3705
DG511	4-Ch. Diff. MUX/200–700Ω/±10V/ –20V, 10V		MM454/MM554
DG506	16-Ch. MUX/400Ω/*/±15V	LF11506	
DG507	8-Ch. Diff. MUX/400Ω/*/±15V	LF11507	
DG508	8-Ch. MUX/400Ω/*/±15V	LF11508	
DG509	4-Ch. Diff. MUX/400Ω/*/±15V	LF11509	
DGM122	2-DPST/100–500Ω/±10V/–20V, 10V,5V		AH0019
SI455/SI555	3-SPST/200–600Ω/±10V/–20V, 10V,5V		MM455/MM555
Solitron			
CM4016	4-SPST/400Ω/±7.5V/±7.5V	CD4016	
CM4051	8-Ch. MUX/280Ω/±7.5V/±7.5V	CD4051	
CM4052	4-Ch. MUX/280Ω/±7.5V/±7.5V	CD4052	
CM4053	3-SPDT/280Ω/±7.5V/±7.5V	CD4053	
CM4116	4-SPST/800Ω/±7.5V/±7.5V	CD4016	
Teledyne–Crystalonics			
CAG-10	SPST/50Ω/–10V,4V/±15V,5V		1/2AM182
CAG-13	2-SPST/50Ω/±10V/–18V,15V		AH0134
CAG-14	SPST/50Ω/–10V,5V/±15V,5V		1/2AM0182
CAG-21	2-DPST/30Ω/–6V,10V/–18V,15V		AH0129
CAG-22	2-SPST/30Ω/–6V,10V/–18V,15V		AH0133
CAG-23	2-SPST/50Ω/±10V/–18V,15V		AH0134
CAG-24	2-SPST/30Ω/–6V,10V/–18V,15V		AH0133
CAG-27-10	2-SPST/10Ω/–6V,10V/–18V,15V		AH0141
CAG-30	SPST/60Ω/±10V/±15V,5V		1/2AM182
CAG-42	2-SPST/60Ω/±10V/–18V,15V		AH0134
CAG-45	2-SPST/60Ω/±10V/–18V,15V		AH0134
CAG-48	2-SPST/60Ω/±10V/–18V,15V		AH0134
CD4066	4-SPST/280Ω/±7.5V/±7.5V	CD4066	
CS4R	2-DPST/15Ω/±10V/–18V,15V		AH0140
Texas Instruments			
TF4016	4-SPST/400Ω/±7.5V/±7.5V	CD4016	
TF4051	8-Ch. MUX/280Ω/±7.5V/±7.5V	CD4051	
TF4052	4-Ch. MUX/280Ω/±7.5V/±7.5V	CD4052	
TF4053	3-SPDT/280Ω/±7.5V/±7.5V	CD4053	

Section 2

FET Selector Guides

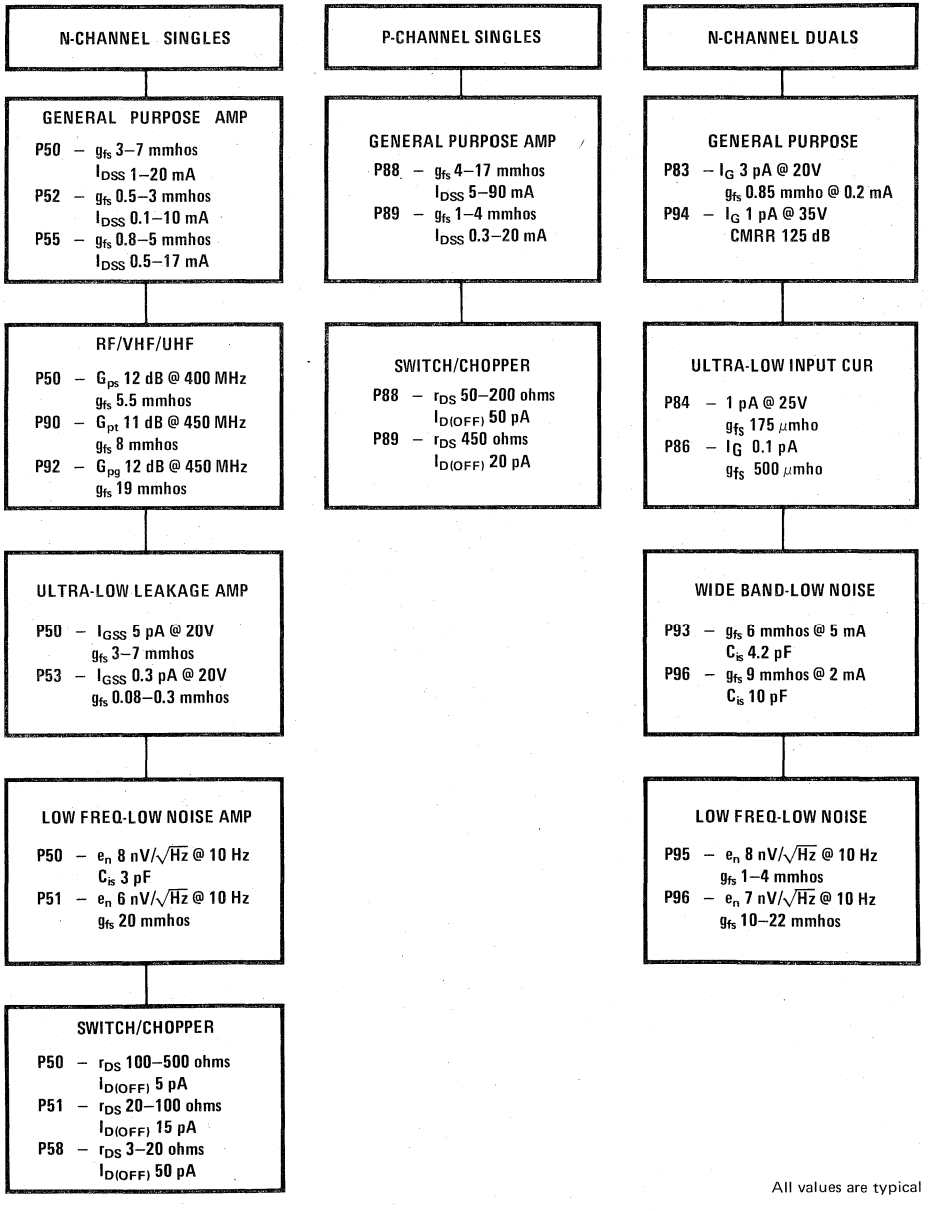
2

Choose The Proper FET

National Semiconductor utilizes 17 different FET geometries to cover, without compromise, the full spectrum of applications. Specific part number characteristics are summarized into application areas further on within this section. In addition, this section includes process comparison charts which graphically indicate the typical values of a given parameter for all geometries under identical test conditions. Detailed data on each process, along with a list of all part numbers manufactured from each process, is to be found in Section 3.

To further simplify the selection procedure, the FET Family Tree is included for quick identification. After narrowing down the process types, it is suggested that the process sheets and specific part number characteristics be consulted.

FET FAMILY TREE



All values are typical

FET Application Guide

National Semiconductor manufactures a broad line of silicon Junction Field Effect Transistors (JFETs). National's JFETs provide excellent performance in many areas such as RF amplifiers, analog switching, low input current amplifiers, low noise high impedance amplifiers and outstanding matched duals for operational amplifiers input applications.

The following FET guides enable the user to determine when to use FETs and where to look for the best choice.

POPULAR PRODUCT TYPES	2N4416, 2N5485, 6 PN4416, PN4302–4	2N4856–61, 2N4391–3 PN4856–61, PN4391–3	2N4338–41, 2N3684–7	2N4117–9, 2N3452–4 2N4117A–19A	2N3821–2, 2N4221–2 2N5457–9	2N5432–4	2N5196–9, 2N5545–7 2N3954–8	2N5902–9	U421–U426	2N5018–21, P1086–7E 2N5114–6	2N2608–9, 2N5460–62	2N5397, J300	U308–10, J308–10	2N5911–12	NDF9401–10	2N5515–24, 2N6483–5	2N5564–6	2N5561–63
PROCESS DESIGNATION	50	51	52	53	55	58	83	84	86	88	89	90	92	93	94	95	96	98
Low Current Amplifier			S	P	S		P	P	P		P				P	P		P
Low Freq Ampli $\leq$ 100 Hz			S		S		P			S	S				P	P		P
High Freq Ampli $>$ 100 MHz	P											P	P	P			P	
General Purpose Amplifier	P		P		P						P							
Low Noise Amp (10 Hz $\overline{e_n}$)	S	S			S	S	P								P	P	P	P
Low Noise Amp $>$ 50 MHz	P				S							P	P	P			P	
High Frequency Mixer	P											P	P					
Dual Diff Pair							P	P	P					P	P	S	P	P
AGC Amplifier	P				P													
Electrometer Preamp				P				P	P						P			S
Microvolt Amplifier				P				P	P						P			P
Low Leakage Diode				P														
Diff/Angle Ended Inp. Stag.							P	P	P					P	P		P	P
Active Filter	P		S		P						S							
Oscillator	P		S		P						S	P	P					
Voltage Variable Resistor	P	P	S		P					P	P							P
Hybrid Chips	P	P		P	P		P	P	P	P	P				P			
Analog/Digital Switch		P				P				P							S	S
Multiplexing	P	P			S	S				P								
Choppers		P				P				P							P	
Nixie Drivers																		
Reed Relay Replacement						P												
Sub pA Dual Diff Pair								P	P									
Sample-Hold	P	P			S				S	P								P
Buffer Interface to CMOS										P	P							
Matched Switch							S							S	S		P	P
HF $\geq$ 400 MHz Prime												P	P					
Current Limiter		P								P								
Current Source			P	S	P						S							

P – Prime Choice S – Secondary (Alternate) Choice

ADVANTAGES OF USING FIELD-EFFECT TRANSISTORS

APPLICATION	ADVANTAGES	FINAL ASSEMBLY WHERE USED
DC Amplifiers	High Z_{in} Low drift duals Low noise	Transducers, military guidance systems, control systems, temp indicators, multimeters
Low frequency amplifiers	Small coupling capacitors Low noise, distortion High input impedance	Sound detection, microphones, inductive transducers, hearing aids, high impedance transducers
Operational amplifiers	Summing point essentially zero. Low device noise. Less loading of transducers	Control systems, potted op amps, test equipment, medical electronics
Medium and high frequency amplifiers	Low cross modulation Low device noise Simplified circuitry	FM tuners, communication received scope inputs, most instrumentation equipment, high impedance inputs
Mixers – 100 MHz and up	Low mixing noise Low cross modulation	FM tuners, communication receivers
Oscillators	Low drift	Transmitters, receivers, organ
Logic gates	Virtually infinite fan in Simplified circuitry Zero storage time Symmetrical	Guidance controls, computer market mini military teaching aids, traffic control, telemetry
Choppers	Zero offset Low leakage currents Simplified circuitry Eliminates input transformers	Op amp modules guidance controls instrumentation equipment
AD Converters Multiplex switching (arrays) and sample hold	Improved isolation of input and output. Zero offset. Symmetrical. Low resistance Simplified circuitry	Control system, DVM's and any read-out equipment, medical electronics
Relay contact replacement	Solid state reliability Zero offset, High isolation Symmetrical No inductive spring No contact bounce High repetition rate	Test equipment, airborne equipment instrumentation market
Voltage variable resistor	Symmetrical Solid state reliability Functions as variable resistor. Low noise. High isolation Improved resolution	Organ, tone controls, control ckts to input operational amplifiers
Current limiters Sources	Two lead simplicity Wide selection range Low voltage operation	Hybrid circuits, amplifiers, power supply protection, timing ckts, voltage regulators

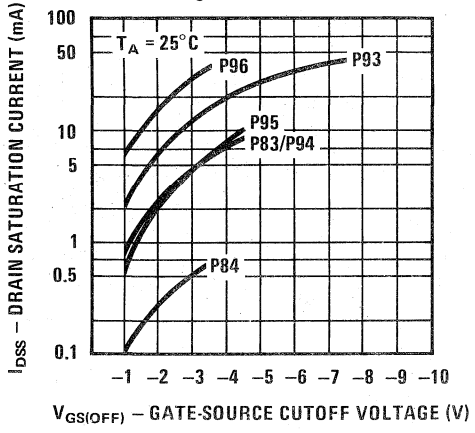
Important Parameters by Application

LISTED IN APPROXIMATE ORDER OF IMPORTANCE

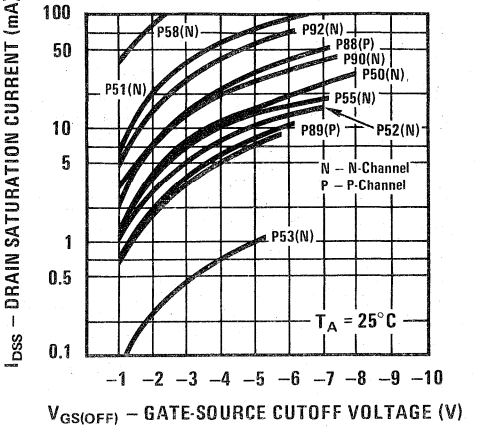
Low Frequency Amplifier	Source Follower	Electrometer Amplifier	Low Drift Amplifier	Low Noise Amplifier	High Frequency Amplifier	Oscillator	Differential Amplifier	Analog and Digital Switch
Y_{fs}	Y_{fs}	I_G	I_{DZ}	e_n	$Re(y_{fs})$	Y_{fs}	$\lvert V_{GS1}-V_{GS2}\rvert$	$R_{DS(ON)}$
I_{DSS}	I_G	Y_{fs}	Y_{fs} @ I_{DZ}	I_G	$Re(y_{is})$	I_{DSS}	$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	$I_{D(off)}$
$V_{GS(off)}$	C_{rss}	I_{DZ}	V_{GS} @ I_{DZ}	i_n	NF	C_{rss}	$\lvert I_{G1}-I_{G2}\rvert$	C_{iss}
C_{iss}	C_{iss}	e_n	I_G	Y_{fs}	C_{rss}	C_{iss}	I_G	C_{rss}
C_{rss}	I_{DSS}	g_{os}	BV_{GSS}	I_{DSS}	$Re(y_{os})$	$V_{GS(off)}$	Y_{fs}	$V_{GS(off)}$
e_n	$V_{GS(off)}$			$V_{GS(off)}$	I_{DSS}	BV_{GSS}	Y_{fs1}/Y_{fs2}	BV_{GSS}
BV_{GSS}	BV_{GSS}				$V_{GS(off)}$		$\lvert Y_{os1}-Y_{os2}\rvert$	
							CMRR	
							$V_{GS(off)}$	

FET Process Comparison Curves

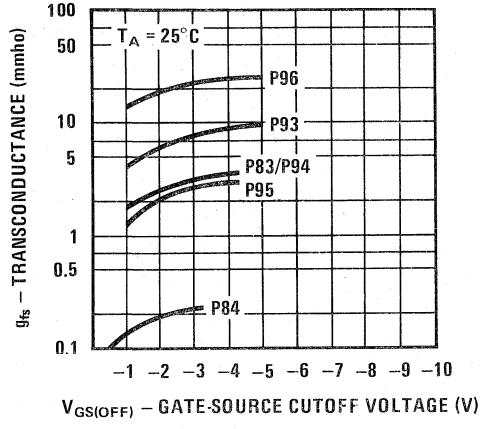
Dual FET Drain Saturation Current vs Cutoff Voltage



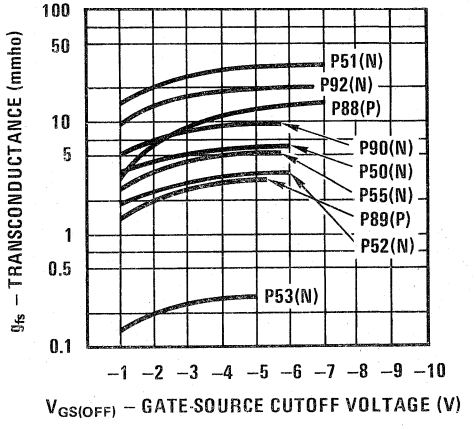
Single FET Drain Saturation Current vs Cutoff Voltage



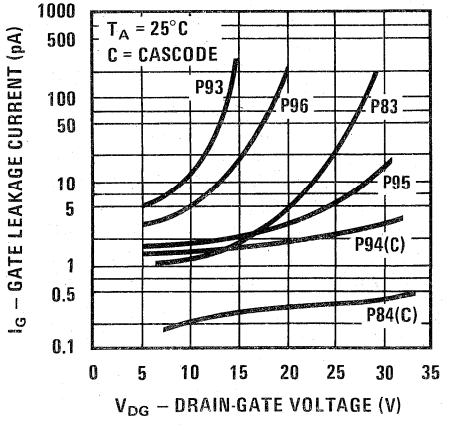
Dual FET Transconductance vs Cutoff Voltage



Single FET Transconductance vs Cutoff Voltage

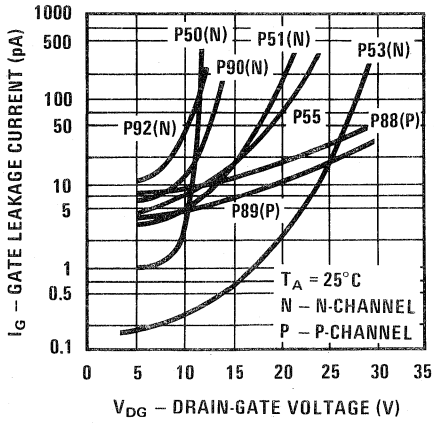


Dual FET Gate Leakage Current vs Drain-Gate Voltage

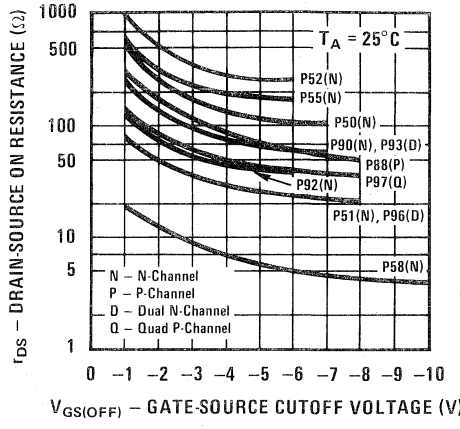


FET Process Comparison Curves (Continued)

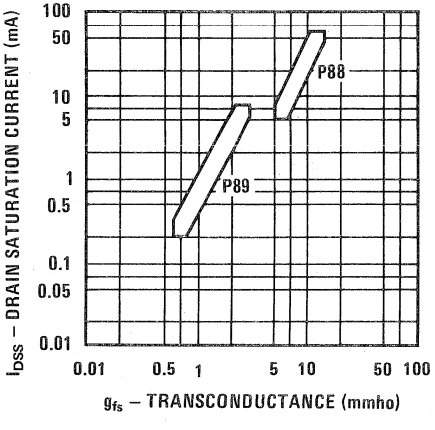
Single FET Gate Leakage Current vs Drain-Gate Voltage



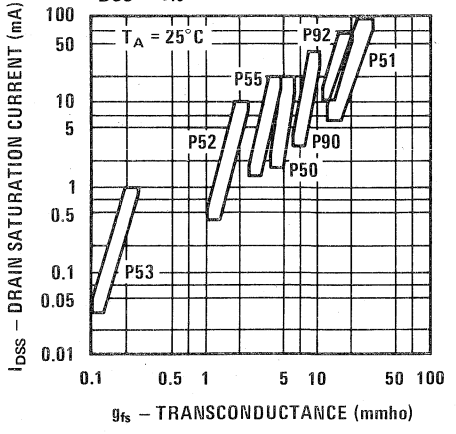
ON Resistance vs Cutoff Voltage



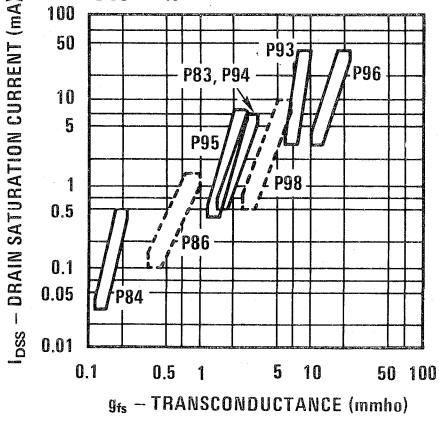
Single P-Channel FET Process Distribution
I_{DSS} vs g_{fs}



Single N-Channel FET Process Distribution
I_{DSS} vs g_{fs}



Monolithic Dual FET Process Distribution
I_{DSS} vs g_{fs}



N-Channel FETs

SWITCHES/CHOPPERS

Type No.	Case Style	BV_{GSS} BV_{GDO} (V) Min	@ I_G (μA)	I_{GSS} *I_{DGO} (nA) Max	@ V_{DG} (V)	$I_{D(off)}$ (nA) Max	@ V_{DS} (V)	V_{GS} (V)	V_p (V) Min	Max	@ V_{DS} (V)	I_D (nA)	I_{DSS} (mA) Min	Max	@ V_{DS} (V)	$r_{ds(on)}$ (Ω) Max	@ I_D (mA)	C_{iss} (pF) Max	@ V_{DS} (V)	V_{GS} (V)	C_{rss} (pF) Max	@ V_{DS} (V)	V_{GS} (V)	t_{on} (ns) Max	t_{off} (ns) Max	Process No.	Pkg. No.
2N3824	TO-72	50	1	0.1	30	0.1	15	−8		8	15	.1				250		6	15	0	3	0	−8			55	25
2N3966	TO-72	30	1	1	20	0.1	10	−7	4	6	10	10	2		20	220		6	20	0	1.5	0	−7			50	25
2N3970	TO-18	40	1	0.25*	20	0.25	20	−12	4	10	20	1	50	150	20	30	1	25	20	0	6	0	−12	20	30	51	02
2N3971	TO-18	40	1	0.25*	20	0.25	20	12	2	5	20	1	25	75	20	60	1	25	20	0	6	0	−12	30	60	51	02
2N3972	TO-18	40	1	0.25*	20	0.25	20	−12	0.5	3	20	1	5	30	20	100	1	25	20	0	6	0	−12	80	100	51	02
•2N4091	TO-18	40	1	0.2*	20	0.2	20	−12	5	10	20	1	30		20	30	1	16	20	0	5	0	−20	25	40	51	02
•2N4092	TO-18	40	1	0.2*	20	0.2	20	−8	2	7	20	1	15		20	50	1	16	20	0	5	0	−20	35	60	51	02
•2N4093	TO-18	40	1	0.2*	20	0.2	20	−6	1	5	20	1	8		20	80	1	16	20	0	5	0	−20	60	80	51	02
2N4391	TO-18	40	1	0.1	20	0.1	20	−12	4	10	20	1	50	150	20	30	1	14	20	0	3.5	0	−12	20	35	51	02
2N4392	TO-18	40	1	0.1	20	0.1	20	−7	2	5	20	1	25	75	20	60	1	14	20	0	3.5	0	−7	20	55	51	02
2N4393	TO-18	40	1	0.1	20	0.1	20	−5	0.5	3	20	1	5	30	20	100	1	14	20	0	3.5	0	−5	20	80	51	02
•2N4856	TO-18	40	1	0.25	20	0.25	15	−10	4	10	15	.5	50		15	25		18	0	−10	8	0	−10	9	25	51	02
2N4856A	TO-18	40	1	0.25	20	0.25	15	−10	4	10	15	.5	50		15	25		10	0	−10	4	0	−10	8	20	51	02
•2N4857	TO-18	40	1	0.25	20	0.25	15	−10	2	6	15	.5	20	100	15	40		18	0	−10	8	0	−10	10	50	51	02
2N4857A	TO-18	40	1	0.25	20	0.25	15	−10	2	6	15	.5	20	100	15	40		10	0	−10	3.5	0	−10	10	40	51	02
•2N4858	TO-18	40	1	0.25	20	0.25	15	−10	0.8	4	15	.5	8	80	15	60		18	0	−10	8	0	−10	20	100	51	02
2N4858A	TO-18	40	1	0.25	20	0.25	15	−10	0.8	4	15	.5	8	80	15	60		10	0	−10	3.5	0	−10	16	80	51	02
•2N4859	TO-18	30	1	0.25	15	0.25	15	−10	4	10	15	.5	50		15	25		18	0	−10	8	0	−10	9	25	51	02
2N4859A	TO-18	30	1	0.25	15	0.25	15	−10	4	10	15	.5	50		15	25		10	0	−10	4	0	−10	8	20	51	02
•2N4860	TO-18	30	1	0.25	15	0.25	15	−10	2	6	15	.5	20	100	15	40		18	0	−10	8	0	−10	10	50	51	02
2N4860A	TO-18	30	1	0.25	15	0.25	15	−10	2	6	15	.5	20	100	15	40		10	0	−10	3.5	0	−10	10	40	51	02
•2N4861	TO-18	30	1	0.25	15	0.25	15	−10	0.8	4	15	.5	8	80	15	60		18	0	−10	8	0	−10	20	100	51	02
2N4861A	TO-18	30	1	0.25	15	0.25	15	−10	0.8	4	15	.5	8	80	15	60		10	0	−10	3.5	0	−10	16	80	51	02
2N5432	TO-52	25	1	0.2	15	0.2	5	−10	4	10	5	3	150		15	5	10	30	0	−10	15	0	−10	5	36	58	07
2N5433	TO-52	25	1	0.2	15	0.2	5	−10	3	9	5	3	100		15	7	10	30	0	−10	15	0	−10	5	36	58	07
2N5434	TO-52	25	1	0.2	15	0.2	5	−10	1	4	5	3	30		15	10	10	30	0	−10	15	0	−10	5	36	58	07
2N5555	TO-92	25	10	1	15	10	12	−10		(10)			15		15	150		5	15	0	1.2	0	−10	10	25	50	72

• **Note.** JAN qualified per applicable MIL-S-19500 specification.

Selection Guide

N-Channel FETs

SWITCHES/CHOPPERS (Continued)

Type No.	Case Style	BV_{GSS} BV_{GDO} (V) @ I_G (μA) Min	I_{GSS} *I_{DGO} (nA) @ V_{DG} (V) Max	$I_{D(off)}$ (nA) @ V_{DG} (V) Max	V_{GS} (V)	V_p (V) Min	Max	@ V_{DS} (V)	I_D (nA)	I_{DSS} (mA) Min	Max	@ V_{DS} (V)	$r_{ds(on)}$ (Ω) @ I_D (mA) Max	C_{iss} (pF) @ V_{DS} (V) Max	V_{GS} (V)	C_{rss} (pF) @ V_{DS} (V) Max	V_{GS} (V)	t_{on} (ns) Max	t_{off} (ns) Max	Process No.	Pkg. No.
2N5638	TO-92	30 10	1 15	1 15	−12		(12)			50		20	30 1	10 0	−12	4 0	−12			51	72
2N5639	TO-92	30 10	1 15	1 15	−8		(8)			25		20	60 1	10 0	−12	4 0	−8			51	72
2N5640	TO-92	30 10	1 15	1 15	−6		(6)			5		20	100 1	10 0	−12	4 0	−6			51	72
2N5653	TO-92	30 10	1 15	1 15	−12		(12)			40		20	50 1	10 0	−12	3.5 0	−12	9	15	51	72
2N5654	TO-92	25 10	1 15	10 15	−8		(8)			15		20	100 1	10 0	−12	3.5 0	−8	14	30	51	72
J108	TO-92	25 1	3 15	3 5	−10	3	10	5	1000	80		15	8 10	t30 0	−10	t15 0	−10	t5	t36	58	72
J109	TO-92	25 1	3 15	3 5	−10	2	6	5	1000	40		15	12 10	t30 0	−10	t15 0	−10	t5	t36	58	72
J110	TO-92	25 1	3 15	3 5	−10	.5	4	5	1000	10		15	18 10	t30 0	−10	t15 0	−10	t5	t36	58	72
J111	TO-92	35 1	1 15	1 5	−10	3	10	5	1000	20		15	30 1	t10 0	−10	t5 0	−10	t13	t35	51	72
J112	TO-92	35 1	1 15	1 5	−10	1	5	5	1000	5		15	50 1	t10 0	−10	t5 0	−10	t13	t35	51	72
J113	TO-92	35 1	1 15	1 5	−10	.5	3	5	1000	2		15	100 1	t10 0	−10	t5 0	−10	t13	t35	51	72
J114	TO-92	25 1	1 15	1 5	−10	3	10	5	1000	15		15	150 1	t4 0	−10	t2 0	−10	t6	t20	90	72
PN4091	TO-92	40 1	1* 20	1 20	−12	5	10	20	1	30		20	30	16 20	0	5 20	0	25	40	51	72
PN4092	TO-92	40 1	1* 20	1 20	−8	2	7	20	1	15		20	50	16 20	0	5 20	0	35	60	51	72
PN4093	TO-92	40 1	1* 20	1 20	−6	1	5	20	1	8		20	80	16 20	0	5 20	0	60	80	51	72
PN4391	TO-92	40 1	1 20	1 20	−12	4	10	20	1	50	150	20	30	14 20	0	3.5 0	−12	20	35	51	72
PN4392	TO-92	40 1	1 20	1 20	−7	2	5	20	1	25	75	20	60	14 20	0	3.5 0	−7	40	80	51	72
PN4393	TO-92	40 1	1 20	1 20	−5	0.5	3	20	1	5	30	20	100	14 20	0	3.5 0	−5	55	130	51	72
PN4856	TO-92	40 1	1 20	1 15	−10	4	10	15	.5	50		15	25	18 0	−10	8 0	−10	9	25	51	72
PN4857	TO-92	40 1	1 20	1 15	−10	2	6	15	.5	20	100	15	40	18 0	−10	8 0	−10	10	50	51	72
PN4858	TO-92	40 1	1 20	1 15	−10	0.8	4	15	.5	8	80	15	60	18 0	−10	8 0	−10	20	100	51	72
PN4859	TO-92	30 1	1 15	1 15	−10	4	10	15	.5	50		15	25	18 0	−10	8 0	−10	9	25	51	72
PN4860	TO-92	30 1	1 15	1 15	−10	2	6	15	.5	20	100	15	40	18 0	−10	8 0	−10	10	50	51	72
PN4861	TO-92	30 1	1 15	1 15	−10	0.8	4	15	.5	8	80	15	60	18 0	−10	8 0	−10	20	100	51	72
TIS73	TO-92	30 1	2 15	2 15	−10	4	10	15	4	50		15	25	18 0	−10	8 0	−10	9	25	51	77
TIS74	TO-92	30 1	2 15	2 15	−10	2	6	15	4	20	100	15	40	18 0	−10	8 0	−10	10	50	51	77
TIS75	TO-92	30 1	2 15	2 15	−10	0.8	4	15	4	8	80	15	60	18 0	−10	8 0	−10	20	100	51	77
U1897E	TO-92	40 1	0.2* 20			5	10	20	1	30		20	30 1	16 20	0	5 0	−20	25	40	51	72
U1898E	TO-92	40 1	0.2* 20			2	7	20	1	15		20	50 1	16 20	0	5 0	−20	35	60	51	72
U1899E	TO-92	40 1	0.2* 20			1	5	20	1	8		20	80 1	16 20	0	5 0	−20	60	80	51	72

N-Channel FETs

RF, VHF, UHF AMPLIFIERS

Type No.	Case Style	BV_{GSS} BV_{GDO} (V) @ I_G (μA) Min	I_{GSS} I_{DGO} (pA) @ V_{DG} (V) Max	V_P (V) @ V_{DS} (V) Min	V_P (V) @ V_{DS} (V) Max	I_D (nA)	I_{DSS} (mA) @ V_{DS} (V) Min	I_{DSS} (mA) @ V_{DS} (V) Max	$\lvert Y_{fs}\rvert$ (mmho) @ Freq (MHz) Min	$\lvert Y_{os}\rvert$ (μmho) @ f (MHz) Max	C_{iss} (pF) @ V_{DS} (V) Max	V_{GS} (V)	C_{rss} (pF) @ V_{DS} (V) Max	V_{GS} (V)	NF (dB) @ R_G = 1k Freq (MHz) Max	Process No.	Pkg. No.
2N3819	TO-92	25 1	2 15		8	15 2	2	20	15 1.6 100		8	15 0	4	15 0		50	74
2N3823	TO-72	30 1	0.5 20		8	15 .5	4	20	15 3.2 200	200 200	6	15 0	2	15 0	2.5 100	50	25
2N4223	TO-72	30 10	0.25 20	0.1	8	15 .25	3	18	15 2.7 200	200 200	6	15 0	2	15 0	5 200	50	25
2N4224	TO-72	30 10	0.5 20	0.1	8	15 .5	2	20	15 1.7 200	200 200	6	15 0	2	15 0		50	25
2N4416	TO-72	30 1	0.1 20		6	15 1	5	15	15 4 400	100 400	4	15 0	0.8	15 0	4 400	50	25
•2N4416A	TO-72	35 1	0.1 20	2.5	6	15 1	5	15	15 4 400	100 400	4	15 0	0.8	15 0	4 400	50	25
2N5078	TO-72	30 1	0.25 20	0.5	8	15	4	25	15 4 200	150 200	6	15 0	2	15 0	3 200	50	25
2N5245	TO-92	30 1	1 20	1	6	15 10	5	15	15 4 400	100 400	4.5	15 0	1	15 0	4 400	90	77
2N5246	TO-92	30 1	1 20	0.5	4	15 10	1.5	7	15 2.5 400	100 400	4.5	15 0	1	15 0		90	77
2N5247	TO-92	30 1	1 20	1.5	8	15 10	8	24	15 4 400	150 400	4.5	15 0	1	15 0		90	77
2N5248	TO-92	30 1	5 20	1	8	15 10	4	20	15 3 200	200 200	6	15 0	2	15 0		50	74
2N5397	TO-72	25 1	0.1 15	1	6	10 1	10	30	10 5.5 450	200 450	5	10 10m	1.2	10 10m	3.5 450	90	25
2N5398	TO-72	25 1	0.1 15	1	6	10 1	5	40	10 5.0 450	400 450	5.5	10 0	1.3	10 0	3.2 450	90	25
2N5484	TO-92	25 1	1 20	0.3	3	15 10	1	5	15 2.5 100	75 100	5	15 0	1	15 0	3 100	50	72
2N5485	TO-92	25 1	1 20	1	4	15 10	4	10	15 3 400	100 400	5	15 0	1	15 0	4 400	50	72
2N5486	TO-92	25 1	1 20	2	6	15 10	8	20	15 3.5 400	100 400	5	15 0	1	15 0	4 400	50	72
2N5668	TO-92	25 10	2 15	0.2	4	15 10	1	5	15 1 100	50 100	7	15 0	3	15 0	2.5 100	50	72
2N5669	TO-92	25 10	2 15	1	6	15 10	4	10	15 1.6 100	100 100	7	15 0	3	15 0	2.5 100	50	72
2N5670	TO-92	25 10	2 15	2	8	15 10	8	20	15 2.5 100	150 100	7	15 0	3	15 0	2.5 100	50	72
2N5949	TO-92	30 1	1 15	3	7	15 100	12	18	15 3.0 100	75 100	6	15 0	2	15 0	5 100	50	77
2N5950	TO-92	30 1	1 15	2.5	6	15 100	10	15	15 3.0 100	75 100	6	15 0	2	15 0	5 100	50	77
2N5951	TO-92	30 1	1 15	2	5	15 100	7	13	15 3.0 100	75 100	6	15 0	2	15 0	5 100	50	77
2N5952	TO-92	30 1	1 15	1.3	3.5	15 100	4	8	15 1.0 100	75 100	6	15 0	2	15 0	5 100	50	77
2N5953	TO-92	30 1	1 15	.8	3	15 100	2.5	5	15 1.0 100	50 100	6	15 0	2	15 0	5 100	50	77
J300	TO-92	25 1	0.5 15	1	6	10 1	6	30	10 4.5 .001	200 .001	5.5	10 5m	1.7	10 5m	t2 100	90	72
J304	TO-92	30 1	0.1 20	2	6	15 1	5	15	15 t4.2 400	t80 100	t3	15 0	t.8	15 0	t4 400	50	72
J305	TO-92	30 1	0.1 20	.5	3	15 1	1	8	15 t3.0 400	t80 100	t3	15 0	t.8	15 0	t4 400	50	72
J308	TO-92	25 1	1 15	1	6.5	10 1	12	60	10 8 .001	200 .001	7.5	0 –10	2.5	0 –10	t1.5 100	92	72
J309	TO-92	25 1	1 15	1	4.0	10 1	12	30	10 10 .001	200 .001	7.5	0 –10	2.5	0 –10	t1.5 100	92	72
J310	TO-92	25 1	1 15	2	6.5	10 1	24	60	10 8 .001	200 .001	7.5	0 –10	2.5	0 –10	t1.5 100	92	72

• **Note.** JAN qualified per applicable MIL-S-19500 specification.

N-Channel FETs

RF, VHF, UHF AMPLIFIERS (Continued)

Type No.	Case Style	BV_{GSS} BV_{GDO} (V) @ I_G Min	(μA)	I_{GSS} I_{DGO} (pA) @ V_{DG} Max	(V)	V_p (V) Min	Max	@ V_{DS} (V)	I_D (nA)	I_{DSS} (mA) Min	Max	@ V_{DS} (V)	$R_e Y_{fs}$ (mMho) @ Freq Min	(MHz)	$R_e(Y_{os})$ (μMho) @ f Max	(MHz)	C_{iss} (pF) @ V_{DS} Max	(V)	V_{GS} (V)	C_{rss} (pF) @ V_{DS} Max	(V)	V_{GS} (V)	NF (dB) @ R_G = 1k Max	Freq (MHz)	Process No.	Pkg. No.
MPF102	TO-92	25	1	2	15		8	15	2	2	20	15	1.6	100	100	200	7	15	0	3	15	0			50	72
MPF106	TO-92	25	1	1	20	0.5	4	15	.5	4	10	15	2.5	0.001			5	15	0	2	15	0	4	400	50	72
MPF107	TO-92	25	1	1	20	2	6	15	.5	8	20	15	4	0.001			5	15	0	1.2	15	0	4	400	50	72
MPF108	TO-92	25	10	1	15	0.5	8	15	10μ	1.5	24	15	1.6	100	200	100	6.5	15	0	2.5	15	0	3	100	50	72
PN4223	TO-92	30	1	0.25	20	0.1	8	15	1	3	18	15	2.7	200	200	200	6	15	0	2	15	0	5	200	50	72
PN4224	TO-92	30	1	0.25	20	0.1	8	15	5	2	20	15	1.7	200	200	200	6	15	0	2	15	0			50	72
PN4416	TO-92	30	1	0.1	20		6	15	1	5	15	15	4	400	100	400	4	15	0	0.8	15	0	4	400	50	72
U308	TO-52	25	1	0.15	15	1	6	10	1	12	60	10	10	0.001	150	100	5	0	10m	2.5	0	10mA	t3	450	92	07
U309	TO-52	25	1	0.15	15	1	4	10	1	12	30	10	10	0.001	150	100	5	0	10m	2.5	0	10mA	t3	450	92	07
U310	TO-52	25	1	0.15	15	2.5	6	10	1	24	60	10	10	0.001	150	100	5	10	10m	2.5	10	10mA	t3	450	92	07
U312	TO-52	25	1	0.1	15	1	6	10	1	10	30	10	6	0.001			3.8	10	10m	1.2	10	10mA	t3.5	450	90	07
U320	TO-39	20	1	3	15	2	10	5	1m	100	500	15	75	0.001			30	0	10	15	0	10	t2.5	30	58	09
U321	TO-39	25	1	3	15	1	4	5	1m	80	250	15	75	0.001			30	0	10	15	0	10	t2.5	30	58	09
U322	TO-39	25	1	3	15	3	10	5	1m	200	700	15	75	0.001			30	0	10	15	0	10	t2.5	30	58	09

N-Channel FETs

LOW FREQUENCY—LOW NOISE AMPLIFIERS

Type No.	Case Style	BV_{GSS} (V) @ I_G Min	(μA)	I_{GSS} (nA) @ V_{DG} Max	(V)	$V_{GS(OFF)}$ (V) Min	Max	@ V_{DS} (V)	I_D (nA)	I_{DSS} (mA) Min	Max	@ V_{DS} (V)	g_{fs} ($Re Y_{fs}$) (mmho) Min	Max	V_{DS} (V)	f (MHz)	G_{oss} (μmho) Max	V_{DS} (V)	C_{iss} (pF) @ V_{DS} Max	(V)	V_{GS} (V)	C_{rss} (pF) @ V_{DS} Max	(V)	$\overline{e_n}$ nV/$\sqrt{Hz}$ @ Max	f (Hz)	Process No.	Pkg. No.
2N4393	TO-18	40	1.0	0.1	20	0.5	3.0	20	1.0	5.0	30	20	t12		20	0.001			14	20	0	3.5	5.0(GS)	t8.0	10	51	02
2N5556	TO-72	30	10	0.1	15	0.2	4.0	15	1.0	0.5	2.5	15	1.5	6.5	15	0.001	20	15	6.0	15	0	3.0	15	35	10	50	25
2N5557	TO-72	30	10	0.1	15	0.8	5.0	15	1.0	2.0	5.0	15	1.5	6.5	15	0.001	20	15	6.0	15	0	3.0	15	35	10	50	25
2N5558	TO-72	30	10	0.1	15	1.5	6.0	15	1.0	4.0	10	15	1.5	6.5	15	0.001	20	15	6.0	15	0	3.0	15	35	10	50	25
NF5101	TO-72	40	1	0.2	15	0.5	1.1	15	1.0	1.0	12	15	3.5		15	0.001	25	15	t12	15	0	t4	15	3.5	1k	51	25
NF5102	TO-72	40	1	0.2	15	0.7	1.6	15	1.0	4.0	20	15	7.5		15	0.001	25	15	t12	15	0	t4	15	3.5	1k	51	25
NF5103	TO-72	40	1	0.2	15	1.2	2.7	15	1.0	10	40	15	7.5		15	0.001	25	15	t12	15	0	t4	15	3.5	1k	51	25
PF5101	TO-92	40	1	0.2	15	0.5	1.1	15	1.0	1.0	12	15	3.5		15	0.001	25	15	t12	15	0	t4	15	3.5	1k	51	72
PF5102	TO-92	40	1	0.2	15	0.7	1.6	15	1.0	4.0	20	15	7.5		15	0.001	25	15	t12	15	0	t4	15	3.5	1k	51	72
PF5103	TO-92	40	1	0.2	15	1.2	2.7	15	1.0	10	40	15	7.5		15	0.001	25	15	t12	15	0	t4	15	3.5	1k	51	72
PN4393	TO-106	40	1.0	0.1	20	0.5	3.0	20	1.0	5.0	30	20	t12		20	0.001			14	20	0	3.5	5.0(GS)	t8.0	10	51	72

N-Channel FETs

ULTRA LOW INPUT CURRENT AMPS

Transistor Type	Case Style	BV_{GSS} / BV_{GDO} (V) Min @ I_G (μA)	I_{GSS} / I_{DGO} (pA) Max @ V_{DG} (V)	V_p (V) Min	V_p (V) Max	V_p @ V_{DS} (V)	I_D (nA)	I_{DSS} (μA) Min	I_{DSS} (μA) Max	I_{DSS} @ V_{DS} (V)	G_{fs} (μmho) Min	G_{fs} (μmho) Max	G_{fs} @ V_{DS} (V)	G_{oss} (μmho) Max	G_{oss} @ V_{DS} (V)	C_{iss} (pF) Max	C_{iss} @ V_{DS} (V)	V_{GS} (V)	C_{rss} (pF) Max	C_{rss} @ V_{DS} (V)	V_{GS} (V)	e_n $\left(\frac{NV}{\sqrt{Hz}}\right)$ Max	e_n @ f (Hz)	Process No.	Pkg. No.
2N4117	TO-72	40	1	10	20	0.6	1.8	10	1	30	90	10	20	210	10	3	10	3	10	0	1.5	10	0			53	25
2N4117A	TO-72	40	1	1	20	0.6	1.8	10	1	30	90	10	70	210	10	3	10	3	10	0	1.5	10	0			53	25
2N4118	TO-72	40	1	10	20	1	3	10	1	80	240	10	80	250	10	5	10	3	10	0	1.5	10	0			53	25
2N4118A	TO-72	40	1	1	20	1	3	10	1	80	240	10	80	250	10	5	10	3	10	0	1.5	10	0			53	25
2N4119	TO-72	40	1	10	20	2	6	10	1	200	600	10	100	330	10	10	10	3	10	0	1.5	10	0			53	25
2N4119A	TO-72	40	1	1	20	2	6	10	1	200	600	10	100	330	10	10	10	3	10	0	1.5	10	0			53	25

N-Channel FETs

GENERAL PURPOSE AMPS

Transistor Type	Case Style	BV_{GSS} / *BV_{GDO} (V) Min @ I_G (μA)	I_{GSS} / I_{DGO} (nA) Max @ V_{DG} (V)	V_p (V) Min	V_p (V) Max	V_p @ V_{DS} (V)	I_D (nA)	I_{DSS} (mA) Min	I_{DSS} (mA) Max	I_{DSS} @ VDS (V)	G_{fs} (mmho) Min	G_{fs} (mmho) Max	G_{fs} @ V_{DS} (V)	G_{oss} (μmho) Max	G_{oss} @ V_{DS} (V)	C_{iss} (pF) Max	C_{iss} @ V_{DS} (V)	V_{GS} (V)	C_{rss} (pF) Max	C_{rss} @ V_{DS} (V)	V_{GS} (V)	e_n $\left(\frac{NV}{\sqrt{Hz}}\right)$ Max	e_n @ Freq (Hz)	Process No.	Pkg. No.
2N3069	TO-18	*50	1	1	30		9.5	30	1000	2	10	30	1	2.5	30	80	30	15	0	−12	1.5	30	0	125	1000	52	02
2N3070	TO-18	*50	1	1	30		4.5	30	1000	0.5	2.5	30	0.75	2.5	30	30	30	15	0	−8	1.5	30	0	125	1000	52	02
2N3368	TO-18	*40	1	5	30		11.5	20	1000	2	12	30	1	4	30	80	30	20	8	0	3	30	0			52	02
2N3369	TO-18	*40	1	5	30		6.5	20	1000	0.5	2.5	30	0.6	2.5	30	30	30	20	8	0	3	30	0			52	02
2N3370	TO-18	*40	1	5	30		3.2	20	1000	0.1	0.6	30	0.3	2.5	30	15	30	20	8	0	3	30	0			52	02
2N3436	TO-18	*50	1	0.5	30		9.8	20	1000	3	15	20	2.5	10	20	35	30	18	0	−10	6	30	0	100	1000	55	02
2N3437	TO-18	*50	1	0.5	30		4.8	20	1000	0.8	4	20	1.5	6	20	20	30	18	0	−6	6	30	0	100	1000	55	02
2N3438	TO-18	*50	1	0.5	30		2.3	20	1000	0.2	1	20	0.8	4.5	20	5	30	18	0	−4	6	30	0	100	1000	55	02
2N3458	TO-18	*50	1	0.25	30		7.8	20	1000	3	15	20	2.5	10	20	35	30	18	0	−10	5	30	0	225	20	52	02
2N3459	TO-18	*50	1	0.25	30		3.4	20	1000	0.8	4	20	1.5	6	20	20	30	18	0	−6	5	30	0	155	20	52	02
2N3460	TO-18	*50	1	0.25	30		1.8	20	1000	0.2	1	20	0.8	4.5	20	5	30	18	0	−4	5	30	0	155	20	52	02
2N3684	TO-72	50	1	0.1	30	2	5	20	1	2.5	7.5	20	2	3	20	50	20	4	20	0	1.2	20	0	150	100	52	25
2N3685	TO-72	50	1	0.1	30	1	3.5	20	1	1	3	20	1.5	2.5	20	25	20	4	20	0	1.2	20	0	150	100	52	25
2N3686	TO-72	50	1	0.1	30	0.6	2	20	1	0.4	1.2	20	1	2	20	10	20	4	20	0	1.2	20	0	150	100	52	25
2N3687	TO-72	50	1	0.1	30	0.3	1.2	20	1	0.1	0.5	20	0.5	1.5	20	5	20	4	20	0	1.2	20	0	150	100	52	25
2N3821	TO-72	50	1	0.1	30		4	15	.5	0.5	2.5	15	1.5	4.5	15	10	15	6	15	0	3	15	0	200	10	55	25
2N3822	TO-72	50	1	0.1	30		6	15	.5	2	10	15	3	6.5	15	20	15	6	15	0	3	15	0	200	10	55	25
2N3967	TO-72	30	1	0.1	20	2	5	20	1	2.5	10	20	2.5		20	35	20¶	5	20	¶	1.3	20	♦	84	100	50	25
2N3967A	TO-72	30	1	0.1	20	2	5	20	1	2.5	10	20	2.5		20	35	20¶	5	20	¶	1.3	20	♦	160	10	50	25
2N3968	TO-72	30	1	0.1	20		3	20	1	1	5	20	2		20	15	20**	5	20	**	1.3	20	†	84	100	50	25
2N3968A	TO-72	30	1	0.1	20		3	20	1	1	5	20	2		20	15	20**	5	20	**	1.3	20	†	160	10	50	25
2N3969	TO-72	30	1	0.1	20		1.7	20	1	0.4	2	20	1.3		20	5	20††	5	20	††	1.3	20	¶	84	100	50	25
2N3969A	TO-72	30	1	0.1	20		1.7	20	1	0.4	2	20	1.3		20	5	20††	5	20	††	1.3	20	¶	160	10	50	25

♦I_D = 1 mA †I_D = 500μA ¶ I_D = 250μA δ I_D = 100μA **I_D = 100μA ††I_D = 40μA

N-Channel FETs

GENERAL PURPOSE AMPS (Continued)

Transistor Type	Case Style	BV_{GSS} *BV_{GDO} (V) @ I_G (μA) Min	I_{GSS} I_{DGO} (nA) @ V_{DG} (V) Max	V_p (V) @ V_{DS} (V) Min	Max	I_D (nA)	I_{DSS} (mA) @ VDS (V) Min	Max	G_{fs} (mmho) @ V_{DS} (V) Min	Max	G_{oss} (μmho) @ V_{DS} (V) Max	C_{iss} (pF) @ V_{DS} (V) Max	V_{GS} (V)	C_{rss} (pF) @ V_{DS} (V) Max	V_{GS} (V)	e_n $\left(\frac{NV}{\sqrt{Hz}}\right)$ @ Freq (Hz) Max		Process No.	Pkg. No.
2N4220	TO-72	30 10	0.1 15		4	15 .1	0.5	3 15	1	4 15	10 15	6	15	0	2	15	0			55	25
2N4220A	TO-72	30 10	0.1 15		4	15 .1	0.5	3 15	1	4 15	10 15	6	15	0	2	15	0	115	100	55	25
2N4221	TO-72	30 10	0.1 15		6	15 .1	2	6 15	2	5 15	20 15	6	15	0	2	15	0			55	25
2N4221A	TO-72	30 10	0.1 15		6	15 .1	2	6 15	2	5 15	20 15	6	15	0	2	15	0	115	100	55	25
2N4222	TO-72	30 10	0.1 15		8	15 .1	5	15 15	2.5	6 15	40 15	6	15	0	2	15	0			55	25
2N4222A	TO-72	30 10	0.1 15		8	15 .1	5	15 15	2.5	6 15	40 15	6	15	0	2	15	0	115	100	55	25
2N4338	TO-18	50 1	0.1 30	0.3	1	15 100	0.2	0.6 15	0.6	1.8 15	5 15	7	15	0	3	15	0	68	1000	52	02
2N4339	TO-18	50 1	0.1 30	0.6	1.8	15 100	0.5	1.5 15	0.8	2.4 15	15 15	7	15	0	3	15	0	68	1000	52	02
2N4340	TO-18	50 1	0.1 30	1	3	15 100	1.2	3.6 15	1.3	3 15	30 15	7	15	0	3	15	0	68	1000	52	02
2N4341	TO-18	50 1	0.1 30	2	6	15 100	3	9 15	2	4 15	60 15	7	15	0	3	15	0	68	1000	55	02
2N5103	TO-72	25 10	0.1 15	0.5	4	15 1	1	8 15	2	8 15	100 15	5	15	0	1	15	0	100	10	50	25
2N5104	TO-72	25 1	0.1 15	0.5	4	15 1	2	6 15	3.5	7.5 15	100 15	5	15	0	1	15	0	50	10	50	25
2N5105	TO-72	25 1	0.1 15	0.5	4	15 1	5	15 15	5	10 15	100 15	5	15	0	1	15	0			50	25
2N5358	TO-72	40 1	0.1 20	0.5	3	15 100	0.5	1 15	1	3 15	10 15	6	15	0	2	15	0	115	100	55	25
2N5359	TO-72	40 1	0.1 20	0.8	4	15 100	0.6	1.6 15	1.2	3.6 15	10 15	6	15	0	2	15	0	115	100	55	25
2N5360	TO-72	40 1	0.1 20	0.8	4	15 100	0.5	2.5 15	1.4	4.2 15	20 15	6	15	0	2	15	0	115	100	55	25
2N5361	TO-72	40 1	0.1 20	1	6	15 100	2.5	5 15	1.5	4.5 15	20 15	6	15	0	2	15	0	115	100	55	25
2N5362	TO-72	40 1	0.1 20	2	7	15 100	4	8 15	2	5.5 15	40 15	6	15	0	2	15	0	115	100	55	25
2N5363	TO-72	40 1	0.1 20	2.5	8	15 100	7	14 15	2.5	6 15	40 15	6	15	0	2	15	0	115	100	55	25
2N5364	TO-72	40 1	0.1 20	2.5	8	15 100	9	18 15	2.7	6.5 15	60 15	6	15	0	2	15	0	115	100	55	25
2N5457	TO-92	25 1	1 15	0.5	6	15 10	1	5 15	2	5 15	50 15	7	15	0	3	15	0			55	72
2N5458	TO-92	25 1	1 15	1	7	15 10	2	9 15	1.5	5.5 15	50 15	7	15	0	3	15	0			55	72
2N5459	TO-92	25 1	1 15	2	8	15 10	4	16 15	2	6 15	50 15	7	15	0	3	15	0			55	72
2N5556	TO-72	30 1	0.1 15	0.2	4	15 1	0.5	2.5 15	1.5	6.5 15	20 15	6	15	0	3	15	0	35	10	50	25
2N5557	TO-72	30 1	0.1 15	0.8	5	15 1	2.0	5.0 15	1.5	6.5 15	20 15	6	15	0	3	15	0	35	10	50	25
2N5558	TO-72	30 1	0.1 15	1.5	6	15 1	4	10 15	1.5	6.5 15	20 15	6	15	0	3	15	0	35	10	50	25
J201	TO-92	40 1	0.1 20	0.3	1.5	20 10	0.2	1.0 20	0.5	20	t1 20	t5	20	0	t2	20	0	t10	1k	52	72
J202	TO-92	40 1	0.1 20	0.8	4.0	20 10	0.9	4.5 20	1.0	20	t3.5 20	t5	20	0	t2	20	0	t10	1k	52	72
J203	TO-92	40 1	0.1 20	2.0	10.0	20 10	4.0	20 20	1.5	20	t10 20	t5	20	0	t2	20	0	t10	1k	52	72
J210	TO-92	25 1	0.1 15	1	3	15 1	2	15 15	4.0	12.0 15	150 15	t5	15	0	t1.5	15	0	t10	1k	90	72
J211	TO-92	25 1	0.1 15	2.5	4.5	15 1	7	20 15	7.0	12.0 15	200 15	t5	15	0	t1.5	15	0	t10	1k	90	72
J212	TO-92	25 1	0.1 15	4	6	15 1	15	40 15	7.0	12.0 15	200 15	t5	15	0	t1.5	15	0	t10	1k	90	72
MPF103	TO-92	25 1	1 15		6	15 1	1	5 15	1	5 15	50 15	7	15	0	3	15	0			55	72
MPF104	TO-92	25 1	1 15		7	15 1	2	9 15	1.5	5.5 15	50 15	7	15	0	3	15	0			55	72
MPF105	TO-92	25 1	1 15		8	15 1	4	16 15	2	6 15	50 15	7	15	0	3	15	0			55	72
MPF109	TO-92	25 10	1 15	0.2	8	15 10	0.5	24 15	0.8	6 15	75 15	7	15	0	3	15	0	115	1000	55	72

N-Channel FETs

GENERAL PURPOSE AMPS (Continued)

Transistor Type	Case Style	BV_{GSS} / BV_{GDO} (V) Min	@ I_G (μA)	I_{GSS} / I_{DGO} (nA) Max	@ V_{DG} (V)	V_P (V) Min	Max	@ V_{DS} (V)	I_D (nA)	I_{DSS} (mA) Min	Max	@ VDS (V)	G_{fs} (mmho) Min	Max	@ V_{DS} (V)	G_{oss} (μmho) Max	@ V_{DS} (V)	C_{iss} (pF) Max	@ V_{DS} (V)	V_{GS} (V)	C_{rss} (pF) Max	@ V_{DS} (V)	V_{GS} (V)	e_n $\left(\frac{NV}{\sqrt{Hz}}\right)$ Max	@ Freq (Hz)	Process No.	Pkg. No.
MPF111	TO-92	20	10	100	10	0.5	10	10	1000	0.5	20	10	0.5		10	200	10										50	72
MPF112	TO-92	25	10	100	10	0.5	10	10	1000	1	25	10	1	7.5	10												55	72
PN3684	TO-92	50	1	1	30	2	5	20	1	2.5	7.5	20	2	3	20	50	20	4	20	0	1.2	20	0	150	20	52	72
PN3685	TO-92	50	1	1	30	1	3.5	20	1	1	3	20	1.5	2.5	20	25	20	4	20	0	1.2	20	0	150	20	52	72
PN3686	TO-92	50	1	1	30	0.6	2	20	1	0.4	1.2	20	1	2	20	10	20	4	20	0	1.2	20	0	150	20	52	72
PN3687	TO-92	50	1	1	30	0.3	1.2	20	1	0.1	0.5	20	0.5	1.5	20	5	20	4	20	0	1.2	20	0	150	20	52	72
PN4220	TO-92	30	10	1	15		4	15	1	0.5	3	15	1	4	15	10	15	6	15	0	2	15	0			55	72
PN4221	TO-92	30	10	1	15		6	15	1	2	6	15	2	5	15	20	15	6	15	0	2	15	0			55	72
PN4222	TO-92	30	10	1	15		8	15	1	5	15	15	2.5	6	15	40	15	6	15	0	2	15	0			55	72
PN4302	TO-92	30	1	1	10		4	20	10	0.5	5	20	1		20	50	20	6	20	0	3	20	0	100	1000	52	72
PN4303	TO-92	30	1	1	10		6	20	10	4	10	20	2		20	50	20	6	20	0	3	20	0	100	1000	52	72
PN4304	TO-92	30	1	1	10		10	20	10	0.5	15	20	1		20	50	20	6	20	0	3	20	0	125	1000	52	72
PN5163	TO-92	25	1	10	15	0.4	8	15	1000	1	40	15	2	9	15	200	15	12	15	0	3	15	0	50	1000	50	72
TIS58	TO-92	25	1	4	15	0.5	5	15	20	2.5	8	15	1.3	4	15			6	15	2 mA	3	15	2 mA			50	74
TIS59	TO-92	25	1	4	15	1	9	15	20	6	25	15	1.3		15			6	15	2 mA	3	15	2 mA			50	74

N-Channel FETs

GENERAL PURPOSE DUAL JFETs

Type No.	Case Style	OPERATING CONDITIONS FOR THESE CHARACTERISTICS: OP. CHAR. V_{DG} (V)	I_D (μA)	$\lvert V_{GS1-2}\rvert$ V_{OS} (mV) Max	DRIFT (μV/°C) ΔV_{GS} Max	I_G (pA) Max	G_{fs} (μmhos) Min	Max	G_{oss} (μmho) Max	CMRR (dB) Min	V_{gs} (V) Min	Max	V_P (V) Min	Max	I_{DSS} (mA) Min	Max	G_{fs} (mmho) Min	Max	G_{oss} (μmho) Max	I_{GSS} (pA) @ V_{DG} Max	(V)	C_{iss} (pF) Max	C_{rss} (pF) Max	BV (V) Min	e_n (nV/√Hz) @ Max	f (Hz)	I_{DSS} Match %	G_{fs} Match %	G_{oss1-2} (μmho)	$I_{G1-}I_{G2}$ 125°C (nA)	Process No.	Pkg. No.
2N3921	TO-71	10	700	5.0	10	250	1500		20				−3.0		1.0	10	1.5	7.5	35	1000	30	18	6.0	50	100	1.0k		5.0				83	12
2N3922	TO-71	10	700	5.0	25	250	1500		20				−3.0		1.0	10	1.5	7.5	35	1000	30	18	6.0	50	100	1.0k		5.0				83	12
2N3934	TO-71	10	200	5.0	10	100	300		5.0				See 2N3954-6 as an improved replacement																				12
2N3935	TO-71	10	200	5.0	25	100	300		5.0				See 2N3954-6 as an improved replacement																				12
2N3954A	TO-71	20	200	5.0	5.0	50					0.5	4.0	1.0	4.5	0.5	5.0	1.0	3.0	35	100	30	4.0	1.2	50	150	100	5.0	3.0		10		83	12
2N3954	TO-71	20	200	5.0	10	50					0.5	4.0	1.0	4.5	0.5	5.0	1.0	3.0	35	100	30	4.0	1.2	50	150	100	5.0	3.0		10		83	12
2N3955A	TO-71	20	200	5.0	15	50					0.5	4.0	1.0	4.5	0.5	5.0	1.0	3.0	35	100	30	4.0	1.2	50	150	100	5.0	3.0		10		83	12
2N3955	TO-71	20	200	10	25	50					0.5	4.0	1.0	4.5	0.5	5.0	1.0	3.0	35	100	30	4.0	1.2	50	150	100	5.0	5.0		10		83	12
2N3956	TO-71	20	200	15	50	50					0.5	4.0	1.0	4.5	0.5	5.0	1.0	3.0	35	100	30	4.0	1.2	50	150	100	5.0	5.0		10		83	12
2N3957	TO-71	20	200	20	75	50					0.5	4.0	1.0	4.5	0.5	5.0	1.0	3.0	35	100	30	4.0	1.2	50	150	100	10	10		10		83	12
2N3958	TO-71	20	200	25	100	50					0.5	4.0	1.0	4.5	0.5	5.0	1.0	3.0	35	100	30	4.0	1.2	50	150	100	15	15		10		83	12
2N4082	TO-71	10	200	15	10	100	300		10				See 2N3954-6 as an improved replacement																				12
2N4083	TO-71	10	200	15	25	100	300		10				See 2N3954-6 as an improved replacement																				12
2N4084	TO-71	10	700	15	10	250	1500		20		0.5	4.0	3.0		1.0	10	1.5	7.5	35	1000	30	18	6.0	50	100	1.0k		5.0				83	12
2N4085	TO-71	10	700	15	25	250	1500		20				3.0		1.0	10	1.5	7.5	35	1000	30	18	6.0	50	100	1.0k		5.0				83	12

Selection Guide

GENERAL PURPOSE DUAL JFETs (Continued)

Type No.	Case Style	OPERATING CONDITIONS FOR THESE CHARACTERISTICS: OP. CHAR. V_{DG} (V)	OP. CHAR. I_D (μA)	$\lvert V_{GS1-2}\rvert$ V_{OS} (mV) Max	DRIFT (μV/°C) ΔV_{GS} Max	I_G (pA) Max	G_{fs} μmhos Min	G_{fs} μmhos Max	G_{oss} (μmho) Max	CMRR (dB) Min	V_{gs} (V) Min	V_{gs} (V) Max	V_p (V) Min	V_p (V) Max	I_{DSS} (mA) Min	I_{DSS} (mA) Max	G_{fs} (mmho) Min	G_{fs} (mmho) Max	G_{oss} (μmho) Max	I_{GSS} (pA) @ V_{DG} Max	I_{GSS} (pA) @ V_{DG} (V)	C_{iss} (pF) Max	C_{rss} (pF) Max	BV (V) Min	$\bar{e}_n$ (nV/$\sqrt{Hz}$) @ Max	f (Hz)	I_{DSS} Match %	G_{fs} Match %	G_{oss1-2} (μmho)	I_{G1}-I_{G2} 125°C (nA)	Process No.	Pkg. No.
2N5045	TO-71	15	200	5.0	67								0.5	4.5	0.5	8.0	1.5	6.0	25	250	30	8.0	4.0	50	200	10		5.0	1.0		83	12
2N5046	TO-71	15	200	10	133								0.5	4.5	0.5	8.0	1.5	6.0	25	250	30	8.0	4.0	50	200	10		10	2.0		83	12
2N5047	TO-71	15	200	15	200								0.5	4.5	0.5	8.0	1.5	6.0	25	250	30	8.0	4.0	50	200	10		20	3.0		83	12
2N5196	TO-71	20	200	5.0	5.0	15	700	1500	4.0		0.2	3.8	0.7	4.5	0.7	7.0	1.0	4.0	50	25	30	6.0	2.0	50	20	1.0k	5.0	3.0	1.0	5.0	83	12
2N5197	TO-71	20	200	5.0	10	15	700	1500	4.0		0.2	3.8	0.7	4.5	0.7	7.0	1.0	4.0	50	25	30	6.0	2.0	50	20	1.0k	5.0	3.0	1.0	5.0	83	12
2N5198	TO-71	20	200	10	20	15	700	1500	4.0		0.2	3.8	0.7	4.5	0.7	7.0	1.0	4.0	50	25	30	6.0	2.0	50	20	1.0k	5.0	5.0	1.0	5.0	83	12
2N5199	TO-71	20	200	15	40	15	700	1500	4.0		0.2	3.8	0.7	4.5	0.7	7.0	1.0	4.0	50	25	30	6.0	2.0	50	20	1.0k	5.0	5.0	1.0	5.0	83	12
2N5452	TO-71	20	200	5.0	5.0				1.0		0.2	4.2	1.0	4.5	0.5	5.0	1.0	3.0	3.0	100	30	4.0	1.2	50	20	1.0k	5.0	3.0	0.25		83	12
2N5453	TO-71	20	200	10	10				1.0		0.2	4.2	1.0	4.5	0.5	5.0	1.0	3.0	3.0	100	30	4.0	1.2	50	20	1.0k	5.0	3.0	0.25		83	12
2N5454	TO-71	20	200	15	25				1.0		0.2	4.2	1.0	4.5	0.5	5.0	1.0	3.0	3.0	100	30	4.0	1.2	50	20	1.0k	5.0	5.0	0.25		83	12
2N5545	TO-71	15	200	5.0	10	50							0.5	4.5	0.5	8.0	1.5	6.0	25	100	30	6.0	2.0	50	180	10	5.0	3.0	1.0	5.0	83	12
2N5546	TO-71	15	200	10	20	50							0.5	4.5	0.5	8.0	1.5	6.0	25	100	30	6.0	2.0	50	200	10	10	5.0	2.0	5.0	83	12
2N5547	TO-71	15	200	15	40	50							0.5	4.5	0.5	8.0	1.5	6.0	25	100	30	6.0	2.0	50			10	10	3.0	5.0	83	12
2N5561	TO-71	PROCESS IN DEVELOPMENT																														12
2N5562	TO-71																															12
2N5563	TO-71																															12
J401	8-Pin Mini-DIP																														98	60
J402																															98	60
J403																															98	60
J404																															98	60
J405																															98	60
J406																															98	60
J410	8-Pin Mini-DIP	20	200	10	10	250	600	1200	5.0		0.3	4.0	0.5	3.5	0.5	6	1	4	20	250	20	4.5	1.2	40	50	100					98	60
J411		20	200	25	25	250	600	1200	5.0		0.3	4.0	0.5	3.5	0.5	6	1	4	20	250	20	4.5	1.2	40	50	100					98	60
J412		20	200	40	80	250	600	1200	5.0		0.3	4.0	0.5	3.5	0.5	6	1	4	20	250	20	4.5	1.2	40	50	100					98	60
NPD8301	8-Pin Mini-DIP	20	200	5	10	100	700	1200	5.0		0.3	4.0	0.5	3.5	0.5	6	1	4	20	100	20	4.5	1.2	40	50	100					83	67
NPD8302		20	200	10	15	100	700	1200	5.0		0.3	4.0	0.5	3.5	0.5	6	1	4	20	100	20	4.5	1.2	40	50	100					83	67
NPD8303		20	200	15	25	100	700	1200	5.0		0.3	4.0	0.5	3.5	0.5	6	1	4	20	100	20	4.5	1.2	40	50	100					83	67
NPD9801		PROCESS IN DEVELOPMENT																													98	67
NPD9802																															98	67
NPD9803																															98	67
U231	TO-71	20	200	5.0	10	50	600		10		0.3	4.0	See 2N3954 as an improved replacement																		83	12
U232	TO-71	20	200	10	25	50	600		10		0.3	4.0	See 2N3955 as an improved replacement																		83	12
U233	TO-71	20	200	15	50	50	600		10		0.3	4.0	See 2N3956 as an improved replacement																		83	12
U234	TO-71	20	200	20	75	50	600		10		0.3	4.0	See 2N3957 as an improved replacement																		83	12
U235	TO-71	20	200	25	100	50	600		10		0.3	4.0	See 2N3958 as an improved replacement																		83	12
U401	TO-71	PROCESS IN DEVELOPMENT																													98	12
U402	TO-71																														98	12
U403	TO-71																														98	12
U404	TO-71																														98	12
U405	TO-71																														98	12
U406	TO-71																														98	12

N-Channel FETs

LOW FREQUENCY—LOW NOISE DUAL JFETs

Type No.	Case Style	OPERATING CONDITIONS FOR THESE CHARACTERISTICS: OP. CHAR. V_{DG} (V)	OP. CHAR. I_D (μA)	$\lvert V_{GS1-2}\rvert$ V_{OS} (mV) Max	DRIFT (μV/°C) ΔV_{GS} Max	I_G (pA) Max	G_{fs} μmhos Min	G_{fs} μmhos Max	G_{oss} (μmho) Max	CMRR (dB) Min	V_{gs} (V) Min	V_{gs} (V) Max	V_p (V) Min	V_p (V) Max	I_{DSS} (mA) Min	I_{DSS} (mA) Max	G_{fs} (μmho) Min	G_{fs} (μmho) Max	G_{oss} (μmho) Max	I_{GSS} (pA) @ V_{DG} Max	I_{GSS} @ V_{DG} (V)	C_{iss} (pF) Max	C_{rss} (pF) Max	BV (V) Min	$\overline{e_n}$ (nV/√Hz) Max	@ f (Hz)	I_{DSS} Match %	G_{fs} Match %	G_{oss1-2} (μmho)	I_{G1-IG2} 125°C (nA)	Process No.	Pkg. No.
2N5515	TO-71	20	200	5.0	5.0	100	500	1000	1.0	100	0.2	3.8	0.7	4.0	0.5	7.5	1.0	4.0	10	250	30	+25	+5.0	40	30	10	5.0	3.0	0.1	10	95	12
2N5516	TO-71	20	200	5.0	10	100	500	1000	1.0	100	0.2	3.8	0.7	4.0	0.5	7.5	1.0	4.0	10	250	30	+25	+5.0	40	↓	10	5.0	3.0	0.1	10	95	12
2N5517	TO-71	20	200	10	20	100	500	1000	1.0	90	0.2	3.8	0.7	4.0	0.5	7.5	1.0	4.0	10	250	30	+25	+5.0	40	↓	10	5.0	5.0	0.1	10	95	12
2N5518	TO-71	20	200	15	40	100	500	1000	1.0		0.2	3.8	0.7	4.0	0.5	7.5	1.0	4.0	10	250	30	+25	+5.0	40	↓	10	5.0	5.0	0.1	10	95	12
2N5519	TO-71	20	200	15	80	100	500	1000	1.0		0.2	3.8	0.7	4.0	0.5	7.5	1.0	4.0	10	250	30	+25	+5.0	40	↓	10	10	10	0.1	10	95	12
2N5520	TO-71	20	200	5.0	5.0	100	500	1000	1.0	100	0.2	3.8	0.7	4.0	0.5	7.5	1.0	4.0	10	250	30	+25	+5.0	40	15	10	5.0	3.0	0.1	10	95	12
2N5521	TO-71	20	200	5.0	10	100	500	1000	1.0	100	0.2	3.8	0.7	4.0	0.5	7.5	1.0	4.0	10	250	30	+25	+5.0	40	↓	10	5.0	3.0	0.1	10	95	12
2N5522	TO-71	20	200	10	20	100	500	1000	1.0	90	0.2	3.8	0.7	4.0	0.5	7.5	1.0	4.0	10	250	30	+25	+5.0	40	↓	10	5.0	5.0	0.1	10	95	12
2N5523	TO-71	20	200	15	40	100	500	1000	1.0		0.2	3.8	0.7	4.0	0.5	7.5	1.0	4.0	10	250	30	+25	+5.0	40	↓	10	5.0	5.0	0.1	10	95	12
2N5524	TO-71	20	200	15	80	100	500	1000	1.0		0.2	3.8	0.7	4.0	0.5	7.5	1.0	4.0	10	250	30	+25	+5.0	40	↓	10	10	10	0.1	10	95	12
2N6483	TO-71	20	200	5.0	5.0	100	500	1500	1.0	100	0.2	3.8	0.7	4.0	0.5	7.5	1.0	4.0	10	200	30	20	3.5	50	10	10	5.0	3.0	0.1	10	95	12
2N6484	TO-71	20	200	10	10	100	500	1500	1.0	100	0.2	3.8	0.7	4.0	0.5	7.5	1.0	4.0	10	200	30	20	3.5	50	↓	10	5.0	3.0	0.1	10	95	12
2N6485	TO-71	20	200	15	25	100	500	1500	1.0	90	0.2	3.8	0.7	4.0	0.5	7.5	1.0	4.0	10	200	30	20	3.5	50	↓	10	5.0	5.0	0.1	10	95	12

N-Channel FETs

WIDE BAND—LOW NOISE DUAL JFETs

Type No.	Case Style	OPERATING CONDITIONS FOR THESE CHARACTERISTICS: OP. CHAR. V_{DG} (V)	OP. CHAR. I_D (μA)	$\lvert V_{GS1-2}\rvert$ V_{OS} (mV) Max	DRIFT (μV/°C) ΔV_{GS} Max	I_G (pA) Max	G_{fs} μmhos Min	G_{fs} μmhos Max	G_{oss} (μmho) Max	CMRR (dB) Min	V_{gs} (V) Min	V_{gs} (V) Max	V_p (V) Min	V_p (V) Max	I_{DSS} (mA) Min	I_{DSS} (mA) Max	G_{fs} (μmho) Min	G_{fs} (μmho) Max	G_{oss} (μmho) Max	I_{GSS} (pA) Max @ V_{DG} (V)	C_{iss} (pF) Max	C_{rss} (pF) Max	BV (V) Min	$\overline{e_n}$ (nV/√Hz) Max @ f (Hz)	I_{DSS} Match %	G_{fs} Match %	G_{oss1-2} (μmho)	I_{G1-IG2} 125°C (nA)	Process No.	Pkg. No.
2N5564	TO-71	15	2000	5.0	10		7500		45				0.5	3.0	5.0	30				100 @ 20	12	3.0	40	50	10	5.0	5.0			96	12
2N5565	TO-71	15	2000	10	25		7500		45				0.5	3.0	5.0	30				100 @ 20	12	3.0	40	50	10	5.0	10			96	12
2N5566	TO-71	15	2000	20	50		7500		45				0.5	3.0	5.0	30				100 @ 20	12	3.0	40	50	10	5.0	10			96	12
2N5911	TO-78	10	5000	10	20	100	5000	10,000	100		0.3	4.0	1.0	5.0	7.0	40				100 @ 15	5.0	1.2	25	20	10k	5.0	5.0	20	20	93	24
2N5912	TO-78	10	5000	15	40	100	5000	10,000	100		0.3	4.0	1.0	5.0	7.0	40				100 @ 15	5.0	1.2	25	20	10k	5.0	5.0	20	20	93	24
NPD5564	8-Pin	15	2000	5.0	10		7500		45				0.5	3.0	5.0	30				100 @ 20	12	3.0	40	50	10	5.0	5.0			96	67
NPD5565	Mini-	15	2000	10	25		7500		45				0.5	3.0	5.0	30				100 @ 20	12	3.0	40	50	10	5.0	10			96	67
NPD5566	DIP	15	2000	20	50		7500		45				0.5	3.0	5.0	30				100 @ 20	12	3.0	40	50	10	5.0	10			96	67
U257	TO-78	10	5000	100			5000	10,000	150				1.0	5.0	5.0	40				100 @ 15	5.0	1.2	25	30	10k	15	15	20		93	24
U430	TO-99	10	10,000				10,000	20,000	150				1.0	4.0	12	30				150 @ 15			25	10	100	10	10			92	24
U431	TO-99	10	10,000				10,000	20,000	150				2.0	6.0	24	60				150 @ 15			25	10	100	10	10				

Selection Guide

N-Channel FETs

LOW LEAKAGE—HIGH CMRR—WIDE BAND DUAL JFETs

Type No.	Case Style	OPERATING CONDITIONS FOR THESE CHARACTERISTICS: OP. CHAR. V_{DG} (V)	OP. CHAR. I_D (μA)	$\lvert V_{GS1-2}\rvert$ V_{OS} (mV) Max	DRIFT $\frac{\Delta V_{OS}}{\Delta T}$ (μV/°C) $\frac{\Delta V_{GS}}{\Delta T}$ Max	I_G (pA) Max	G_{fs} μmhos Min	G_{fs} μmhos Max	G_{oss} (μmho) Max	CMRR (dB) Min	V_{gs} (V) Min	V_{gs} (V) Max	V_p (V) Min	V_p (V) Max	I_{DSS} (mA) Min	I_{DSS} (mA) Max	G_{fs} (μmho) Min	G_{fs} (μmho) Max	G_{oss} (μmho) Max	I_{GSS} (pA) Max	@ V_{DG} (V)	C_{iss} (pF) Max	C_{rss} (pF) Max	BV (V) Min	e_n (nV/√Hz)@ Max	f (Hz)	I_{DSS} Match %	G_{fs} Match %	G_{oss1-2} (μmho)	I_{G1}-I_{G2} 125°C (nA)	Process No.	Pkg. No.
NDF9401	TO-78	20	200	5.0	5.0	5.0¶	950	2000	0.1	120	0.1	4.0	0.5	4.0	0.5	10				10	30	5.0	0.02	50	30	10	5.0	3.0	0.1	1.0	94	24
NDF9402	TO-78	20	200	5.0	10	5.0¶	950	2000	0.1	120	0.1	4.0	0.5	4.0	0.5	10				10	30	5.0	0.02	50	30	10	5.0	3.0	0.1		94	24
NDF9403	TO-78	20	200	10	10	5.0¶	950	2000	0.1	110	0.1	4.0	0.5	4.0	0.5	10				10	30	5.0	0.02	50	30	10	5.0	5.0	0.1	1.0	94	24
NDF9404	TO-78	20	200	15	10	5.0¶	950	2000	0.1	110	0.1	4.0	0.5	4.0	0.5	10				10	30	5.0	0.02	50	30	10	5.0	5.0	0.1	1.0	94	24
NDF9405	TO-78	20	200	25	25	5.0¶	950	2000	0.1	100	0.1	4.0	0.5	4.0	0.5	10				10	30	5.0	0.02	50	30	10	5.0	5.0	0.1	1.0	94	24
NDF9406	TO-71	20	200	5.0	5.0	5.0¶	950	2000	0.1	120	0.1	4.0	0.5	4.0	0.5	10				10	30	5.0	0.02	50	30	10	10	10	0.1	1.0	94	24
NDF9407	TO-71	20	200	5.0	10	5.0¶	950	2000	0.1	120	0.1	4.0	0.5	4.0	0.5	10				10	30	5.0	0.02	50	30	10	5.0	3.0	0.1	1.0	94	12
NDF9408	TO-71	20	200	10	10	5.0¶	950	2000	0.1	110	0.1	4.0	0.5	4.0	0.5	10				10	30	5.0	0.02	50	30	10	5.0	3.0	0.1	1.0	94	12
NDF9409	TO-71	20	200	15	10	5.0¶	950	2000	0.1	110	0.1	4.0	0.5	4.0	0.5	10				10	30	5.0	0.02	50	30	10	5.0	5.0	0.1	1.0	94	12
NDF9410	TO-71	20	200	25	25	5.0¶	950	2000	0.1	100	0.1	4.0	0.5	4.0	0.5	10				10	30	5.0	0.02	50	30	10	5.0	5.0	0.1	1.0	94	12

¶ V_{DG} = 35V

N-Channel FETs

ULTRA LOW LEAKAGE DUALS

Type No.	Case Style	OPERATING CONDITIONS FOR THESE CHARACTERISTICS: Oper. Cond. V_{DG} (V)	Oper. Cond. I_D (μA)	V_{GS1-2} V_{OS} (mV) Max	$\frac{\Delta V_{GS}}{\Delta T}$ DRIFT (μV/°C) Max	I_G (pA) Max	G_{fs} (mMho) Min	G_{fs} (mMho) Max	G_{oss} (μMho) Max	V_{GS} (V) Min	V_{GS} (V) Max	V_p (V) Min	V_p (V) Max	I_{DSS} (mA) Min	I_{DSS} (mA) Max	G_{fs} (mmho) Min	G_{fs} (mmho) Max	G_{oss} (μmho) Max	I_{GSS} (pA) Max	@ V_{GS} (V)	C_{iss} (pF) Max	C_{rss} (pF) Max	BV_{GSS} (V) Min	I_{G1}-I_{G2} @ 125°C (nA) Max	Process No.	Pkg. No.
2N5902	TO-78	10	30	5	5	3	50μ	1			4	0.6	4.5	30μ	0.5	70μ	0.25	5	5	20	3	1.5	40	2	84	24
2N5903	TO-78	10	30	5	10	3	50μ	1			4	0.6	4.5	30μ	0.5	70μ	0.25	5	5	20	3	1.5	40	2	84	24
2N5904	TO-78	10	30	10	20	3	50μ	1			4	0.6	4.5	30μ	0.5	70μ	0.25	5	5	20	3	1.5	40	2	84	24
2N5905	TO-78	10	30	15	40	3	50μ	1			4	0.6	4.5	30μ	0.5	70μ	0.25	5	5	20	3	1.5	40	2	84	24
2N5906	TO-78	10	30	5	5	1	50μ	1			4	0.6	4.5	30μ	0.5	70μ	0.25	5	2	20	3	1.5	40	0.2	84	24
2N5907	TO-78	10	30	5	10	1	50μ	1			4	0.6	4.5	30μ	0.5	70μ	0.25	5	2	20	3	1.5	40	0.2	84	24
2N5908	TO-78	10	30	10	20	1	50μ	1			4	0.6	4.5	30μ	0.5	70μ	0.25	5	2	20	3	1.5	40	0.2	84	24
2N5909	TO-78	10	30	15	40	1	50μ	1			4	0.6	4.5	30μ	0.5	70μ	0.25	5	2	20	3	1.5	40	0.2	84	24
U421	TO-78	PROCESS IN DEVELOPMENT																							84	24
U422	TO-78																								86	24
U423	TO-78																								86	24
U424	TO-78																								86	24
U425	TO-78																								86	24
U426	TO-78																								86	24

P-Channel FETs

SWITCHES

Transistor Type	Case Style	BV_{GSS} BV_{GDO} (V) @ I_G (μA) Min		I_{GSS} I_{DGO} (nA) @ V_{DG} (V) Max		$I_{D(off)}$ (nA) @ V_{DS} (V)	V_{GS} (V)	V_p (V) Min	Max	@ V_{DS} (V)	I_D (μA)	I_{DSS} (mA) @ V_{DS} (V) Min	Max		r_{ds} (Ω) @ I_D (mA) Max		C_{iss} (pF) @ V_{DS} (V) Max		V_{GS} (V)	C_{rss} (pF) @ V_{DS} (V) Max		V_{GS} (V)	t_{on} (ns) Max	t_{off} (ns) Max	Process No.	Pkg. No.
2N3382	TO-72	30	1	15	30	2	−5	6	1	5	−5	1	3	30	10	300										88	23
2N3384	TO-72	30	1	15	30	2	−5	6	4	5	−5	1	15	30	10	180										88	23
2N3386	TO-72	30	1	15	30	2.5	−5	10	4	9.5	−5	1	15	50	10	150										88	23
2N3993	TO-72	25	1	1.2*	15	1.2	−10	10	4	9.5	−10	1	10		10	150		16	−10	0	4.5	0	10			88	23
2N3993A	TO-72	25	1	1.2*	15	1.2	−10	10	4	9.5	−10	1	10		10	150		12	−10	0	3	0	10			88	23
2N3994	TO-72	25	1	1.2*	15	1.2	−10	6	1	5.5	−10	1	2		10	300		16	−10	0	4.5	0	10			88	23
2N3994A	TO-72	25	1	1.2*	15	1.2	−10	6	1	5.5	−10	1	2		10	300		12	−10	0	3	0	10			88	23
2N5018	TO-18	30	1	2	15	10	−15	12		10	−15	1	10		20	75		45	−15	0	10	0	12	35	65	88	11
2N5019	TO-18	30	1	2	15	10	−15	7		5	−15	1	5		20	150		45	−15	0	10	0	7	90	125	88	11
•2N5114	TO-18	30	1	0.5	20	0.5	−15	12	5	10	−15	.001	30	90	18	75	1	25	−15	0	7	0	12	16	21	88	11
•2N5115	TO-18	30	1	0.5	20	0.5	−15	7	3	6	−15	.001	16	60	15	100	1	25	−15	0	7	0	7	30	38	88	11
•2N5116	TO-18	30	1	0.5	20	0.5	−15	5	1	4	−15	.001	5	25	15	150	1	25	−15	0	7	0	5	42	60	88	11
J174	TO-92	30	1	1	20	1	−15	10	5	10	−15	.01	20	100	15	85	1	11	0	10	5.5	0	10	2	5	88	74
J175	TO-92	30	1	1	20	1	−15	10	3	6	−15	.01	7	60	15	125	.5	11	0	10	5.5	0	10	5	10	88	74
J176	TO-92	30	1	1	20	1	−15	10	1	4	−15	.01	2	25	15	250	.25	11	0	10	5.5	0	10	15	15	88	74
J177	TO-92	30	1	1	20	1	−15	10	.8	2.25	−15	.01	1.5	20	15	300	.1	11	0	10	5.5	0	10	20	20	88	74
P1086E	TO-92	30	1	2	20	10	−15	10		10	−15	.01	10		15	75	1	45	−15	0	10	15	0	35	50	88	71
P1087E	TO-92	30	1	2	20	10	−15	5		5	−15	.01	5		15	150		45	−15	0	10	15	0	40	75	88	71
U304	TO-18	30	1	0.5	20	0.5	−15	12	5	10	15	1	30	90	15	85		27	−15	0	7	0	12	35	35	88	11
U305	TO-18	30	1	0.5	20			7	3	4	15	1	15	60	15	110		27	−15	0	7	0	7	50	45	88	11
U306	TO-18	30	1	0.5	20			5	1	4	15	1	5	25	15	175		27	−15	0	7	0	5	60	80	88	11

• Note. JAN qualified per applicable MIL-S-19500 specification

P-Channel FETs

AMPLIFIERS

Transistor Type	Case Style	BV_{GSS} BV_{GDO} (V) @ I_G (μA) Min		I_{GSS} I_{DGO} (nA) @ V_{DG} (V) Max		V_p (V) Min	Max	@ V_{DS} (V)	I_D (μA)	I_{DSS} (mA) @ V_{DS} (V) Min	Max		G_{fs} (mmho) @ V_{DS} (V) Min	Max		G_{oss} (μmho) @ V_{DS} (V) Max		C_{iss} (pF) V_{DS} (V) Max	V_{GS} (V)	(pF) Max	C_{rss} V_{DS} (V)	V_{GS} (V)	$\left(\frac{NV}{\sqrt{Hz}}\right)_n$ @ Freq (Hz) Max		Process No.	Pkg. No.
•2N2608	TO-18	30	1	10	30	1	4	−5	1	0.9	4.5	5	1		5			17	−5	1				125	1000	89	11
2N2609	TO-18	30	1	30	30	1	4	−5	1	2	10	5	2.5		5			30	−5	1				125	1000	88	11
2N3329	TO-72	20	10	10	10		5	−15	10	1	3	10	1	2	10/1mA	20	10	20	−10	1				125	1000	89	23
2N3330	TO-72	20	10	10	10		6	−15	10	2	6	10	1.5	3	10/2mA	40	10	20	−10	1				125	1000	89	23
2N3331	TO-72	20	10	10	10		8	−15	10	5	15	10	2	4	10/5mA	100	10	20	−10	1				155	1000	89	23
2N3332	TO-72	20	10	10	10		6	−15	10	1	6	10	1	2.2	10/1mA	20	10	20	−10	1				65	1000	89	23
2N4381	TO-18	25	1	1	15	1	5	−15	1	3	12	15	2	6	15	75	15	20	−15	0	5	−15	0	20	1000	89	11
2N4382	TO-18	25	1	1	15	2.5	9	−15	1	10	30	15	4	8	15	100	15	20	−15	0	5	−15	0	20	1000	88	11

• Note. JAN qualified per applicable MIL-S-19500 specification

Selection Guide

P-Channel FETs

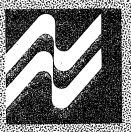
AMPLIFIERS (Continued)

Transistor Type	Case Style	BV_{GSS} BV_{GDO} (V) @ I_G Min	(μA)	I_{GSS} I_{DGO} (nA) @ V_{DG} Max	(V)	V_P (V) Min	Max	@ V_{DS} (V)	I_D (μA)	I_{DSS} (mA) Min	Max	@ V_{DS} (V)	G_{fs} (mmho) Min	Max	@ V_{DS} (V)	G_{oss} (μmho) @ V_{DS} Max	(V)	C_{iss} (pF) Max	V_{DS} (V)	V_{GS} (V)	C_{rss} (pF) Max	V_{DS} (V)	V_{GS} (V)	e_n $\left(\frac{NV}{\sqrt{Hz}}\right)$ @ Freq Max	(Hz)	Process No.	Pkg. No.
2N5020	TO-18	25	1	1	15	0.3	1.5	−15	1	0.3	1.2	15	1	3.5	15	20	15	25	−15	0	7	−15	0	30	1000	89	11
2N5021	TO-18	25	1	1	15	0.5	2.5	−15	1	1	3.5	15	1.5	6	15	20	15	25	−15	0	7	−15	0	30	1000	89	11
2N5460	TO-92	40	10	5	20	0.75	6	−15	1	1	5	15	1	4	15	50	15	7	−15	0	2	−15	0	115	100	89	71
2N5461	TO-92	40	10	5	20	1	7.5	−15	1	2	9	15	1.5	5	15	50	15	7	−15	0	2	−15	0	115	100	89	71
2N5462	TO-92	40	10	5	20	1.8	9	−15	1	4	16	15	2	6	15	50	15	7	−15	0	2	−15	0	115	100	89	71
J270	TO-92	30	1	0.2	20	0.5	2.0	15	.001	2	15	15	6.0	15.0	15	200	15	t20	15	0	t5	15	0	t10	1k	88	71
J271	TO-92	30	1	0.2	20	1.5	4.5	15	.001	6	50	15	8.0	18.0		500	15	t20	15	0	t5	15	0	t10	1k	88	71
PN4342	TO-92	25	10	10	15		5.5	−10	1	4	12	10	2	6	10	75	10	20	−10	0	5	−10	0	80	100	89	71
PN4343	TO-92	25	10	10	15		10	−10	1	10	30	10	4	8	10	100	10	20	−10	0	5	−10	0	80	100	88	71
PN4360	TO-92	20	10	10	15	0.7	10	−10	1	3	30	10	2	8	10	100	10	20	−10	0	5	−10	0	190	100	89	71
PN5033	TO-92	20	10	10	15	0.3	2.5	−10	1	0.3	3.5	10	1	5	10	20	10	25	−10	0	7	−10	0	100	1000	89	71
U300	TO-18	40	1	0.1	20	5	10	−15	.001	30	90		8	12	15			20	−15	15 mA	5.5	−15	15 mA	40	1000	88	11
U301	TO-18	40	1	0.1	20	2.5	60	−15	.001	15	60		7	11	15			20	−15	7 mA	5.5	−15	5.5 mA	40	1000	88	11

Pro-Electron FETs

AMPLIFIERS

Type No.	Case Style	BV_{GSS} BV_{GDO} (V) @ I_G Min	(μA)	I_{GSS} I_{DGD} (nA) @ V_{GD} Max	(V)	V_P (V) Min	Max	@ V_{DS} (V)	I_D (nA)	V_{GS} (V) Min	Max	@ V_{DS} (V)	I_D (μA)	I_{DSS} (mA) Min	Max	@ V_{DS} (V)	$R_e(Y_{FS})$ (mmho) @ f Min	Max	(MHz)	C_{iss} (pF) @ V_{DS} Typ	(V)	V_{GS} (V)	C_{rss} (pF) @ V_{DS} Typ	(V)	V_{GS} (V)	NF (dB) @ R_G = 1k e_n* Max	Typ	f (Hz)* (MHz)	Process No.	Pkg. No.
BF244A	TO-92	30	1	5	20	.5	8	15	10	.4	2.2	15	200	2	6.5	15	3	6.5	.001	4	20	−1	1.1	20	−1		1.5	100	50	74
BF244B	TO-92	30	1	5	20	.5	8	15	10	1.6	3.8	15	200	6	15	15	3	6.5	.001	4	20	−1	1.1	20	−1		1.5	100	50	74
BF244C	TO-92	30	1	5	20	.5	8	15	10	3.2	7.5	15	200	12	25	15	3	6.5	.001	4	20	−1	1.1	20	−1		1.5	100	50	74
BF245A	TO-92	30	1	5	20	.5	8	15	10	.4	2.2	15	200	2	6.5	15	3	6.5	.001	4	20	−1	1.1	20	−1				50	77
BF245B	TO-92	30	1	5	20	.5	8	15	10	1.6	3.8	15	200	6	15	15	3	6.5	.001	4	20	−1	1.1	20	−1				50	77
BF245C	TO-92	30	1	5	20	.5	8	15	10	3.2	7.5	15	200	12	25	15	3	6.5	.001	4	20	−1	1.1	20	−1				50	77
BF246A	TO-92	25	1	5	15	.6	14.5	15	10	1.5	4.0	15	200	30	80	15	8		.001	11	15	0	3.5	15	0				51	74
BF246B	TO-92	25	1	5	15	.6	14.5	15	10	3.0	7.0	15	200	60	140	15	8		.001	11	15	0	3.5	15	0				51	74
BF246C	TO-92	25	1	5	15	.6	14.5	15	10	5.5	12	15	200	110	250	15	8		.001	11	15	0	3.5	15	0				51	74
BF247A	TO-92	25	1	5	15	.6	14.5	15	10	1.5	4.0	15	200	30	80	15	8		.001	11	15	0	3.5	15	0				51	77
BF247B	TO-92	25	1	5	15	.6	14.5	15	10	3.0	7.0	15	200	60	140	15	8		.001	11	15	0	3.5	15	0				51	77
BF247C	TO-92	25	1	5	15	.6	14.5	15	10	5.5	12	15	200	110	250	15	8		.001	11	15	0	3.5	15	0				51	77
BF256A	TO-92	30	1	5	20					.5	7.5	15	200	3	7	15	4.5		.001				.7	20	−1		7.5	800	50	77
BF256B	TO-92	30	1	5	20					.5	7.5	15	200	6	13	15	4.5		.001				.7	20	−1		7.5	800	50	77
BF256C	TO-92	30	1	5	20					.5	7.5	15	200	11	18	15	4.5		.001				.7	20	−1		7.5	800	50	77
BC264A	TO-92	30	1	10	20	.5		15	10	.2	1.2	15	1000	2	4.5	15	2.5		.001	4.0	15	−1	1.2	15	−1		40*	10*	50	77
BC264B	TO-92	30	1	10	20	.5		15	10	.4	1.4	15	1500	3.5	6.5	15	3.0		.001	4.0	15	−1	1.2	15	−1		40*	10*	50	77
BC264C	TO-92	30	1	10	20	.5		15	10	.5	1.5	15	2500	5.0	8.0	15	3.5		.001	4.0	15	−1	1.2	15	−1		40*	10*	50	77
BC264D	TO-92	30	1	10	20	.5		15	10	.6	1.6	15	3500	7.0	12.0	15	4.0		.001	4.0	15	−1	1.2	15	−1		40*	10*	50	77



Section 3

Process Characteristics

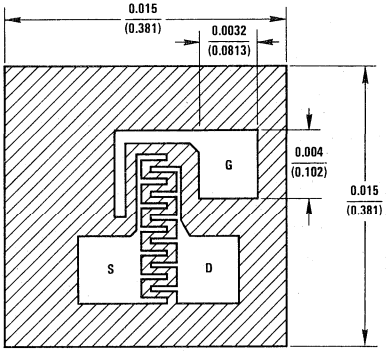
3

Introduction

This section contains complete design curves for all of National Semiconductor discrete FET processes. In all cases, temperature and $V_{GS(off)}$ distribution data is provided to facilitate worst-case design. In addition, a complete list, by package, of all device types supplied from this process is included to aid in cross reference searches and the selection of preferred device types.

The curves in this section should be considered typical of the process supplied by National Semiconductor. Every effort is made to keep the process in tolerance with the published graphs, but the exact distribution of any specific lot of material is not guaranteed.

Process 50 N-Channel JFET



GATE IS ALSO BACKSIDE CONTACT

DESCRIPTION

Process 50 is designed primarily for RF amplifier and mixer applications. It will operate up to 450 MHz with low noise figure and good power gain. These devices offer outstanding performance at VHF aircraft and communications frequencies. Their major advantage is low crossmodulation and intermodulation, low noise figure and good power gain. The device is also a good choice for analog switching where low capacitance is very important.

CHARACTERISTIC	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Gate-Source Breakdown Voltage	BV_{GSS}	V_{DS} = 0V, I_G = −1 μA	−25	−40		V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 15V, V_{GS} = 0V	1.0	10	20	mA
Forward Trans-conductance	g_{fs}	V_{DS} = 15V, V_{GS} = 0	3.0	5.5	7.0	mmhos
Forward Trans-conductance	g_{fs}	V_{DG} = 15V, I_D = 200 μA		1.1		mmhos
Reverse Gate Leakage	I_{GSS}	V_{GS} = −20V, V_{DS} = 0		−5.0	−100	pA
"ON" Resistance	r_{DS}	V_{DS} = 100 mV, V_{GS} = 0	100	175	500	Ω
Pinch Off Voltage	$V_{GS(OFF)}$	V_{DS} = 15V, I_D = 1 nA	−0.7	−3.5	−6.0	V
Output Conductance	g_{os}	V_{DG} = 15V, I_D = 1 mA, f = 1 kHz		10		μmhos
Feedback Capacitance	C_{rss}	V_{DG} = 15V, V_{GS} = 0		0.7	0.9	pF
Input Capacitance	C_{iss}	V_{DS} = 15V, V_{GS} = 0		3.5	4.0	pF
Noise Voltage	e_n	V_{DG} = 15V, I_D = 1 mA, f = 100 Hz		8.0		$nV/\sqrt{Hz}$
Noise Figure	NF	V_{DG} = 15V, I_D = 5 mA, R_G = 1 kΩ, f = 400 MHz		2.2	4.0	dB
Power Gain	G_{PS}	V_{DG} = 15V, I_D = 5 mA, f = 400 MHz		12		dB

This process is available in the following device types. *Denotes preferred parts.

TO-72 (CASE 25)

2N3823
2N3966
2N4223
2N4224
2N4416
*2N4416A
2N5078
2N5103
2N5104
2N5105
2N5556
2N5557
2N5558

TO-92 (CASE 72)

*2N5484
*2N5485
*2N5486
2N5555
2N5668
2N5669
2N5670
*J304
*J305
PN4223
PN4224
*PN4416
PN5163
MPF102
MPF106
MPF107
MPF110
MPF111

TO-92 (CASE 74)

2N3819
2N5248
BF244A
BF244B
BF244C
TIS58
TIS59

TO-92 (CASE 77)

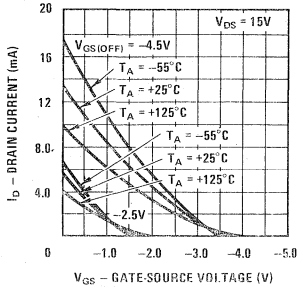
2N5949
2N5950
2N5951
2N5952
2N5953
BC264A
BC264B
BC264C
BC264D
BF245A
BF245B
BF245C
BF256A
BF256B
BF256C

QUALIFIED PER MIL-S-19500

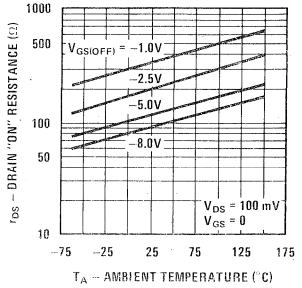
2N3823JAN, JANTX, JANTXV
2N4416AJAN, JANTX, JANTXV

Process 50

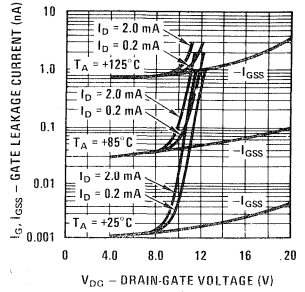
Transfer Characteristics



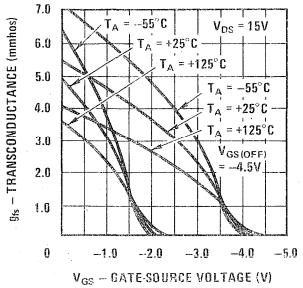
Channel Resistance vs Temperature



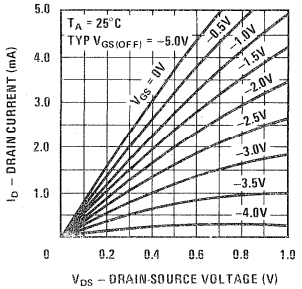
Leakage Current vs Voltage



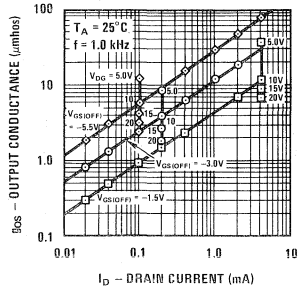
Transconductance Characteristics



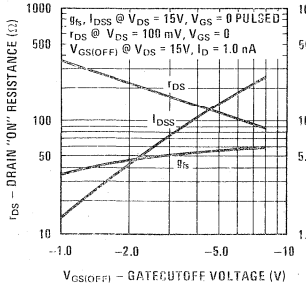
Common Drain-Source Characteristics



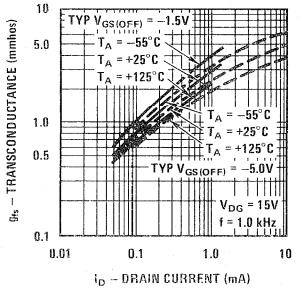
Output Conductance vs Drain Current



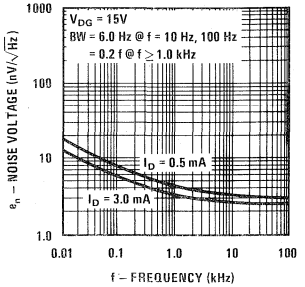
Parameter Interactions



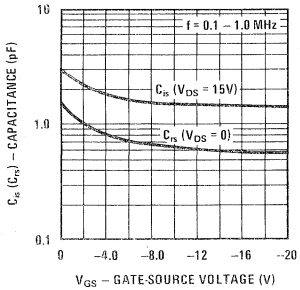
Transconductance vs Drain Current



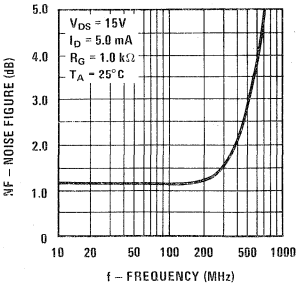
Noise Voltage vs Frequency



Capacitance vs Voltage

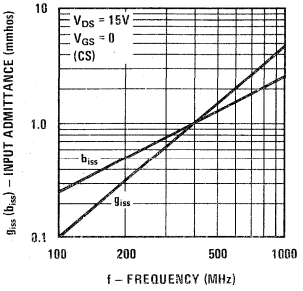


Noise Figure Frequency

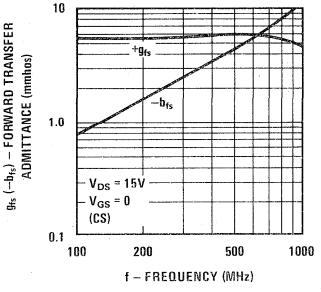


COMMON SOURCE

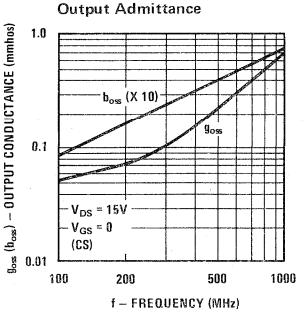
Input Admittance



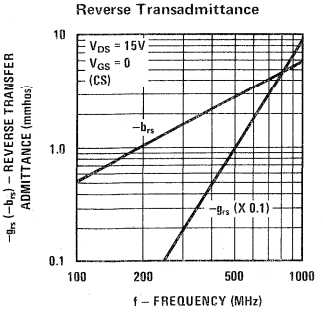
Forward Transadmittance



Output Admittance

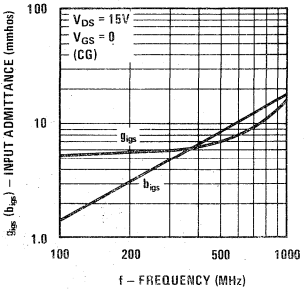


Reverse Transadmittance

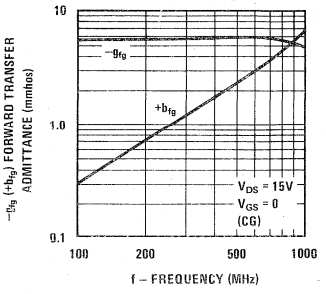


COMMON GATE

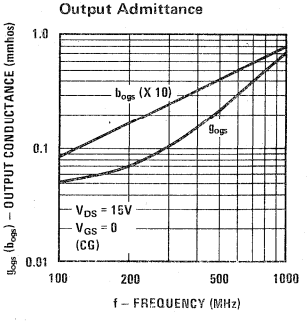
Input Admittance



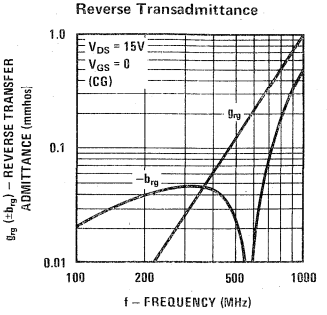
Forward Transadmittance



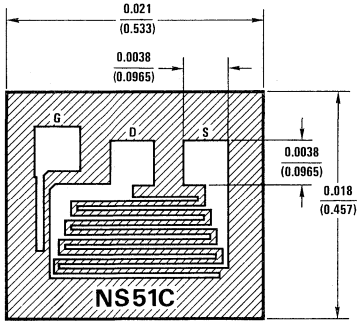
Output Admittance



Reverse Transadmittance



Process 51 N-Channel JFET



GATE IS ALSO BACKSIDE CONTACT

DESCRIPTION

Process 51 is designed primarily for electronic switching applications such as low ON resistance analog switching. It features excellent C_{iss} $R_{DS(ON)}$ time constant. The inherent zero offset voltage and low leakage current make these devices excellent for chopper stabilized amplifiers, sample and hold circuits, and reset switches. Low feedthrough capacitance also allows them to handle video signals to 100 MHz.

CHARACTERISTIC	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Gate-Source Breakdown Voltage	BV_{GSS}	V_{DS} = 0V, I_G = −1 μA	−30	−50		V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20V, V_{GS} = 0 Pulse Test	5.0	65	170	mA
Reverse Gate Leakage	I_{GSS}	V_{GS} = −20V, V_{DS} = 0		−15	−200	pA
"ON" Resistance	r_{DS}	V_{DS} = 100 mV, V_{GS} = 0	20	35	100	Ω
Forward Transconductance	g_{fs}	V_{DG} = 15V, I_D = 2 mA		8.5		mmhos
Pinch Off Voltage	$V_{GS(OFF)}$	V_{DS} = 20V, I_D = 1 nA	−0.5	−4.5	−9.0	V
Drain "OFF" Current	$I_{D(OFF)}$	V_{DS} = 20V, V_{GS} = −10V		15	200	pA
Feedback Capacitance	C_{rss}	V_{DG} = 15V, I_D = 5 mA, f = 1 MHz		3.5	4.0	pF
Input Capacitance	C_{iss}	V_{DS} = 15V, I_D = 5 mA, f = 1 MHz		12	16	pF
Noise Voltage	e_n	V_{DG} = 15V, I_D = 1 mA, f = 100 Hz		6.0		$nV/\sqrt{Hz}$
Turn-On Time	t_{on}	V_{DD} = 10V, I_D = 6.6 mA		12	20	ns
Turn-Off Time	t_{off}	V_{DD} = 10V, I_D = 6.6 mA		40	80	ns

This process is available in the following device types. *Denotes preferred parts.

TO-18 (CASE 02)

2N3970
2N3971
2N3972
*2N4091
*2N4092
*2N4093
*2N4391
*2N4392
*2N4393
*2N4856
2N4856A
*2N4857
2N4857A
*2N4858
2N4858A
2N4859
2N4859A
2N4860
2N4860A
2N4861
2N4861A

TO-72 (CASE 25)

*NF5101
*NF5102
*NF5103

TO-92 (CASE 72)

*2N5638
*2N5639
*2N5640
2N5653
2N5654
*J111
*J112
*J113
*PF5101
*PF5102
*PF5103
*PN4091
*PN4092
*PN4093
*PN4391
*PN4392
*PN4393
*PN4856
*PN4857
*PN4858
*PN4859
*PN4860
*PN4861
U1897E
U1898E
U1899E

TO-92 (CASE 74)

BF246A
BF246B
BF246C

TO-92 (CASE 77)

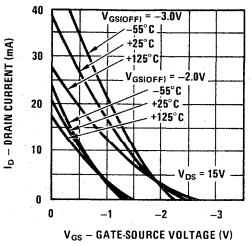
BF247A
BF247B
BF247C
TIS73
TIS74
TIS75

QUALIFIED PER MIL-S-19500

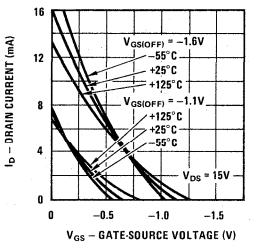
2N4091 JAN, JANTX, JANTXV
2N4092 JAN, JANTX, JANTXV
2N4093 JAN, JANTX, JANTXV
2N4856 JAN, JANTX, JANTXV
2N4857 JAN, JANTX JANTXV
2N4858 JAN, JANTX, JANTXV
2N4859 JAN, JANTX, JANTXV
2N4860 JAN, JANTX, JANTXV
2N4861 JAN, JANTX, JANTXV

Process 51

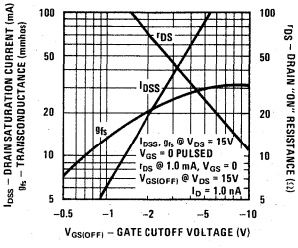
Transfer Characteristics



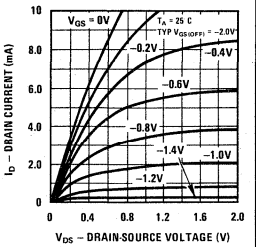
Transfer Characteristics



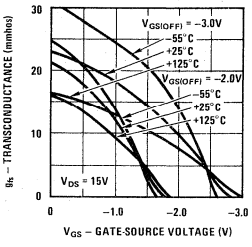
Parameter Interactions



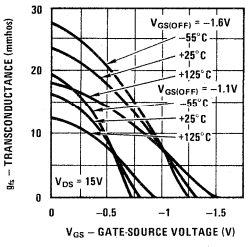
Common Drain-Source Characteristics



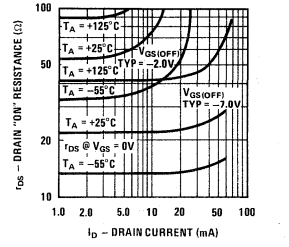
Transfer Characteristics



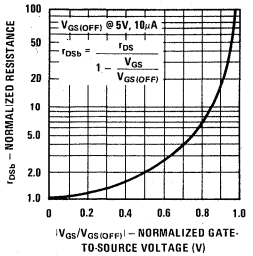
Transfer Characteristics



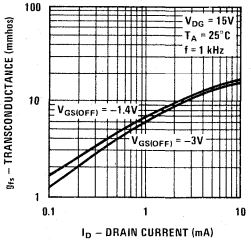
Resistance vs Drain Current



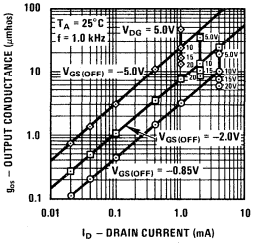
Normalized Drain Resistance vs Bias Voltage



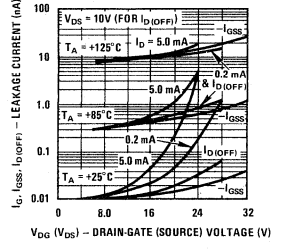
Transconductance vs Drain Current



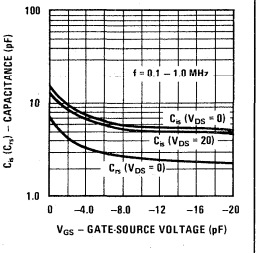
Output Conductance vs Drain Current



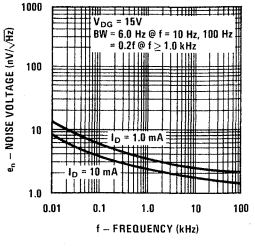
Leakage Current vs Voltage



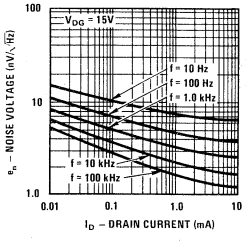
Capacitance vs Voltage



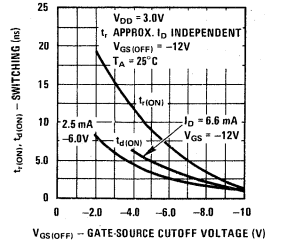
Noise Voltage vs Frequency



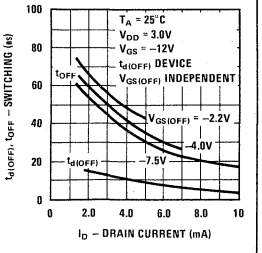
Noise Voltage vs Current



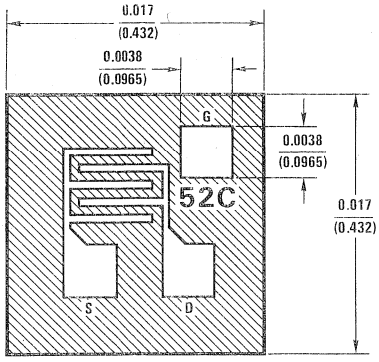
Turn-On Switching



Turn-Off Switching



Process 52 N-Channel JFET



GATE IS ALSO BACKSIDE CONTACT

DESCRIPTION

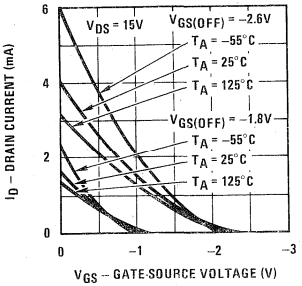
Process 52 is designed primarily for low level audio and general purpose applications. These devices provide excellent performance as input stages for piezo electric transducers or other high impedance signal sources. Their high output impedance and high voltage breakdown lend them to high gain audio and video amplifier applications. Source and drain are interchangeable.

CHARACTERISTIC	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Gate-Source Breakdown Voltage	BV_{GSS}	V_{DS} = 0V, I_G = −1 μA	−40	−70		V
Drain Saturation Current	I_{DSS}	V_{DS} = 20V, V_{GS} = 0V	0.2	1.5	12	mA
Forward Transconductance	g_{fs}	V_{DS} = 20V, V_{GS} = 0V	1.0	2.5	5.0	mmho
Forward Transconductance	g_{fs}	V_{DS} = 20V, I_D = 200 μA		700		μmho
Reverse Gate Leakage Current	I_{GSS}	V_{GS} = −30V, V_{DS} = 0V		−10		pA
Drain ON Resistance	r_{DS}	V_{DS} = 100 mV, V_{GS} = 0V	250	400	2000	Ω
Gate Cutoff Voltage	$V_{GS(OFF)}$,V_P	V_{DS} = 15V, I_D = 1 nA	−0.3	1.0	−8.0	V
Output Conductance	g_{os}	V_{DG} = 15V, I_D = 200 μA		2.0		μmho
Feedback Capacitance	C_{rss}	V_{DG} = 15V, V_{GS} = 0V, f = 1 MHz		1.3	1.8	pF
Input Capacitance	C_{iss}	V_{DG} = 15V, V_{GS} = 0V, f = 1 MHz		5	6	pF
Noise Voltage	e_n	V_{DG} = 15V, I_D = 200 μA, f = 100 Hz		10		$nV/\sqrt{Hz}$

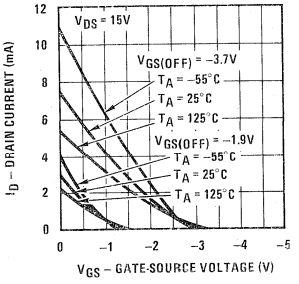
This process is available in the following device types.
*Denotes preferred parts.

TO-18 (CASE 02)	TO-72 (CASE 25)	TO-92 (CASE 72)
2N3069	*2N3684	*J201
2N3070	*2N3685	*J202
2N3071	*2N3686	*J203
2N3368	*2N3687	*PN3684
2N3369	2N3967	*PN3685
2N3370	2N3967A	*PN3686
2N3458	2N3968	*PN3687
2N3459	2N3968A	*PN4302
2N3460	2N3969	*PN4303
*2N4338	2N3969A	*PN4304
*2N4339		
*2N4340		
*2N4341		

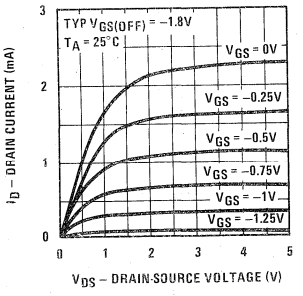
Transfer Characteristics



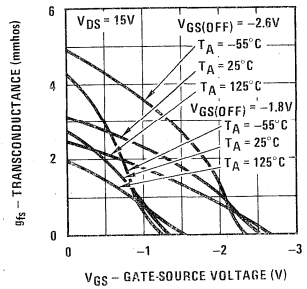
Transfer Characteristics



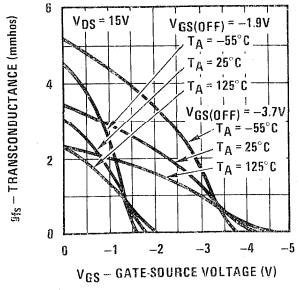
Common Drain-Source Characteristics



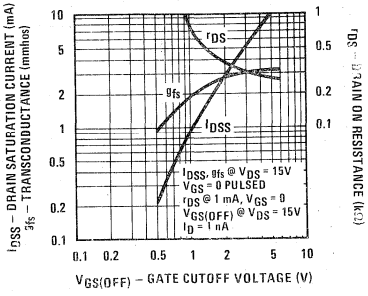
Transfer Characteristics



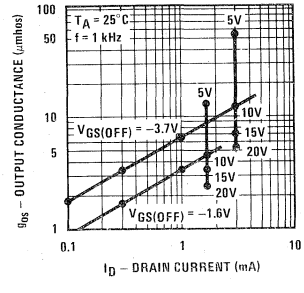
Transfer Characteristics



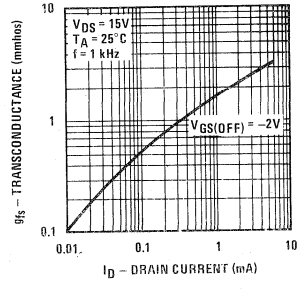
Parameter Interactions



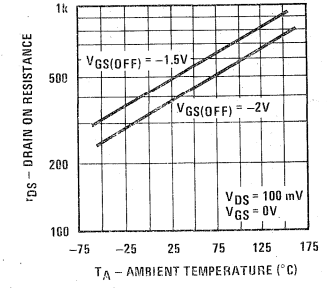
Output Conductance vs Drain Current



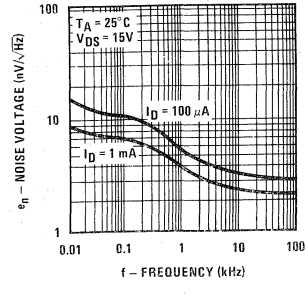
Transconductance vs Drain Current



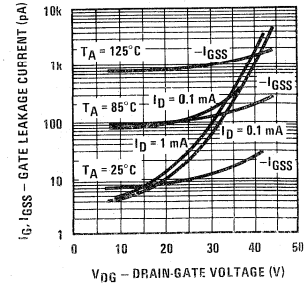
Channel Resistance vs Temperature



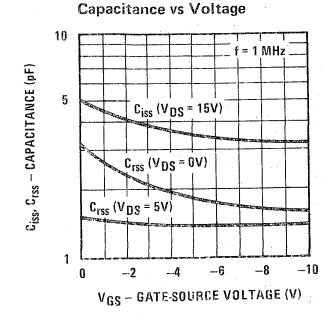
Noise Voltage vs Frequency



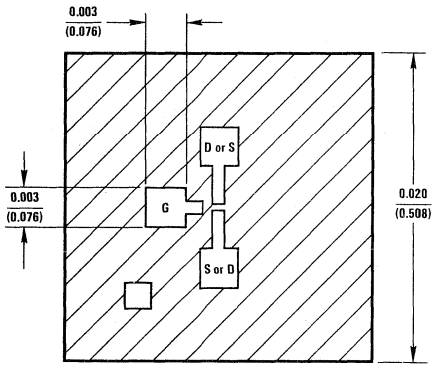
Leakage Current vs Voltage



Capacitance vs Voltage



Process 53 N-Channel JFET



GATE IS BACKSIDE CONTACT

DESCRIPTION

Process 53 is designed primarily for low current DC and audio applications. These devices provide excellent performance as input stages for sub pico-amp instrumentation or any high impedance signal sources.

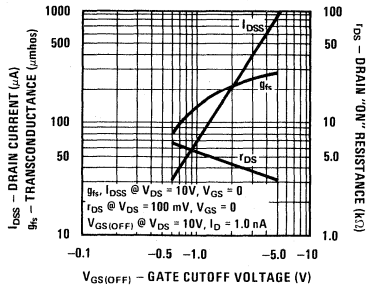
CHARACTERISTIC	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Gate-Source Breakdown Voltage	BV_{GSS}	V_{DS} = 0V, I_G = −1 μA	−40	−60		V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 10V, V_{GS} = 0	0.02	0.25	1.0	mA
Forward Trans-conductance	g_{fs}	V_{DS} = 10V, V_{GS} = 0	80	250	350	μmho
Forward Trans-conductance	g_{fs}	V_{DG} = 15V, I_D = 50 μA		120		μmho
Reverse Gate Leakage	I_{GSS}	V_{GS} = −20V, V_{DS} = 0		−0.3	−10	pA
Pinch Off Voltage	$V_{GS(OFF)}$	V_{DS} = 10V, I_D = 1 nA	−0.5	−2.2	−6.0	V
Feedback Capacitance	C_{rss}	V_{DG} = 15V, V_{GS} = 0, f = 1 MHz		0.85	1.0	pF
Input Capacitance	C_{iss}	V_{DS} = 15V, V_{GS} = 0, f = 1 MHz		2.0	2.5	pF
Output Conductance	g_{os}	V_{DG} = 10V, I_D = 50 μA		0.9	5.0	μmhos
Noise Voltage	e_n	V_{DG} = 10V, I_D = 50 μA, f = 100 Hz		45	150	$nV/\sqrt{Hz}$

This process is available in the following device types.
*Denotes preferred parts.

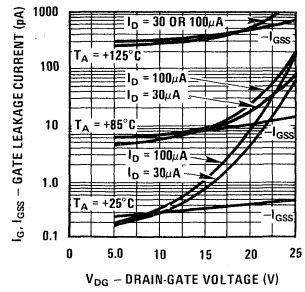
TO-72 (CASE 25)

2N4117
*2N4117A
2N4118
*2N4118A
2N4119
*2N4119A

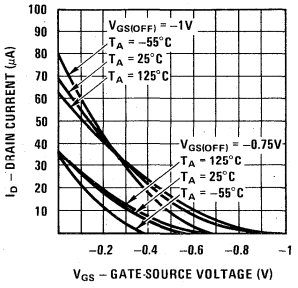
Parameter Interactions



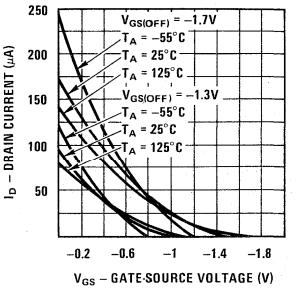
Leakage Current vs Voltage



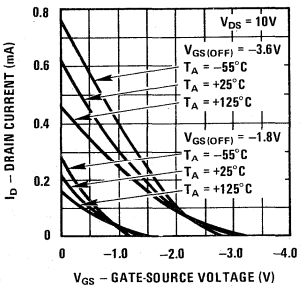
Transfer Characteristics



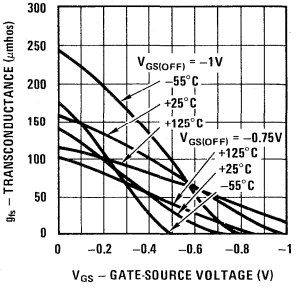
Transfer Characteristics



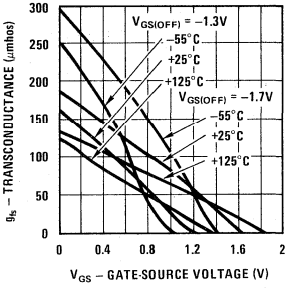
Transfer Characteristics



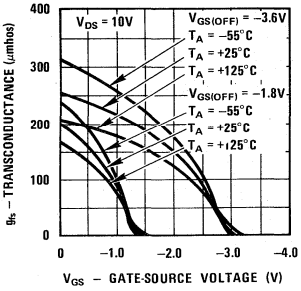
Transfer Characteristics



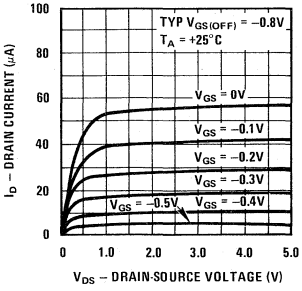
Transfer Characteristics



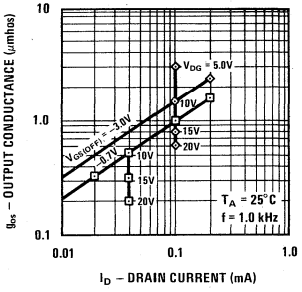
Transfer Characteristics



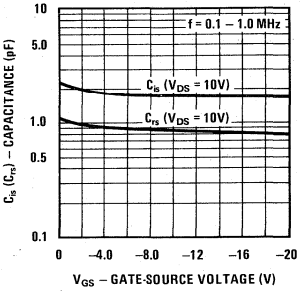
Common Drain-Source Characteristics



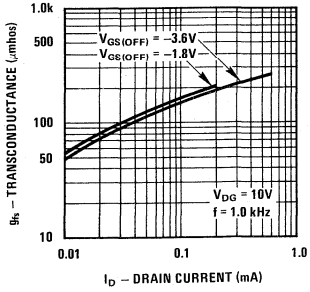
Output Conductance vs Drain Current



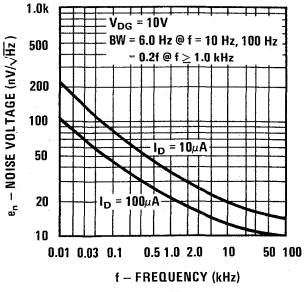
Capacitance vs Voltage



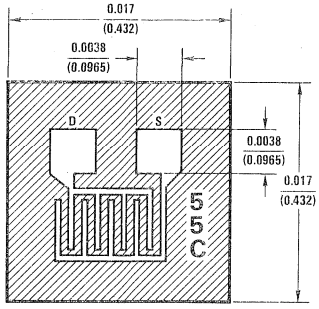
Transconductance vs Drain Current



Noise Voltage vs Frequency



Process 55 N-Channel JFET



GATE IS BACKSIDE CONTACT

DESCRIPTION

Process 55 is a general purpose low level audio amplifier and switching transistor. Wafer processing is similar to process 52 but process 55 uses a larger geometry. This results in higher Y_{fs}, I_{DSS}, and capacitance and lower $R_{DS(ON)}$. It is useful for audio and video frequency amplifiers and RF amplifiers under 50 MHz. It may also be used for analog switching applications.

CHARACTERISTIC	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Gate-Source Breakdown Voltage	BV_{GSS}	V_{DS} = 0V, I_G = −1 μA	−40	−70		V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20V, V_{GS} = 0	0.5	5.0	20	mA
Forward Transconductance	g_{fs}	V_{DS} = 20V, V_{GS} = 0	2.0	4.5	7.0	mmho
Forward Transconductance	g_{fs}	V_{DG} = 15V, I_D = 200 μA		1200		μmhos
Reverse Gate Leakage	I_{GSS}	V_{GS} = −30V, V_{DS} = 0		−10	−100	pA
"ON" Resistance	r_{DS}	V_{DS} = 100 mV, V_{GS} = 0	140	250	600	Ω
Pinch Off Voltage	$V_{GS(OFF)}$	V_{DS} = 20V, I_D = 1 nA	−0.5	−2.0	−8.0	V
Feedback Capacitance	C_{rss}	V_{DG} = 15V, V_{GS} = 0, f = 1 MHz		1.5	2.0	pF
Input Capacitance	C_{iss}	V_{DS} = 15V, V_{GS} = 0, f = 1 MHz		6.0	7.0	pF
Output Conductance	g_{os}	V_{DG} = 15V, I_D = 200 μA		2		μmhos
Noise Voltage	e_n	V_{DG} = 15V, I_D = 200 μA, f = 100 Hz		10		$nV/\sqrt{Hz}$

This process is available in the following device types. *Denotes preferred parts.

TO-18 (CASE 02)

2N3436
2N3437
2N3438
*2N5361
*2N5362
*2N5363
*2N5364

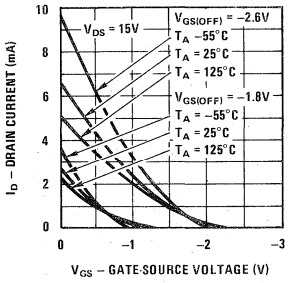
TO-72 (CASE 25)

2N3821
2N3822
2N3824
2N4220
2N4220A
2N4221
2N4221A
2N4222
2N4222A
*2N5358
*2N5359
*2N5360

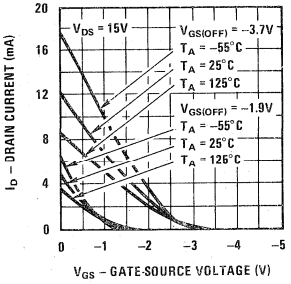
TO-92 (CASE 72)

*2N5457
*2N5458
*2N5459
MPF103
MPF104
MPF105
MPF108
MPF109
MPF112
PN4220
PN4221
PN4222

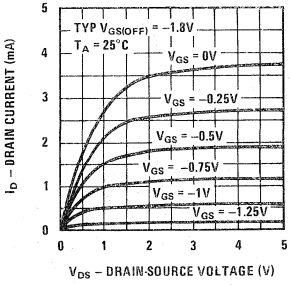
Transfer Characteristics



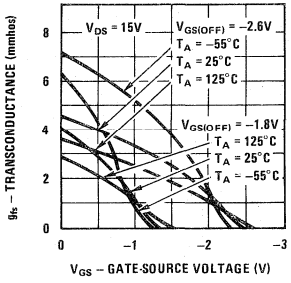
Transfer Characteristics



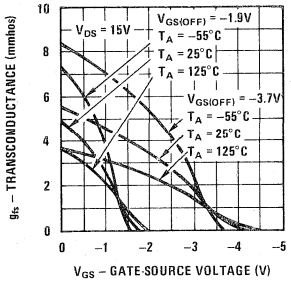
Common Drain-Source Characteristics



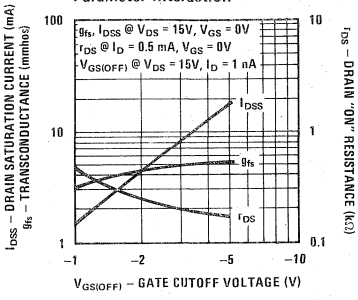
Transfer Characteristics



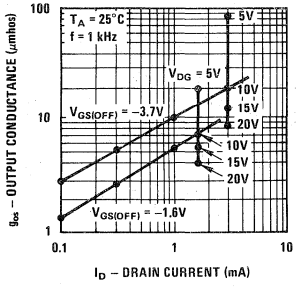
Transfer Characteristics



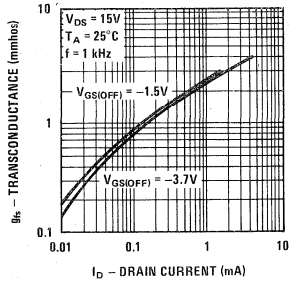
Parameter Interaction



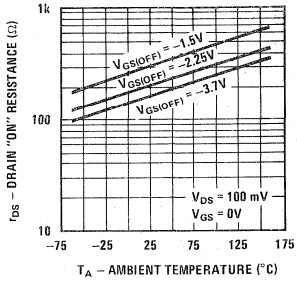
Output Conductance vs Drain Current



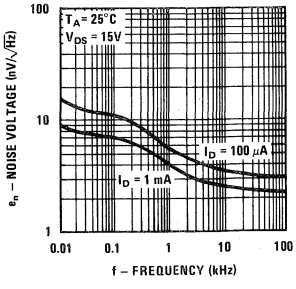
Transconductance vs Drain Current



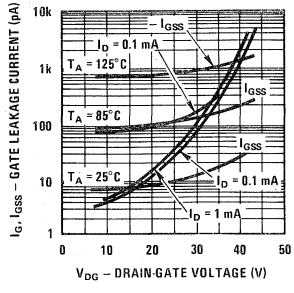
Channel Resistance vs Temperature



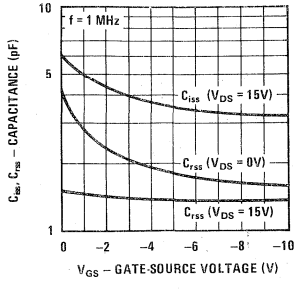
Noise Voltage vs Frequency



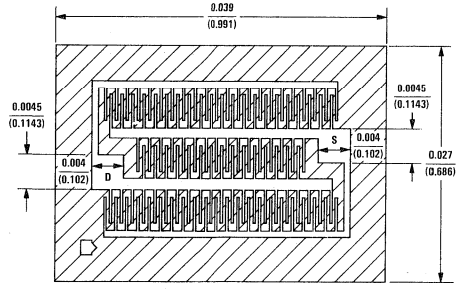
Leakage Current vs Voltage



Capacitance vs Voltage



Process 58 N-Channel JFET



GATE IS BACKSIDE CONTACT

DESCRIPTION

Process 58 was developed for analog or digital switching applications where very low $r_{DS(ON)}$ is mandatory. Switching times are very fast and $R_{DS(ON)}$ C_{iss} time constant is low. The 6Ω typical on resistance is very useful in precision multiplex systems where switch resistance must be held to an absolute minimum. With r_{DS} increasing only 0.7%/ °C, accuracy is retained over a wide temperature excursion.

CHARACTERISTIC	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Gate-Source Breakdown Voltage	BV_{GSS}	V_{DS} = 0V, I_G = −1 μA	−25	−30		V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 5V, V_{GS} = 0 Pulse Test	100	400	1000	mA
Reverse Gate Leakage	I_{GSS}	V_{GS} = −15V, V_{DS} = 0		−50	−500	pA
"ON" Resistance	r_{DS}	V_{DS} = 100 mV, V_{GS} = 0	3.0	6.0	20	Ω
Pinch Off Voltage	$V_{GS(OFF)}$	V_{DS} = 5V, I_D = 3 nA	−0.5	−5.0	−12	V
Drain "OFF" Current	$I_{D(OFF)}$	V_{DS} = 5V, V_{GS} = −10V		0.05	20	nA
Feedback Capacitance	C_{rss}	V_{DG} = 15V, I_D = 2 mA, f = 1 MHz		12	25	pF
Input Capacitance	C_{iss}	V_{DG} = 15V, I_D = 2 mA, f = 1 MHz		25	50	pF
Forward Transconductance	g_{fs}	V_{DG} = 10V, I_D = 2 mA		10		mmhos
Output Conductance	g_{os}	V_{DG} = 10V, I_D = 2 mA		100		μmhos
Noise Voltage	e_n	V_{DG} = 15V, I_D = 2 mA, f = 100 Hz		6.0		$nV/\sqrt{Hz}$

This process is available in the following device types. *Denotes preferred parts.

TO-39 (CASE 09)

U320
U321
U322

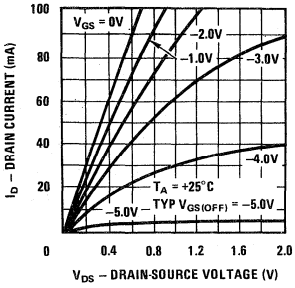
TO-52 (CASE 07)

*2N5432
*2N5433
*2N5434

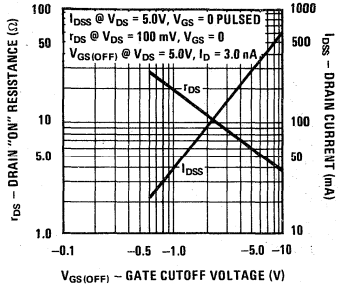
TO-92 (CASE 72)

*J108
*J109
*J110

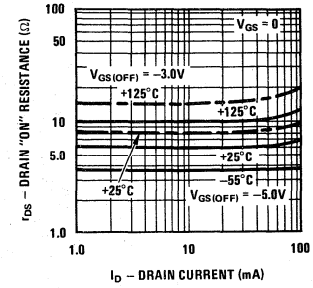
Common Drain-Source Characteristics



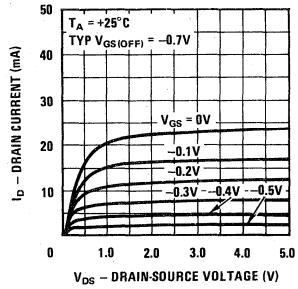
Parameter Interactions



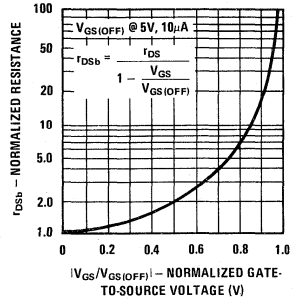
"ON" Resistance vs Drain Current



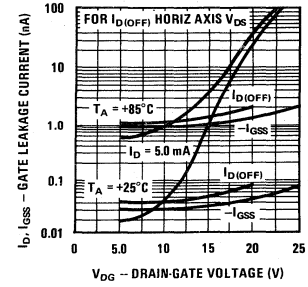
Common Drain-Source Characteristics



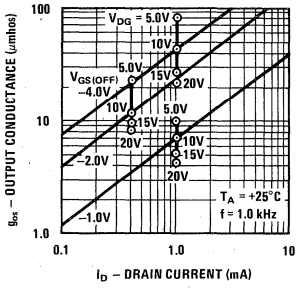
Normalized Drain Resistance vs Bias Voltage



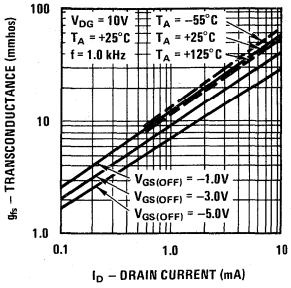
Leakage Current vs Voltage



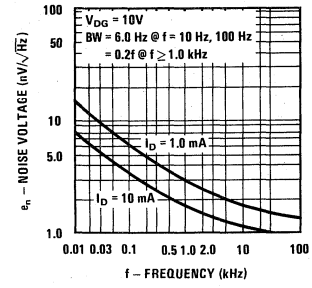
Output Conductance vs Drain Current



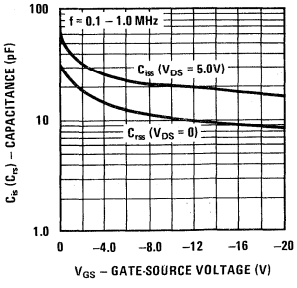
Transconductance vs Drain Current



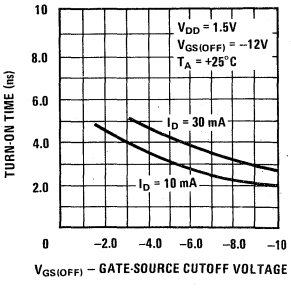
Noise Voltage vs Frequency



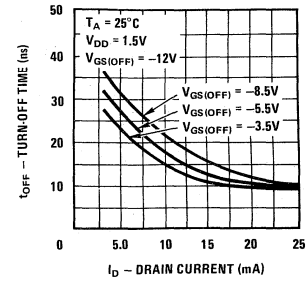
Capacitance vs Voltage



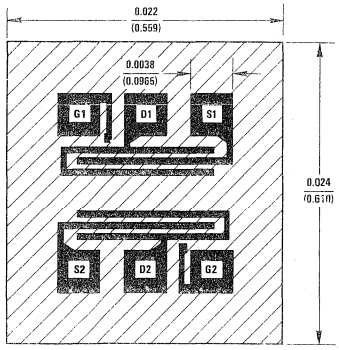
Switching Turn-On vs Gate-Source Voltage



Switching Turn-On Time vs Drain Current



Process 83 N-Channel JFET



DESCRIPTION

Process 83 is a monolithic dual JFET with a diode isolated substrate. It is intended for operational amplifier input buffer applications. Processing results in low input bias current and virtually unmeasureable offset current. Likewise matching characteristics are virtually independent of operating current and voltage, providing design flexibility. Most GP 2N types are sorted from this family.

CHARACTERISTIC	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Gate-Source Breakdown Voltage	BV_{GSS}	V_{DS} = 0V, I_G = −1 μA	−50	−70		V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 15V, V_{GS} = 0	0.5	2.5	8.0	mA
Forward Transconductance	g_{fs}	V_{DS} = 15V, V_{GS} = 0	1.0	2.5	5.0	mmho
Pinch Off Voltage	$V_{GS(OFF)}$	V_{DS} = 15V, I_D = 1 nA	−0.5	−2.0	−4.5	V
Gate Current	I_G	V_{DG} = 20V, I_D = 0.2 mA		3.0	50	pA
Forward Transconductance	g_{fs}	V_{DG} = 15V, I_D = 0.2 mA	600	850		μmhos
Output Conductance	g_{os}	V_{DG} = 15V, I_D = 0.2 mA		1.0	5.0	μmhos
"ON" Resistance	r_{DS}	V_{DS} = 100 mV, V_{GS} = 0		450		Ω
Noise Voltage	e_n	V_{DG} = 15V, I_D = 0.2 mA f = 100 Hz		10	50	$nV/\sqrt{Hz}$
Differential Match	$\lvert V_{GS1}-V_{GS2}\rvert$	V_{DG} = 15V, I_D = 0.2 mA		7.0	25	mV
Differential Match	ΔV_{GS1-2}	V_{DG} = 15V, I_D = 0.2 mA		10	50	μV/°C
Common Mode Rejection	CMRR	V_{DG} = 15V, I_D = 0.2 mA	80	95		dB
Feedback Capacitance	C_{rs}	V_{DG} = 15V, I_D = 0.2 mA, f = 1 MHz		1.0	1.2	pF
Input Capacitance	C_{is}	V_{DG} = 15V, I_D = 0.2 mA, f = 1 MHz		3.4	4.0	pF

This process is available in the following device types. *Denotes preferred parts.

TO-71 (CASE 12)

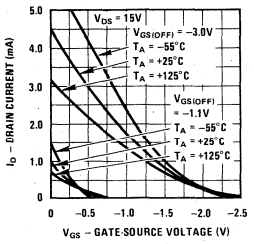
2N3921	2N5047	U233	J410
2N3922	*2N5196	U234	J411
*2N3954	*2N5197	U235	J412
*2N3954A	*2N5198		
*2N3955	*2N5199		
*2N3955A	2N5452		
*2N3956	2N5453		
*2N3957	2N5454		
*2N3958	*2N5545		
2N4084	*2N5546		
2N4085	*2N5547		
2N5045	U231		
2N5046	U232		

8-Pin MiniDIP (CASE 60)

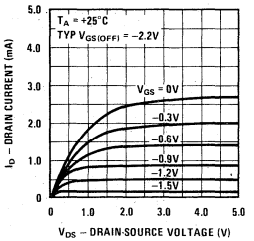
8-Pin MiniDIP (CASE 67)

*NPD8301
*NPD8302
*NPD8303

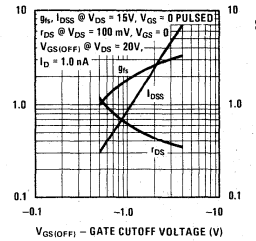
Transfer Characteristics



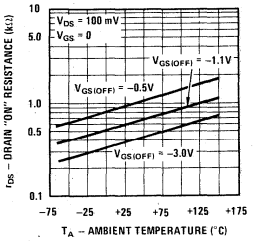
Common Drain-Source Characteristics



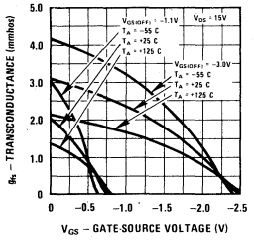
Parameter Interactions



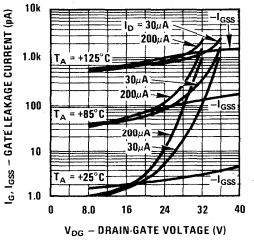
Channel Resistance vs Temperature



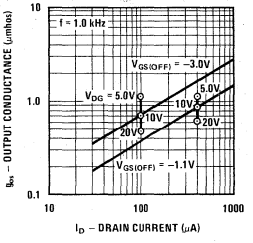
Transfer Characteristics



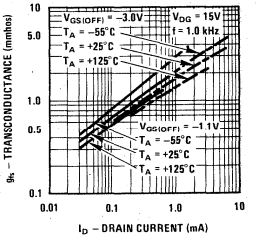
Leakage Current vs Voltage



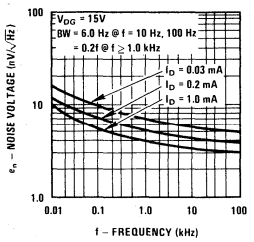
Output Conductance vs Drain Current



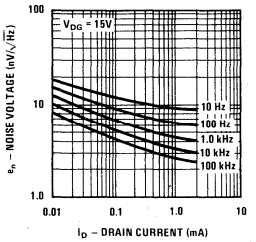
Transconductance vs Drain Current



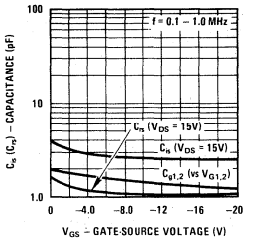
Noise Voltage vs Frequency



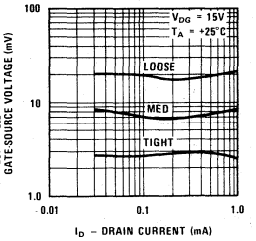
Noise Voltage vs Current



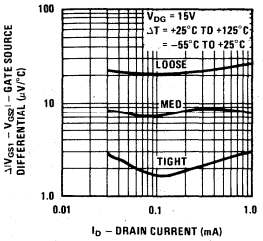
Capacitance vs Voltage



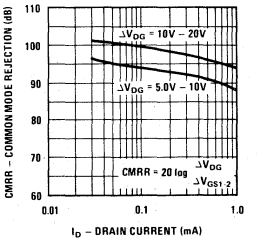
Differential Offset



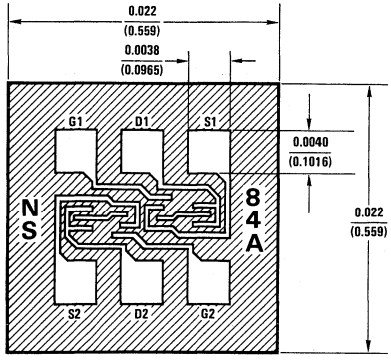
Differential Drift



CMRR vs Drain Current



Process 84 N-Channel JFET



DESCRIPTION

Process 84 is a monolithic dual JFET with a diode isolated substrate. It is designed for the most critical operational amplifier input stages or electrometer single ended preamp. Ideal for medical applications and instrumentation inputs where subpicoamp inputs are important. Device design considered high CMRR, subpicoamp leakage over wide input swings, low capacitance, and tight match over wide current range.

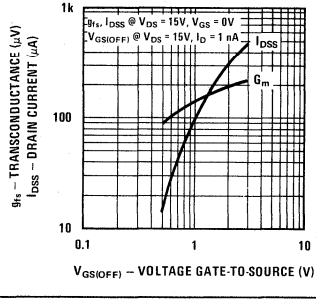
CHARACTERISTIC	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Gate-Source Breakdown Voltage	BV_{GSS}	V_{DS} = 0V, I_G = −1 μA	−40	−60		V
Drain Saturation Current	I_{DSS}	V_{DS} = 15V, V_{GS} = 0V	20	300	1000	μA
Forward Transconductance	g_{fs}	V_{DS} = 15V, V_{GS} = 0V	90	180	300	μV
Forward Transconductance	g_{fs}	V_{DS} = 15V, I_D = 30 μA	50	120	150	μV
Gate Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 15V, I_D = 1 nA	0.5	2	4.5	V
Reverse Gate Leakage Current	I_{GSS}	V_{DS} = 0V, V_{GS} = −20V		1	5	pA
Gate Leakage Current	I_G	V_{DG} = 10V, I_D = 30 μA		0.5	3	pA
Feedback Capacitance	C_{rss}	V_{DS} = 15V, V_{GS} = 0, f = 1 MHz		0.3	0.4	pF
Input Capacitance	C_{iss}	V_{DS} = 15V, V_{GS} = 0, f = 1 MHz		2	3	pF
Noise Voltage	e_n	V_{DS} = 15V, I_D = 30 μA, f = 1 kHz		30	50	$nV/\sqrt{Hz}$
Noise Voltage	e_n	V_{DS} = 15V, I_D = 30 μA, f = 10 Hz		180		$nV/\sqrt{Hz}$
Output Conductance	g_{os}	V_{DS} = 10V, I_D = 30 μA		0.1	0.2	μV
Differential Gate-Source Voltage	$\lvert V_{GS1}-V_{GS2}\rvert$	V_{DS} = 10V, I_D = 30 μA		12	25	mV
Differential Gate-Source Voltage Drift	ΔV_{GS1-2}	V_{DS} = 10V, I_D = 30 μA		10	50	μV/°C
Common-Mode Rejection Ratio	CMRR	V_{DS} = 10V, I_D = 30 μA		112		dB

This process is available in the following device types. *Denotes preferred parts.

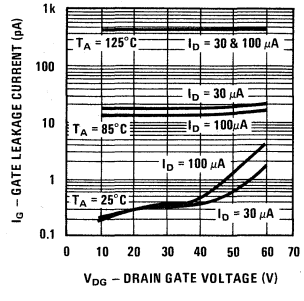
TO-78 (CASE 24)

2N5902	*2N5906
2N5903	*2N5907
2N5904	*2N5908
2N5905	*2N5909

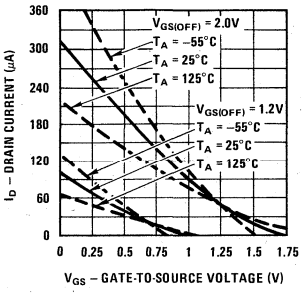
Parameter Interactions



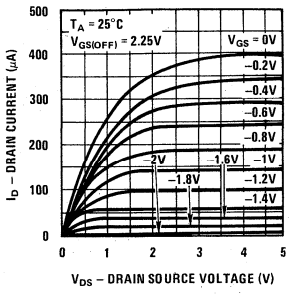
Leakage Current vs Voltage and Drain Current



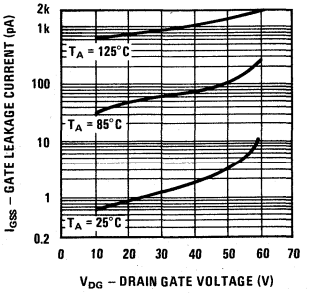
Transfer Characteristics



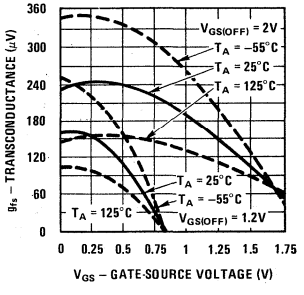
Common Drain-Source Characteristics



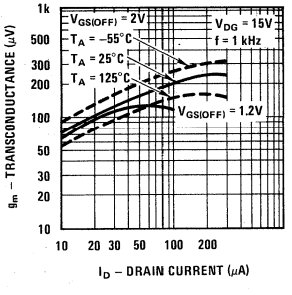
Leakage Current vs Voltage



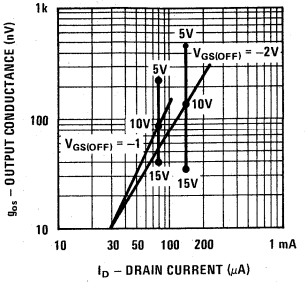
Transfer Characteristics



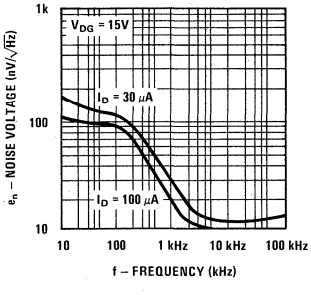
Transconductance vs Drain Current



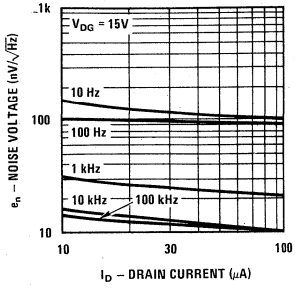
Output Conductance vs Drain Current



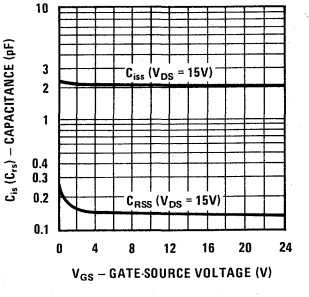
Noise Voltage vs Frequency



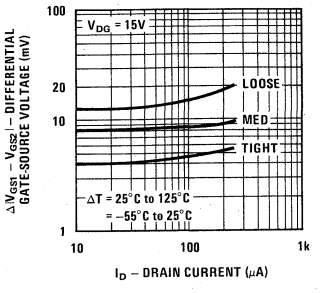
Noise Voltage vs Current



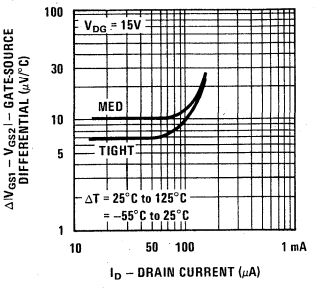
Capacitance vs Voltage



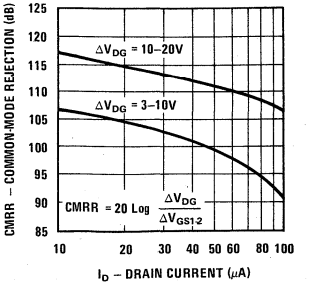
Differential Offset



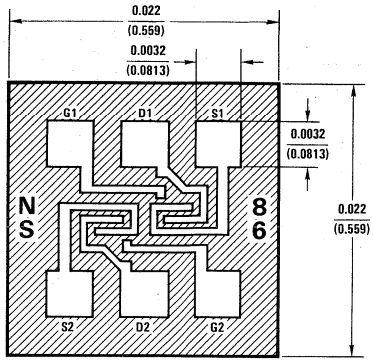
Differential Drift



CMRR vs Drain Current



Process 86 Monolithic Dual JFET



DESCRIPTION

Process 86 is a monolithic dual JFET with a diode isolated substrate. It is intended for critical amplifier input stages requiring low noise, sub picoamp bias currents and high gain. Exacting process control results in consistent parameter distribution with tight match and low drift.

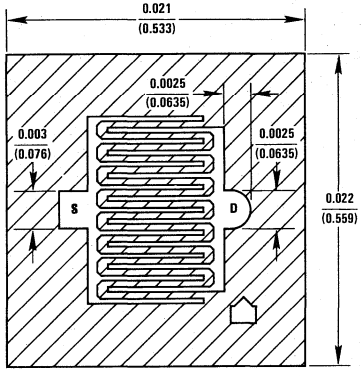
This process is available in the following device types. *Denotes preferred parts.

TO-78 (CASE 24)

U421
U422
U423
U424
U425
U426

PROCESS IN DEVELOPMENT

Process 88 P-Channel JFET



GATE IS BACKSIDE CONTACT

DESCRIPTION

Process 88 is designed primarily for electronic switching applications where a P channel device is desirable. Inherent zero offset voltage, low leakage and low $R_{DS(ON)}$ C_{iss} time constant make this device excellent for low level analog switching, sample and hold circuits and chopper stabilized amplifiers. This device is the complement to Process 51.

CHARACTERISTIC	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Gate-Source Breakdown Voltage	BV_{GSS}	V_{DS} = 0V, I_G = 1 μA	30	40		V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = −15V, V_{GS} = 0	−5.0	−30	−90	mA
Forward Transconductance	g_{fs}	V_{DS} = −15V, V_{GS} = 0	4.0	13	17	mmhos
Forward Transconductance	g_{fs}	V_{DG} = −15V, I_D = −2 mA		3.5		mmhos
Gate Leakage	I_{GSS}	V_{GS} = 20V, V_{DS} = 0		0.05	1.0	nA
"ON" Resistance	r_{DS}	V_{DS} = −100 mV, V_{GS} = 0	50	80	200	Ω
Pinch Off Voltage	$V_{GS(OFF)}$	V_{DS} = −15V, I_D = −1 nA	0.5	5.0	10	V
Drain "OFF" Current	$I_{D(OFF)}$	V_{DS} = −15V, V_{GS} = 10V		−0.05	−10	nA
Feedback Capacitance	C_{rss}	V_{DG} = −15V, I_D = −2 mA, f = 1 MHz		4.0	5.0	pF
Input Capacitance	C_{iss}	V_{DS} = −15V, I_D = −2 mA, f = 1 MHz		14	15	pF
Output Conductance	g_{os}	V_{DG} = −15V, I_D = −2 mA		100	300	μmhos
Noise Voltage	e_n	V_{DG} = −15V, I_D = −2 mA, f = 100 Hz		20		nV/$\sqrt{Hz}$

This process is available in the following device types. *Denotes preferred parts.

TO-18 (CASE 11)

2N2609
2N4382
2N5018
2N5019
*2N5114
*2N5115
*2N5116
U300
U301
U304
U305
U306

TO-72 (CASE 23)

2N3382
2N3384
2N3386
2N3993
2N3993A
2N3994
2N3994A

TO-92 (CASE 71)

P1086E
P1087E
PN4343

TO-92 (CASE 74)

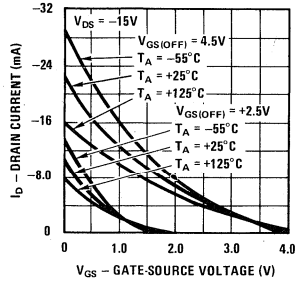
*J174
*J175
*J176
*J177
*J270
*J271

QUALIFIED PER MIL-S-19500

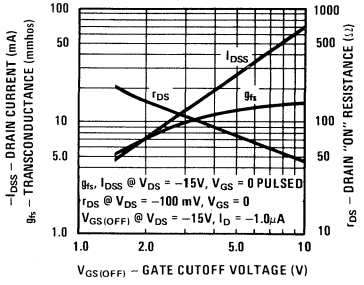
*2N5114JAN, JANTX, JANTXV
*2N5115JAN, JANTX, JANTXV
*2N5116JAN, JANTX, JANTXV

Process 88

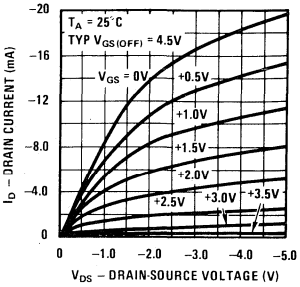
Transfer Characteristics



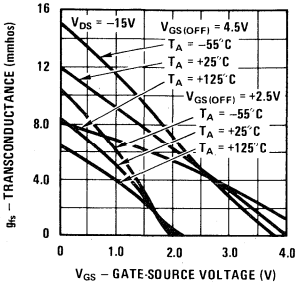
Parameter Interactions



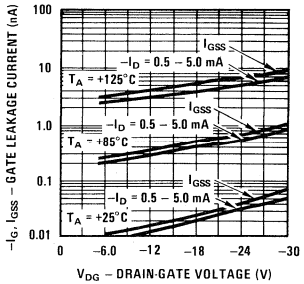
Common Drain-Source Characteristics



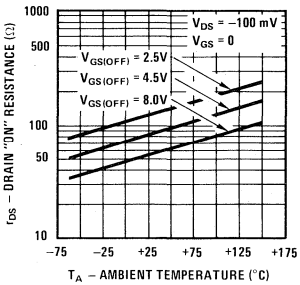
Transfer Characteristics



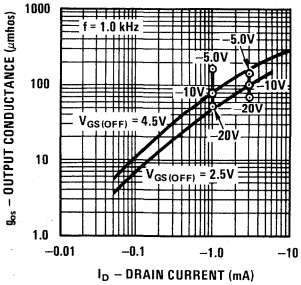
Leakage Current vs Voltage



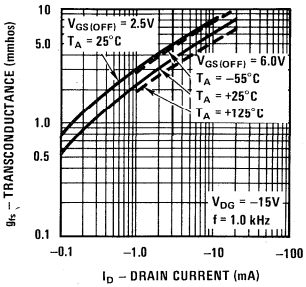
Channel Resistance vs Temperature



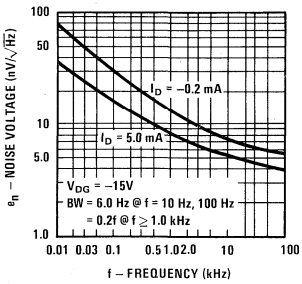
Output Conductance vs Drain Current



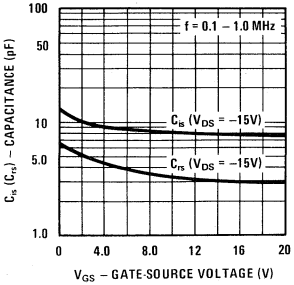
Transconductance vs Drain Current



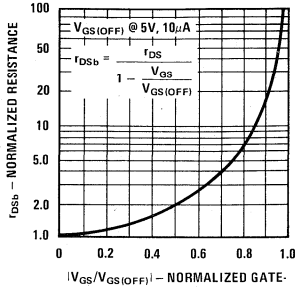
Noise Voltage vs Frequency



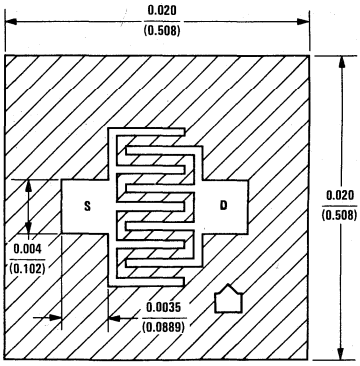
Capacitance vs Voltage



Normalized Drain Resistance vs Bias Voltage



Process 89 P-Channel JFET



GATE IS BACKSIDE CONTACT

DESCRIPTION

Process 89 is designed primarily for low level amplifier applications. This device is the complement to Process 55. Commonly used in voltage variable resistor applications.

CHARACTERISTIC	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Gate-Source Breakdown Voltage	BV_{GSS}	V_{DS} = 0V, I_G = 1 μA	20	40		V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = −15V, V_{GS} = 0	−0.3	−4.0	−20	mA
Forward Transconductance	g_{fs}	V_{DS} = −15V, V_{GS} = 0	1.0	2.5	4.0	mmhos
Forward Transconductance	g_{fs}	V_{DG} = −15V, I_D = −0.2 mA		700		μmhos
Gate Leakage	I_{GSS}	V_{GS} = 20V, V_{DS} = 0		0.02	1.0	nA
Pinch Off Voltage	$V_{GS(OFF)}$	V_{DS} = −15V, I_D = −1 nA	0.5	3.0	9.0	V
Feedback Capacitance	C_{rss}	V_{DG} = −15V, V_{GS} = 0, f = 1 MHz		2.0	2.5	pF
Input Capacitance	C_{is}	V_{DS} = −15V, I_D = −2 mA, f = 1 MHz		7.0	8.5	pF
"ON" Resistance	r_{DS}	V_{DS} = −100 mV, V_{GS} = 0		450		Ω
Output Conductance	g_{os}	V_{DG} = −15V, I_D = −0.2 mA		5.0	15	μmhos
Noise Voltage	e_n	V_{DG} = −15V, I_D = −0.2 mA, f = 100 Hz		30		$nV/\sqrt{Hz}$

This process is available in the following device types. *Denotes preferred parts.

TO-18 (CASE 11)

2N2608
2N4381
2N5020
2N5021

TO-72 (CASE 23)

2N3329
2N3330
2N3331
2N3332

TO-92 (CASE 71)

*2N5460
*2N5461
*2N5462
PN4342
PN4360
PN5033

TO-92 (CASE 74)

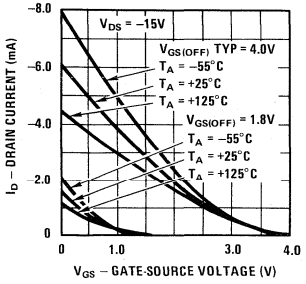
2N3820

QUALIFIED PER MIL-S-19500

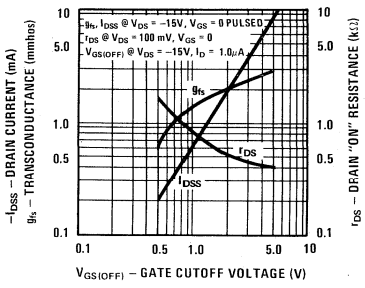
2N2608JAN

Process 89

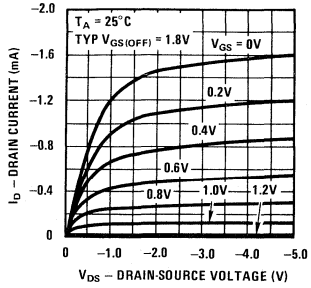
Transfer Characteristics



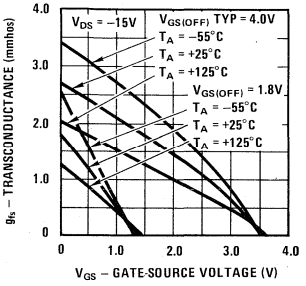
Parameter Interactions



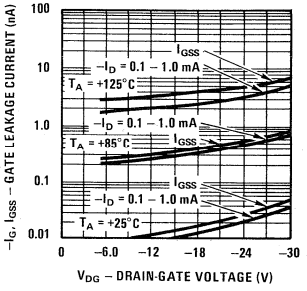
Common Drain-Source Characteristics



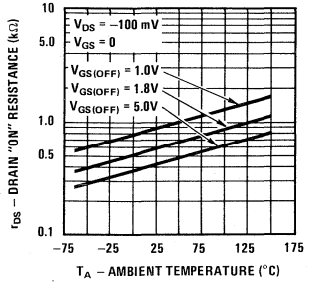
Transfer Characteristics



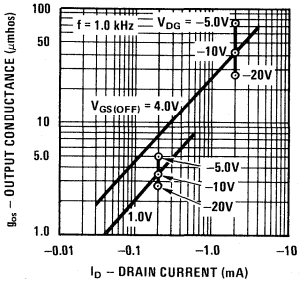
Leakage Current vs Voltage



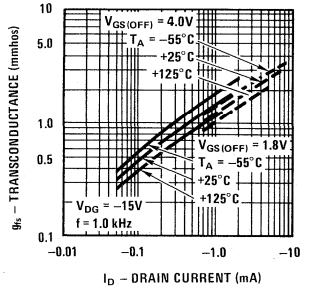
Channel Resistance vs Temperature



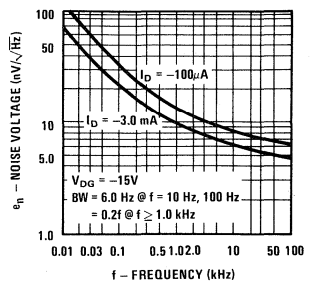
Output Conductance vs Drain Current



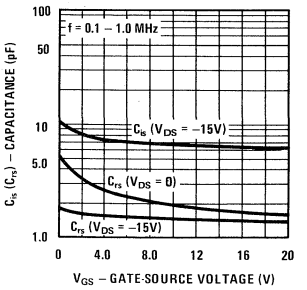
Transconductance vs Drain Current



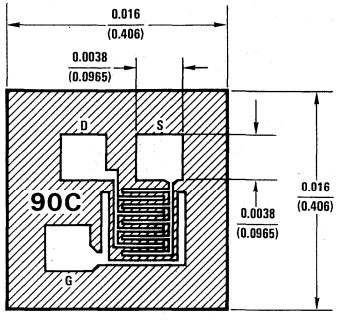
Noise Voltage vs Frequency



Capacitance vs Voltage



Process 90 N-Channel JFET



GATE IS ALSO BACKSIDE CONTACT

DESCRIPTION

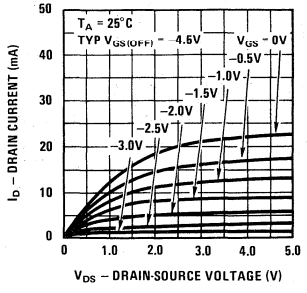
Process 90 is designed for VHF/UHF mixer/amplifier and applications where Process 50 is not adequate. Has sufficient gain and low noise, common gate configuration at 450 MHz, for sensitive receivers. The high transconductance and square law characteristics insures low crossmodulation and intermodulation distortions. Common-gate operation simplifies circuitry. Consider Process 92 for even higher performance.

CHARACTERISTIC	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Gate-Source Breakdown Voltage	BV_{GSS}	V_{DS} = 0V, I_G = −1 μA	−20	−30		V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 10V, V_{GS} = 0	3	18	40	mA
Forward Transconductance	g_{fs}	V_{DS} = 10V, V_{GS} = 0	5.5	8.0	10	mmhos
Forward Transconductance	g_{fs}	V_{DS} = 10V, I_D = 5 mA	4.5	5.8		mmhos
Reverse Gate Current	I_{GSS}	V_{GS} = −15V, V_{DS} = 0		−5.0	−100	pA
"ON" Resistance	r_{DS}	V_{DS} = 100 mV, V_{GS} = 0		90		Ω
Pinch Off Voltage	$V_{GS(OFF)}$	V_{DS} = 10V, I_D = 1 nA	−1.5	−3.5	−6.0	V
Output Conductance	g_{os}	V_{DG} = 10V, I_D = 5 mA		45	100	μmhos
Feedback Capacitance	C_{rs}	V_{DG} = 10V, I_D = 5 mA		1.0	1.2	pF
Input Capacitance	C_{is}	V_{DG} = 10V, I_D = 5 mA		4.0	5.0	pF
Noise Voltage	e_n	V_{DG} = 10V, I_D = 5 mA, f = 100 Hz		13		$nV/\sqrt{Hz}$
Noise Figure	NF	V_{DG} = 10V, I_D = 5 mA, f = 450 MHz		3.0		dB
Power Gain	G_{pg} (CG)	V_{DG} = 10V, I_D = 5 mA, f = 450 MHz		11		dB

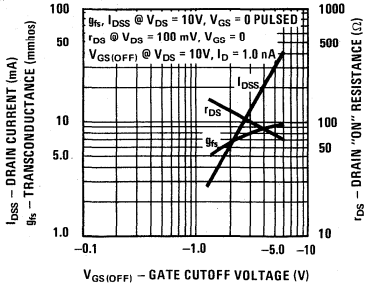
This process is available in the following device types. *Denotes preferred parts.

TO-52 (CASE 07)	TO-72 (CASE 25)	TO-92 (CASE 72)	TO-92 (CASE 77)
U312	*2N5397	J114	*2N5245
	2N5398	*J210	*2N5246
		*J211	*2N5247
		*J212	
		*J300	

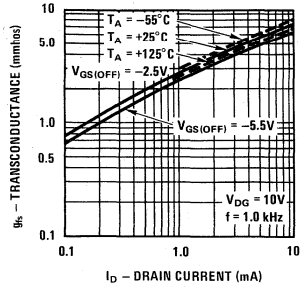
Common Drain-Source Characteristics



Parameter Interactions



Transconductance vs Drain Current

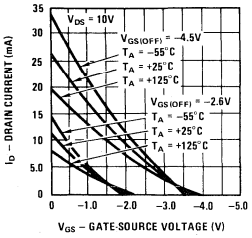


Process 90

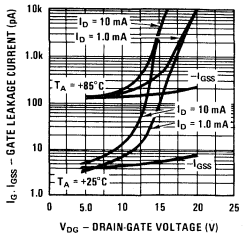
COMMON SOURCE

COMMON GATE

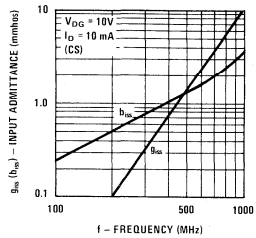
Transfer Characteristics



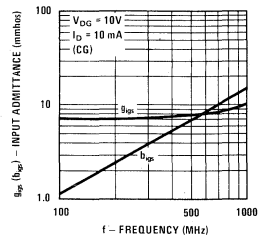
Leakage Current vs Voltage



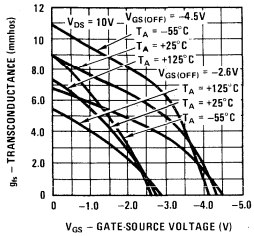
Input Admittance



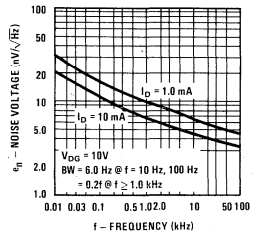
Input Admittance



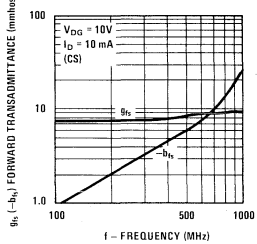
Transfer Characteristics



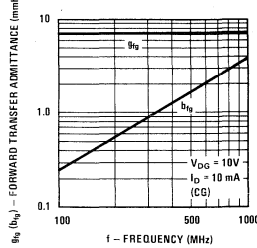
Noise Voltage vs Frequency



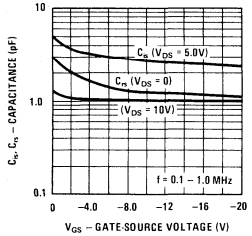
Forward Transadmittance



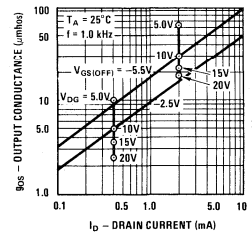
Forward Transadmittance



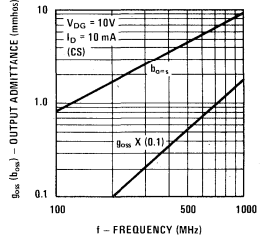
Capacitance vs Voltage



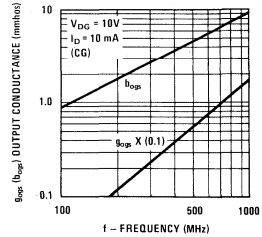
Output Conductance vs Drain Current



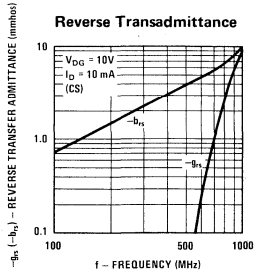
Output Admittance



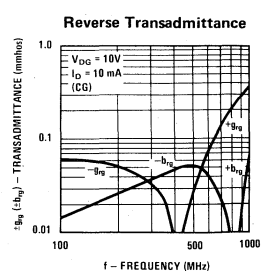
Output Admittance



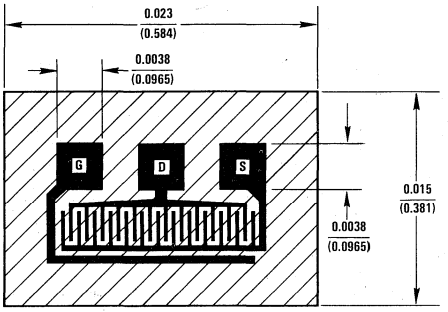
Reverse Transadmittance



Reverse Transadmittance



Process 92 N-Channel Junction Match



GATE IS ALSO BACKSIDE CONTACT

DESCRIPTION

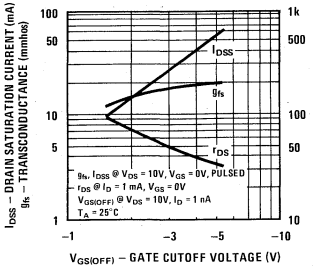
Process 92 is designed for VHF/UHF amplifier, oscillator, and mixer applications. As a common gate amplifier, 16 dB at 100 MHz and 12 dB at 450 MHz can be realized. Worst case 75 ohm input impedance provides ideal input match.

CHARACTERISTIC	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Gate-Source Breakdown Voltage	BV_{GSS}	V_{DS} = 0V, I_G = −1 μA	−20	−30		V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 10V, V_{GS} = 0, Pulsed	10	38	80	mA
Forward Trans-conductance	g_{fs}	V_{DS} = 10V, V_{GS} = 0, Pulsed		19		mmhos
Forward Trans-conductance	g_{fs}	V_{DG} = 10V, I_D = 10 mA	10	13	18	mmhos
Reverse Gate Current	I_{GSS}	V_{GS} = −15V, V_{DS} = 0		−15	−100	pA
"ON" Resistance	r_{DS}	V_{DS} = 100 mV, V_{GS} = 0	35	45	80	Ω
Pinch Off Voltage	$V_{GS(OFF)}$	V_{DS} = 10V, I_D = 1 nA	−1.5	−4.0	−6.5	V
Output Conductance	g_{os}	V_{DG} = 10V, I_D = 10 mA		160	250	μmhos
Feedback Capacitance	C_{gd}	V_{DG} = 10V, I_D = 10 mA, f = 1 MHz		2.0	2.5	pF
Input Capacitance	C_{gs}	V_{DG} = 10V, I_D = 10 mA, f = 1 MHz		4.1	5.0	pF
Noise Voltage	e_n	V_{DG} = 10V, I_D = 10 mA, f = 100 Hz		6.0		$nV/\sqrt{Hz}$
Noise Figure	NF	V_{DG} = 10V, I_D = 10 mA, f = 450 MHz		3.0		dB
Power Gain	G_{pg}	V_{DG} = 10V, I_D = 10 mA, f = 450 MHz		12		dB

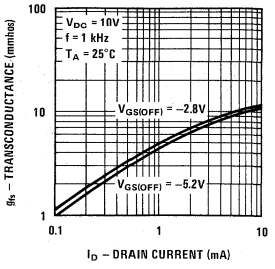
This process is available in the following device types. *Denotes preferred parts.

TO-52 (CASE 07)	TO-99 (CASE 24)	TO-92 (CASE 72)
U308	U430	J308
*U309	U431	*J309
*U310		*J310

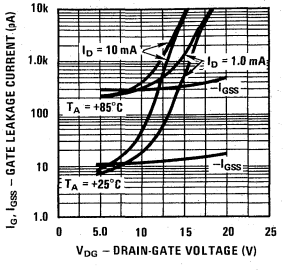
Parameter Interactions



Transconductance vs Drain Current

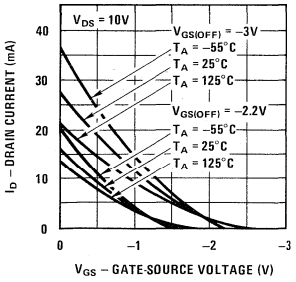


Leakage Current vs Voltage

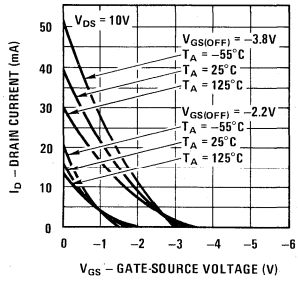


Process 92

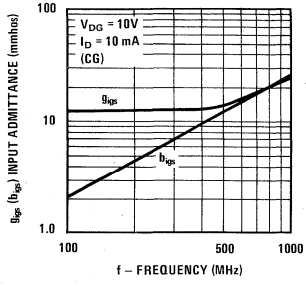
Transfer Characteristics



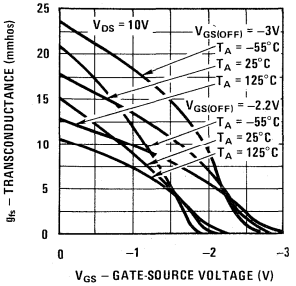
Transfer Characteristics



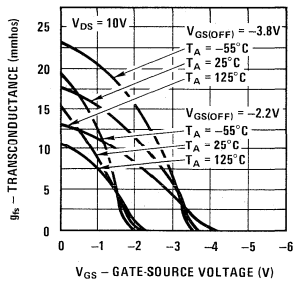
Input Admittance



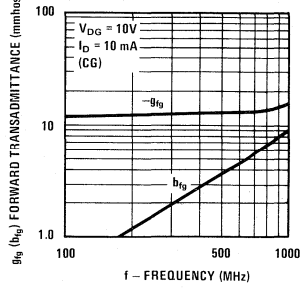
Transfer Characteristics



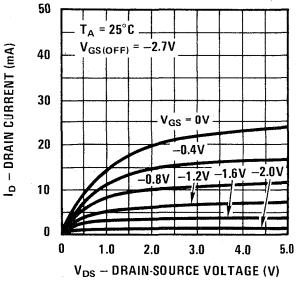
Transfer Characteristics



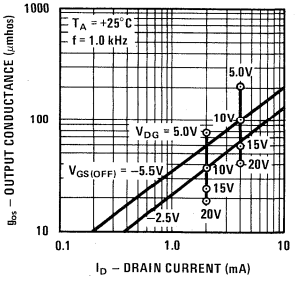
Forward Transadmittance



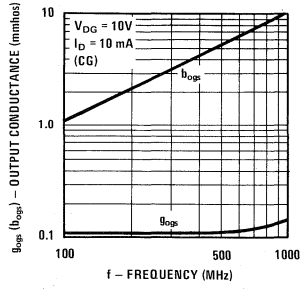
Common Drain-Source Characteristics



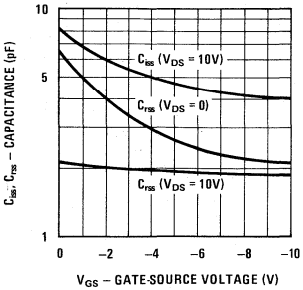
Output Conductance vs Drain Current



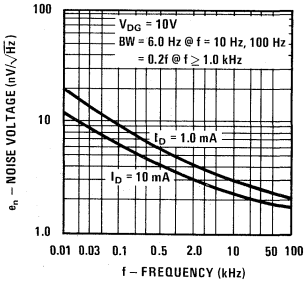
Output Admittance



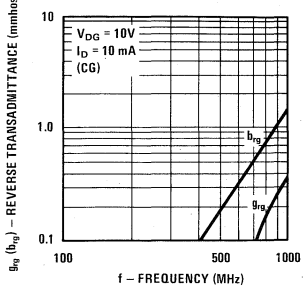
Capacitance vs Voltage



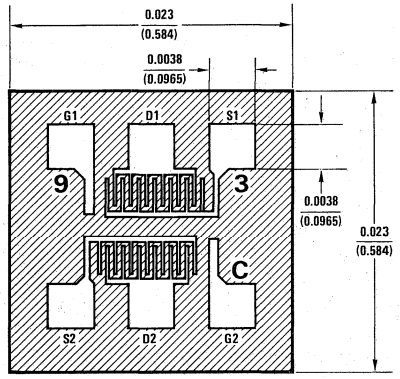
Noise Voltage vs Frequency



Reverse Transadmittance



Process 93 N-Channel JFET



DESCRIPTION

Process 93 is a monolithic dual JFET with a diode isolated substrate. It is intended for wide band, low noise, single ended video amplifier input stages, and high slew rate op amps. Monolithic structure eliminates thermal transient errors, and provides freedom to pick operating current and voltage.

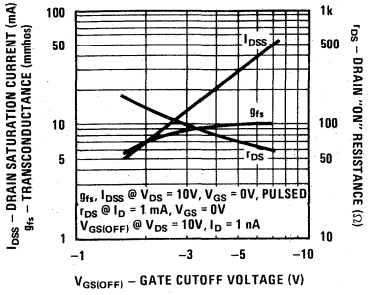
CHARACTERISTIC	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Gate-Source Breakdown Voltage	BV_{GSS}	V_{DS} = 0V, I_G = −1 μA	−25	−30		V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 10V, V_{GS} = 0, Pulsed	3.0	18	40	mA
Forward Transconductance	g_{fs}	V_{DS} = 10V, V_{GS} = 0, Pulsed		8.0		mmhos
Forward Transconductance	g_{fs}	V_{DG} = 10V, I_D = 5 mA	5.0	6.0	10	mmhos
Output Conductance	g_{os}	V_{DG} = 10V, I_D = 5 mA		50	100	μmhos
Pinch Off Voltage	$V_{GS(OFF)}$	V_{DS} = 10V, I_D = 1 nA	−1.5	−3.5	−6.0	V
"ON" Resistance	r_{DS}	V_{DS} = 100 mV, V_{GS} = 0		100		Ω
Gate Current	I_G	V_{DG} = 10V, I_D = 5 mA		10	100	pA
Noise Voltage	e_n	V_{DG} = 10V, I_D = 5 mA, f = 100 Hz		9.0	30	$nV/\sqrt{Hz}$
Differential Match	$\lvert V_{GS1}-V_{GS2}\rvert$	V_{DG} = 10V, I_D = 5 mA		9.0	30	mV
Differential Match	ΔV_{GS1-2}	V_{DG} = 10V, I_D = 5 mA		15	40	μV/°C
Common Mode Rejection	CMRR	V_{DG} = 10V, I_D = 5 mA		90		dB
Feedback Capacitance	C_{rs}	V_{DG} = 10V, I_D = 5 mA, f = 1 MHz		1.0	1.2	pF
Input Capacitance	C_{is}	V_{DG} = 10V, I_D = 5 mA, f = 1 MHz		4.2	5.0	pF

This process is available in the following device types. *Denotes preferred parts.

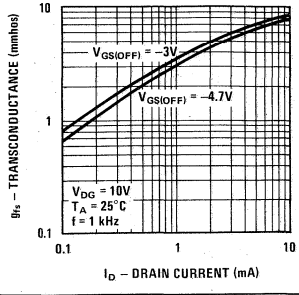
TO-78 (CASE 24)

*2N5911
*2N5912
U257

Parameter Interactions

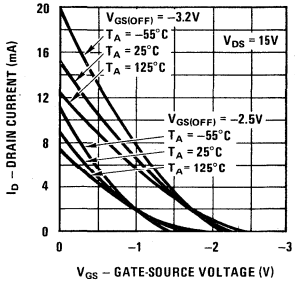


Transconductance vs Drain Current

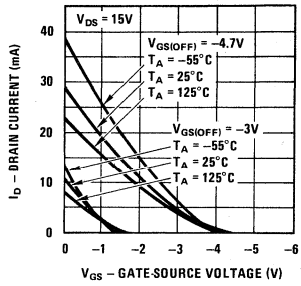


Process 93

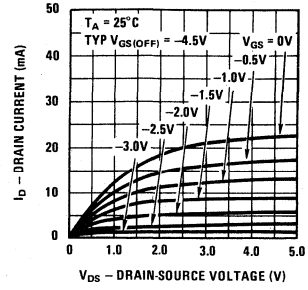
Transfer Characteristics



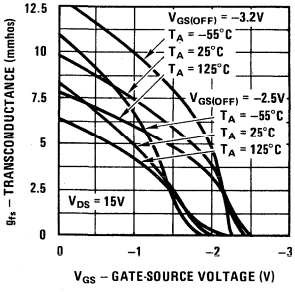
Transfer Characteristics



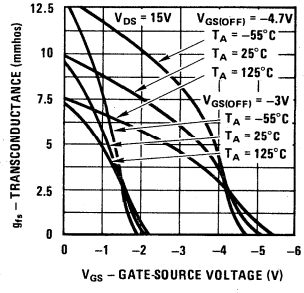
Common Drain-Source Characteristics



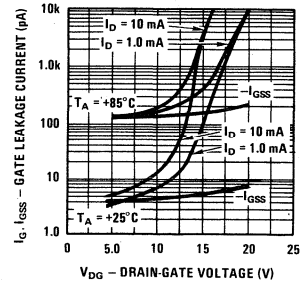
Transfer Characteristics



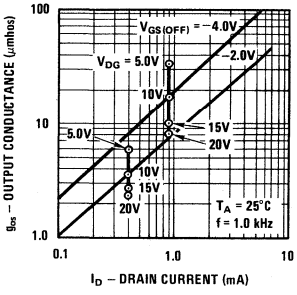
Transfer Characteristics



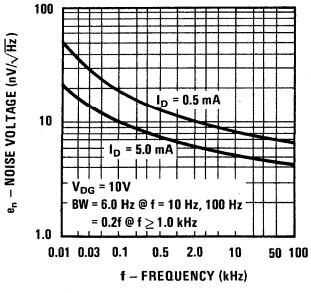
Leakage Current vs Voltage



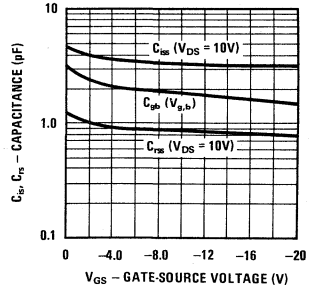
Output Conductance vs Drain Current



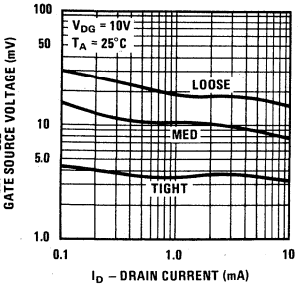
Noise Voltage vs Frequency



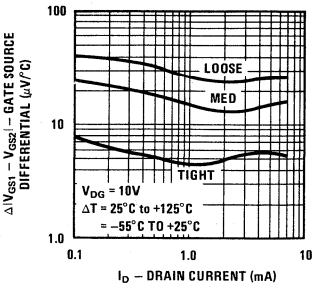
Capacitance vs Voltage



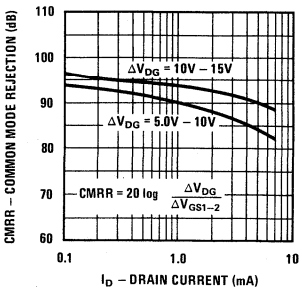
Differential Offset



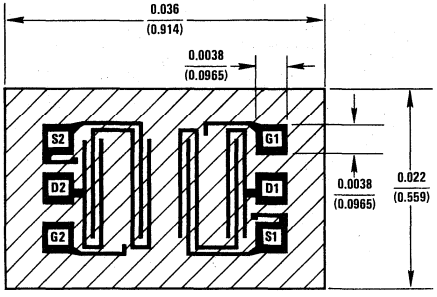
Differential Drift



CMRR vs Drain Current



Process 94 N-Channel JFET



DESCRIPTION

Process 94 is a monolithic dual JFET. It is strictly intended for operational amplifier input buffer applications. Special processing results in extremely low input bias current and virtually unmeasureable offset current. It is important to note that the <5 pico ampere bias current is measured at 35 volts. Typical CMRR is 125 dB. Performance superior to electrometer tubes can be readily achieved with low offset voltage and almost zero long term drift.

CHARACTERISTIC	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Gate-Source Breakdown Voltage	BV_{GSS}	V_{DS} = 0V, I_G = −1 μA	−40	−70		V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 15V, V_{GS} = 0	0.5	3.0	10	mA
Forward Transconductance	g_{fs}	V_{DS} = 15V, V_{GS} = 0	1.5	3.5	7.0	mmho
Forward Transconductance	g_{fs}	V_{DG} = 15V, I_D = 0.2 mA	0.9	1.2	1.8	mmhos
Pinch Off Voltage	$V_{GS(OFF)}$	V_{DS} = 15V, I_D = 1 nA	−0.5	−2.0	−6.0	V
Gate Current	I_G	V_{DG} = 35V, I_D = 0.20 mA		1.0	15	pA
Feedback Capacitance	C_{rss}	V_{DS} = 15V, V_{GS} = 0, f = 1 MHz		0.01	0.02	pF
Input Capacitance	C_{iss}	V_{DS} = 15V, V_{GS} = 0, f = 1 MHz		4.0	5.0	pF
Noise Voltage	e_n	V_{DG} = 15V, I_D = 0.2 mA, f = 10 Hz		12	50	$nV/\sqrt{Hz}$
Output Conductance	g_{os}	V_{DG} = 15V, I_D = 0.2 mA		<0.1		μmhos
Differential Match	$\|V_{GS1}-V_{GS2}\|$	V_{DG} = 15V, I_D = 0.2 mA		5.0	25	mV
Differential Match	ΔV_{GS1-2}	V_{DG} = 15V, I_D = 0.2 mA		6.0	50	μV/°C
Common Mode Rejection	CMRR	V_{DG} = 15V, I_D = 0.2 mA		125		dB

This process is available in the following device types.
*Denotes preferred parts.

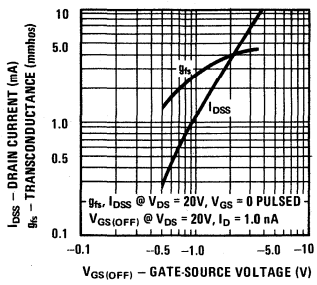
TO-71 (CASE 12)

*NDF9406
*NDF9407
*NDF9408
*NDF9409
*NDF9410

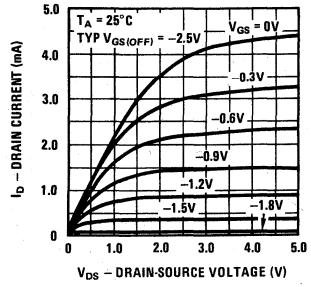
TO-78 (CASE 24)

NDF9401
NDF9402
NDF9403
NDF9404
NDF9405

Parameter Interactions

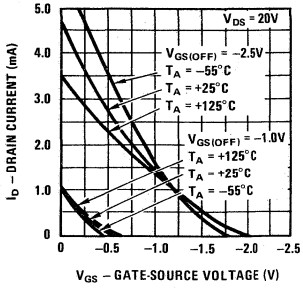


Common Drain-Source Characteristics

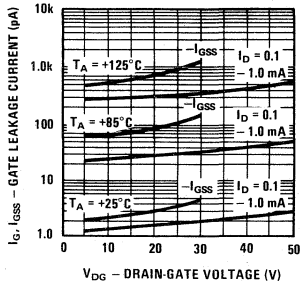


Process 94

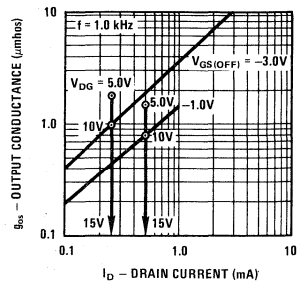
Transfer Characteristics



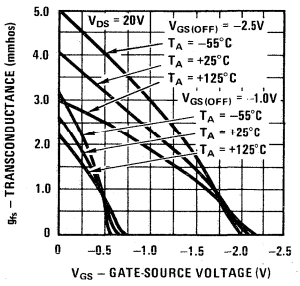
Leakage Current vs Voltage



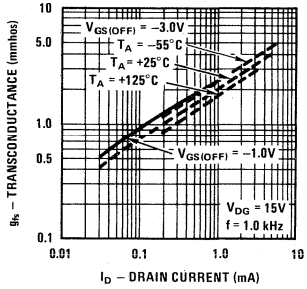
Output Conductance vs Drain Current



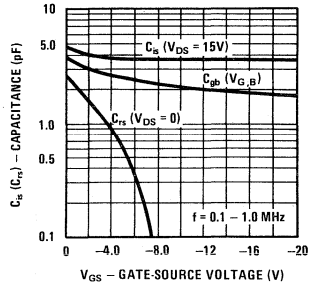
Transfer Characteristics



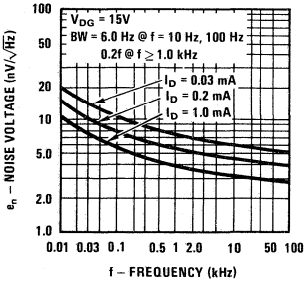
Transconductance vs Drain Current



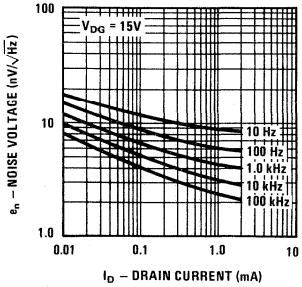
Capacitance vs Voltage



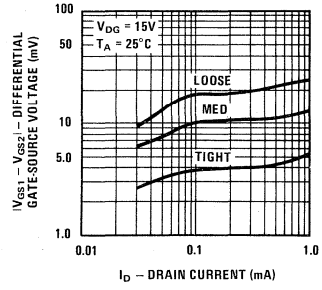
Noise Voltage vs Frequency



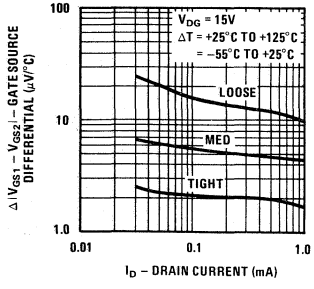
Noise Voltage vs Current



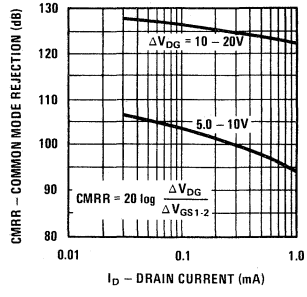
Differential Offset



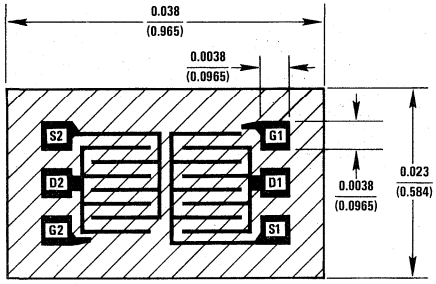
Differential Drift



CMRR vs Drain Current



Process 95 N-Channel JFET



DESCRIPTION

Process 95 is a monolithic dual JFET with a diode isolated substrate. It is intended for operational amplifier input buffer applications. Processing results in low input bias current and virtually unmeasureable offset current. Low noise voltage and high CMRR for critical I/f applications.

CHARACTERISTIC	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Gate-Source Breakdown Voltage	BV_{GSS}	V_{DS} = 0V, I_G = −1 μA	−40	−70		V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 15V, V_{GS} = 0	0.5	3.0	8.0	mA
Forward Transconductance	g_{fs}	V_{DS} = 15V, V_{GS} = 0	1.0	2.5	4.0	mmhos
Forward Transconductance	g_{fs}	V_{DG} = 15V, I_D = 0.2 mA	0.5	0.7		mmhos
Gate Leakage	I_{GSS}	V_{GS} = −20V, V_{DS} = 0		−5.0	−100	pA
Pinch Off Voltage	$V_{GS(OFF)}$	V_{DS} = 15V, I_D = 1 nA	−0.5	−2.5	−4.0	V
Input Capacitance	C_{iss}	V_{DS} = 15V, V_{GS} = 0, f = 1 MHz		10	14	pF
Noise Voltage	e_n	V_{DS} = 15V, I_D = 0.2 mA, f = 10 Hz		8.0	30	$nV/\sqrt{Hz}$
Noise Voltage	e_n	V_{DS} = 15V, I_D = 0.2 mA, f = 100 Hz		6.0	10	$nV/\sqrt{Hz}$
Output Conductance	g_{os}	V_{DG} = 15V, I_D = 0.2 mA		0.3	1.0	μmhos
Feedback Capacitance	C_{rss}	V_{DS} = 15V, V_{GS} = 0, f = 1 MHz		3.5	5.0	pF
Differential Match	$\|V_{GS1}-V_{GS2}\|$	V_{DG} = 20V, I_D = 0.2 mA		6.0	25	mV
Differential Match	ΔV_{GS1-2}	V_{DG} = 20V, I_D = 0.2 mA		9.0	60	μV/°C
Common Mode Rejection	CMRR	V_{DG} = 20V, I_D = 0.2 mA	86	115		dB

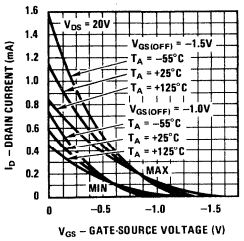
This process is available in the following device types. *Denotes preferred parts.

TO-71 (CASE 12)

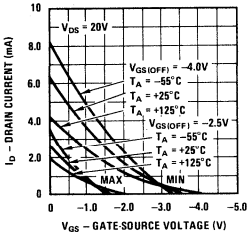
2N5515	*2N5522
2N5516	*2N5523
2N5517	*2N5524
2N5518	*2N6483
2N5519	*2N6484
*2N5520	*2N6485
*2N5521	

Process 95

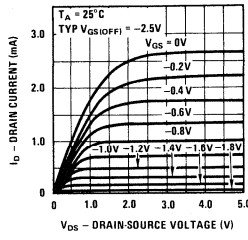
Transfer Characteristics



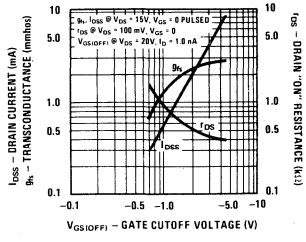
Transfer Characteristics



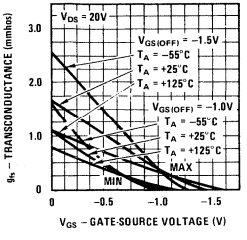
Common Drain-Source Characteristics



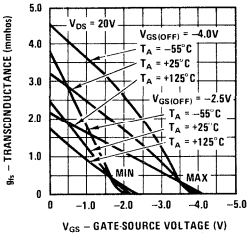
Parameter Interactions



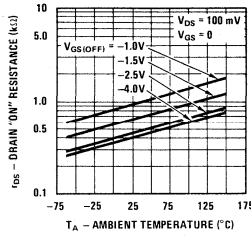
Transconductance Characteristics



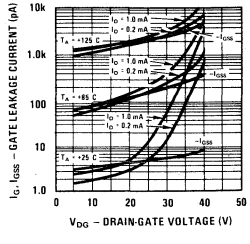
Transconductance Characteristics



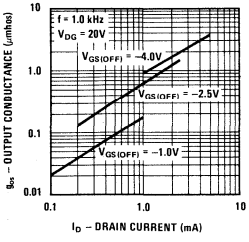
Channel Resistance vs Temperature



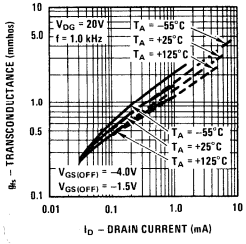
Leakage Current vs Voltage



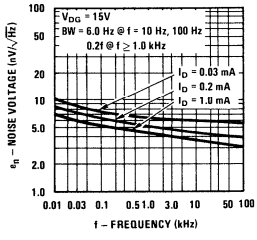
Output Conductance vs Drain Current



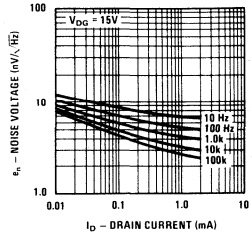
Transconductance vs Drain Current



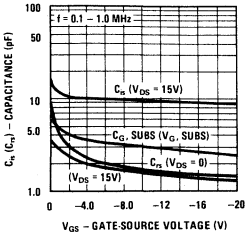
Noise Voltage vs Frequency



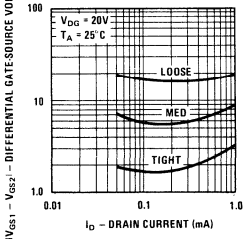
Noise Voltage vs Current



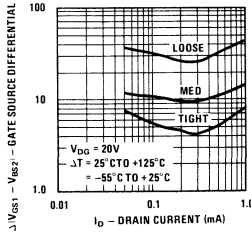
Capacitance vs Voltage



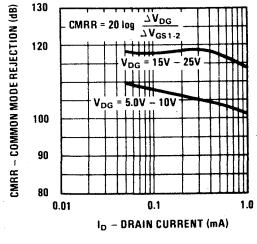
Differential Offset



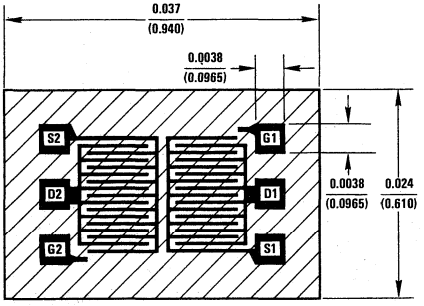
Differential Drift



CMRR vs Drain Current



Process 96 N-Channel JFET



DESCRIPTION

Process 96 is a monolithic dual JFET with a diode isolated substrate. It is intended for wide band, low noise, single ended video amplifier input stages. Also ideal for matched voltage variable resistor applications over 60 dB tracking range.

CHARACTERISTIC	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Gate-Source Breakdown Voltage	BV_{GSS}	V_{DS} = 0V, I_G = −1 μA	−40	−55		V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 15V, V_{GS} = 0	5.0	15	30	mA
Forward Transconductance	g_{fs}	V_{DS} = 15V, V_{GS} = 0	9.0	18	30	mmhos
Forward Transconductance	g_{fs}	V_{DG} = 15V, I_D = 2 mA	7.5	9.0		mmhos
Output Conductance	g_{os}	V_{DG} = 15V, I_D = 2 mA		15	45	μmhos
Pinch Off Voltage	$V_{GS(OFF)}$	V_{DS} = 15V, I_D = 1 nA		−1.8	−3.0	V
"ON" Resistance	r_{DS}	V_{DS} = 100 mV, V_{GS} = 0	35	70	120	Ω
Gate Current	I_{GSS}	V_{GS} = −20V, V_{DS} = 0		−8.0	−100	pA
Gate Current	I_G	V_{DG} = 15V, I_D = 2 mA		15	200	pA
Noise Voltage	e_n	V_{DG} = 15V, I_D = 2 mA, f = 100 Hz		4.5	10	$nV/\sqrt{Hz}$
Feedback Capacitance	C_{rs}	V_{DG} = 15V, I_D = 2 mA, f = 1 MHz		2.5	3.0	pF
Input Capacitance	C_{is}	V_{DG} = 15V, I_D = 2 mA, f = 1 MHz		10	12	pF
Differential Voltage	$\lvert V_{GS1}-V_{GS2}\rvert$	V_{DG} = 15V, I_D = 2 mA		8.0	25	mV
Differential Voltage	ΔV_{GS}	V_{DG} = 15V, I_D = 2 mA		9.0	50	μV/°C
Common Mode Rejection	CMRR	V_{DG} = 15V, I_D = 2 mA	76	95		dB

This process is available in the following device types. *Denotes preferred parts.

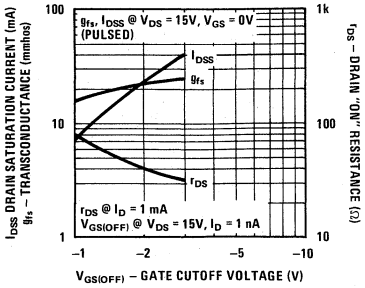
TO-71 (CASE 12)

*2N5564
*2N5565
*2N5566

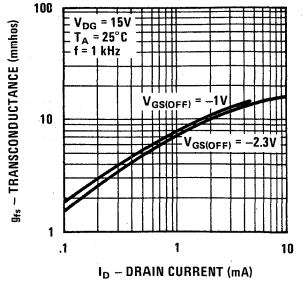
8-Pin DIP (CASE 67)

*NPD5564
*NPD5565
*NPD5566

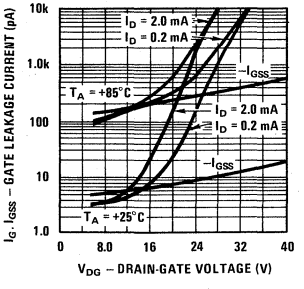
Parameter Interactions



Transconductance vs Drain Current

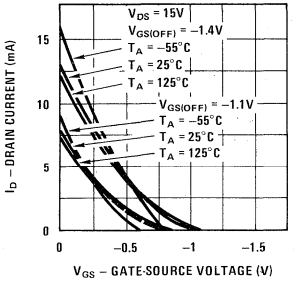


Leakage Current vs Voltage

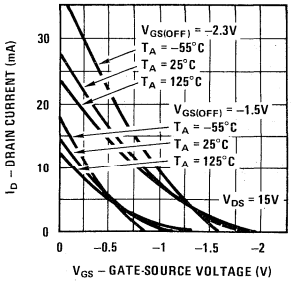


Process 96

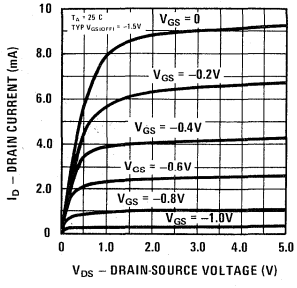
Transfer Characteristics



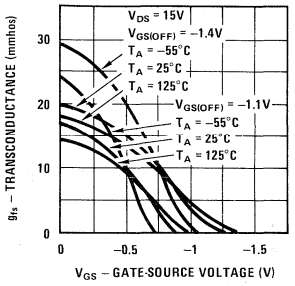
Transfer Characteristics



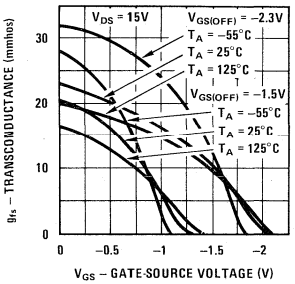
Common Drain-Source Characteristics



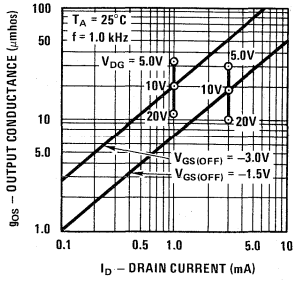
Transfer Characteristics



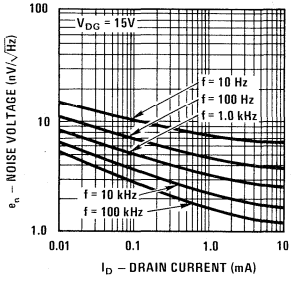
Transfer Characteristics



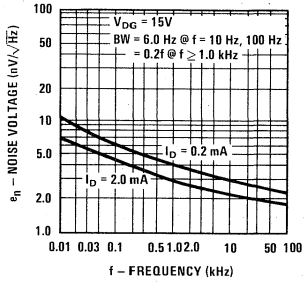
Output Conductance vs Drain Current



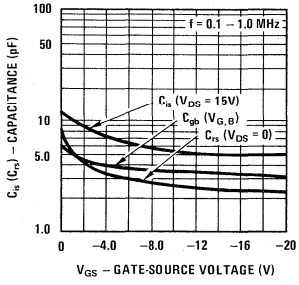
Noise Voltage vs Current



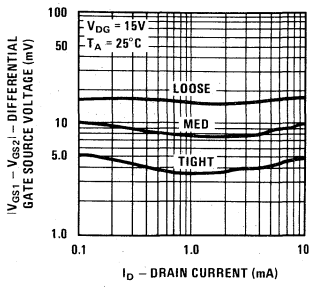
Noise Voltage vs Frequency



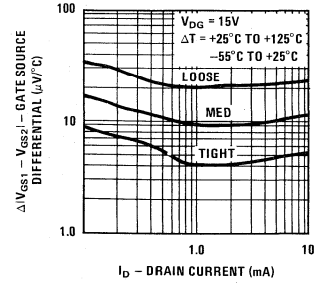
Capacitance vs Voltage



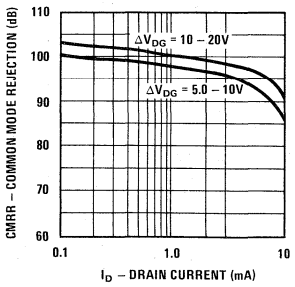
Differential Offset



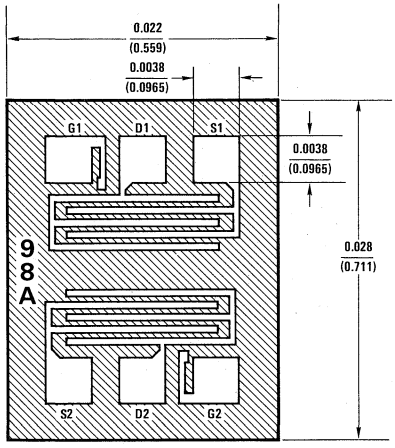
Differential Drift



CMRR vs Drain Current



Process 98 N-Channel JFET



DESCRIPTION

Process 98 is a high gain, general purpose, monolithic dual JFET with a diode isolated substrate. It is intended for amplifier input stages requiring high gain, low noise and low offset drift over temperature. Strict processing controls result in low input bias currents and virtually immeasurable offset currents. Matching characteristics are essentially independent of operating current and voltage.

This process is available in the following device types. *Denotes preferred parts.

TO-71 (CASE 12)

2N5561
2N5562
2N5563
U401
U402
U403
U404
U405
U406

8-Pin DIP (CASE 60)

J401
J402
J403
J404
J405
J406

PROCESS IN DEVELOPMENT

Section 4

Preferred Parts Data Sheets

4

2N3684-87/PN3684-87 N-Channel JFETs

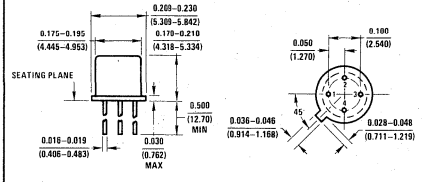
General Description

The 2N3684/PN3684 thru 2N3687/PN3687 series of N-channel JFETs is characterized for general purpose small signal amplifier applications requiring low noise and tightly specified I_{DSS} ranges.

Absolute Maximum Ratings (25°C)

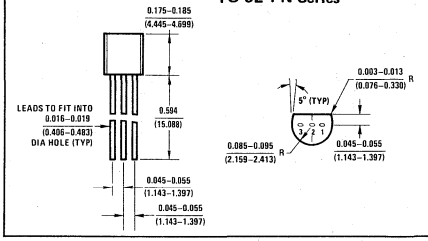
Gate-Drain or Gate-Source Voltage (Note 2)	−50V
Gate Current or Drain Current	50 mA
Total Device Dissipation (Derate 2 mW/°C to 175°C)	350 mW
Storage Temperature Range	
2N Series	−65°C to +200°C
PN Series	−65°C to +150°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-72 2N Series



PIN	FET
1	S
2	D
3	G
4	Case

TO-92 PN Series



PIN	FET
1	G
2	S
3	D

Electrical Characteristics (25°C unless otherwise noted)

PARAMETER		CONDITIONS		2N3684/ PN3684		2N3685/ PN3685		2N3686/ PN3686		2N3687/ PN3687		UNITS
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
I_{GSS}	Gate Reverse Current	V_{GS} = −30V, V_{DS} = 0			−0.1		−0.1		−0.1		−0.1	nA
			150°C		−0.5		−0.5		−0.5		−0.5	μA
BV_{GSS}	Gate-Source Breakdown Voltage	I_G = −1 μA, V_{DS} = 0		−50		−50		−50		−50		V
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 20V, I_D = 1 nA		−2	−5	−1	−3.5	−0.6	−2	−0.3	−1.2	
I_{DSS}	Saturation Drain Current	V_{DS} = 20V, V_{GS} = 0		2.5	7.5	1	3	0.4	1.2	0.1	0.5	mA
$r_{DS(on)}$	Drain-Source ON Resistance	V_{DS} = 0V, V_{GS} = 0, (Note 1)			600		800		1200		2400	Ω
g_{fs}	Common-Source Forward Transconductance, (Note 3)	V_{DS} = 20V, V_{GS} = 0	f = 1 kHz	2000	3000	1500	2500	1000	2000	500	1500	μmho
g_{os}	Common-Source Output Conductance				50		25		10		5	
C_{rss}	Common-Source Reverse Transfer Capacitance				1.2		1.2		1.2		1.2	pF
C_{iss}	Common-Source Input Capacitance				4		4		4		4	
e_n	Equivalent Short-Circuit Input Spot Noise Voltage	V_{DS} = 10V, V_{GS} = 0	f = 20 Hz		0.15		0.15		0.15		0.15	$\frac{\mu V}{\sqrt{Hz}}$
NF	Noise Figure	V_{DS} = 10V, V_{GS} = 0, R_{gen} = 10M, BW = 6 Hz	f = 100 Hz		0.5		0.5		0.5		0.5	dB

Note 1: Not JEDEC registered data.
Note 2: Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
Note 3: Pulse test duration: 2 ms.

2N3954-55/2N3954A-55A N-Channel Monolithic Dual JFETs

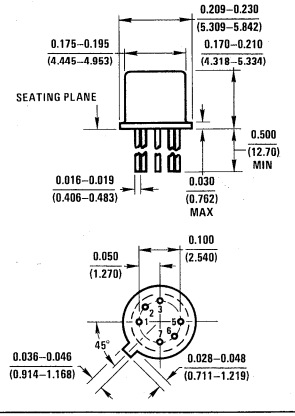
General Description

The 2N3954 thru 2N3955/A series of N-channel monolithic dual JFETs is designed for low to medium frequency differential amplifier applications requiring low noise, high common-mode rejection, and very tight match.

Absolute Maximum Ratings (25°C)

Gate-Drain or Gate-Source Voltage		−50V
Gate-to-Gate Voltage		±50V
Gate Current		50 mA
Total Device Dissipation 85°C	(Each Side)	250 mW
Case Temperature	(Both Sides)	500 mW
Power Derating (Each Side)		2.86 mW/°C
(Both Sides)		4.3 mW/°C
Storage Temperature Range		−65°C to +200°C
Lead Temperature (1/16" from case for 10 seconds)		300°C

TO-71



PIN	FET (12)
1	S1
2	D1
3	G1
5	S2
6	D2
7	G2

Electrical Characteristics (25°C unless otherwise noted)

PARAMETER		CONDITIONS		2N3954		2N3954A		2N3955		2N3955A		UNITS
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
I_{GSS}	Gate Reverse Current	V_{GS} = −30V, V_{DS} = 0			−100		−100		−100		−100	pA
			T_A = 125°C		−500		−500		−500		−500	nA
BV_{GSS}	Gate-Source Breakdown Voltage	V_{DS} = 0, I_G = −1 μA		−50		−50		−50		−50		V
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 20V, I_D = 1 nA		−1.0	−4.5	−1.0	−4.5	−1.0	−4.5	−1.0	−4.5	
$V_{GS(f)}$	Gate-Source Forward Voltage	V_{DS} = 0, I_G = 1 mA			2.0		2.0		2.0		2.0	
V_{GS}	Gate-Source Voltage	V_{DS} = 20V	I_D = 50 μA		−4.2		−4.2		−4.2		−4.2	
			I_D = 200 μA	−0.5	−4.0	−0.5	−4.0	−0.5	−4.0	−0.4	−4.0	
I_G	Gate Operating Current	V_{DS} = 20V, I_D = 200 μA			−50		−50		−50		−50	pA
			T_A = 125°C		−250		−250		−250		−250	nA
I_{DSS}	Saturation Drain Current	V_{DS} = 20V, V_{GS} = 0		0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	mA
g_{fs}	Common-Source Forward Transconductance	V_{DS} = 20V, V_{GS} = 0	f = 1 kHz	1000	3000	1000	3000	1000	3000	1000	3000	μmho
			f = 200 MHz	1000		1000		1000		1000		
g_{os}	Common-Source Output Conductance		f = 1 kHz		35		35		35		35	
C_{iss}	Common-Source Input Capacitance		f = 1 MHz		4.0		4.0		4.0		4.0	pF
C_{rss}	Common-Source Reverse Transfer Capacitance				1.2		1.2		1.2		1.2	
C_{dgo}	Drain-Gate Capacitance	V_{DG} = 10V, I_S = 0			1.5		1.5		1.5		1.5	
NF_f	Common Source Spot Noise Figure	V_{DS} = 20V, V_{GS} = 0, R_G = 10 MΩ	f = 100 Hz		0.5		0.5		0.5		0.5	dB
$\lvert I_{G1}-I_{G2}\rvert$	Differential Gate Current	V_{DS} = 20V, I_D = 200 μA	T = 125°C		10		10		10		10	nA
I_{DSS1}/I_{DSS2}	Drain Saturation Current Ratio	V_{DS} = 20V, V_{GS} = 0		0.95	1.0	0.95	1.0	0.95	1.0	0.95	1.0	
$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage	V_{DS} = 20V, I_D = 200 μA			5.0		5.0		10.0		5.0	mV
$\Delta\lvert V_{GS1}-V_{GS2}\rvert$	Gate-Source Differential Voltage Change with Temperature		T = 25°C to −55°C		0.8		0.4		2.0		1.2	
			T = 25°C to 125°C		1.0		0.5		2.5		1.5	
g_{fs1}/g_{fs2}	Transconductance Ratio		f = 1 kHz	0.97	1.0	0.97	1.0	0.97	1.0	0.95	1.0	

2N3956-58 N-Channel Monolithic Dual JFETs

General Description

The 2N3956 thru 2N3958 series of N-channel monolithic dual JFETs is designed for low to medium frequency differential amplifier applications requiring tight match, low noise and high common-mode rejection.

Absolute Maximum Ratings (25°C)

Gate-Drain or Gate-Source Voltage	−50V
Gate-to-Gate Voltage	±50V
Gate Current	50 mA
Total Device Dissipation 85°C (Each Side)	250 mW
Case Temperature (Both Sides)	500 mW
Power Derating (Each Side)	2.86 mW/°C
(Both Sides)	4.3 mW/°C
Storage Temperature Range	−65°C to +200°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

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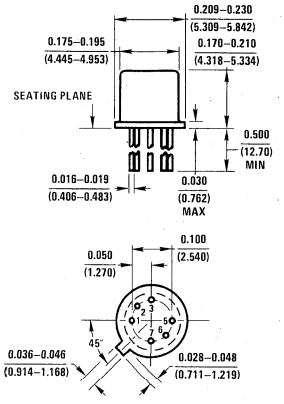


PIN	FET (12)
1	S1
2	D1
3	G1
5	S2
6	D2
7	G2

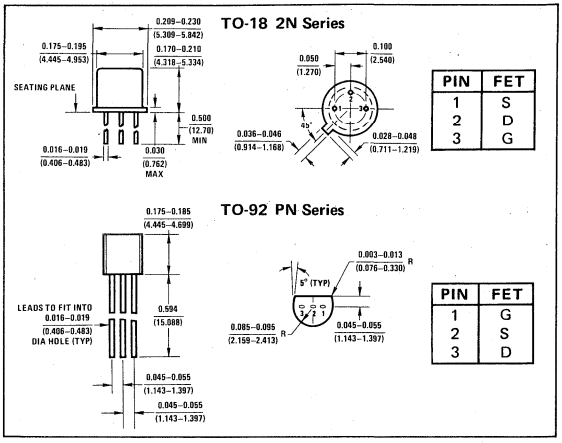
Electrical Characteristics (25°C unless otherwise noted)

PARAMETER		CONDITIONS		2N3956		2N3957		2N3958		UNITS
				MIN	MAX	MIN	MAX	MIN	MAX	
I_{GSS}	Gate Reverse Current	V_{GS} = −30V, V_{DS} = 0			−100		−100		−100	pA
			T_A = 150°C		−500		−500		−500	nA
BV_{GSS}	Gate-Source Breakdown Voltage	V_{DS} = 0V, I_G = −1 μA		−50		−50		−50		V
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 20V, I_D = 1 nA		−1.0	−4.5	−1.0	−4.5	−1.0	−4.5	V
$V_{GS(f)}$	Gate-Source Forward Voltage	V_{DS} = 0V, I_G = 1 mA			2.0		2.0		2.0	V
V_{GS}	Gate-Source Voltage	V_{DS} = 20V, I_D = 50 μA			−4.2		−4.2		−4.2	V
		V_{DS} = 20V, I_D = 200 μA		−0.5	−4.0	−0.5	−4.0	−0.5	−4.0	V
I_G	Gate Operating Current	V_{DS} = 20V, I_D = 200 μA			−50		−50		−50	pA
			T_A = 125°C		−250		−250		−250	nA
I_{DSS}	Saturation Drain Current	V_{DS} = 20V, V_{GS} = 0		0.5	5.0	0.5	5.0	0.5	5.0	mA
$\|y_{fs}\|$	Common-Source Forward Transconductance	V_{DS} = 20V, V_{GS} = 0	f = 1 kHz	1000	3000	1000	3000	1000	3000	μmho
			f = 200 MHz	1000		1000		1000		μmho
g_{os}	Common-Source Output Conductance		f = 1 kHz		35		35		35	μmho
C_{iss}	Common-Source Input Capacitance		f = 1 MHz		4.0		4.0		4.0	pF
C_{rss}	Common-Source Reverse Transfer Capacitance				1.2		1.2		1.2	pF
C_{dgo}	Drain-Gate Capacitance	V_{DG} = 10V, I_S = 0			1.5		1.5		1.5	pF
NF	Common-Source Spot Noise Figure	V_{DS} = 20V, V_{GS} = 0, R_G = 10 MΩ	f = 100 Hz		0.5		0.5		0.5	dB
$\|I_{G1}-I_{G2}\|$	Differential Gate Reverse Current	V_{DS} = 20V, I_D = 200 μA	T = 125°C		10		10		10	nA
I_{DSS1}/I_{DSS2}	Saturation Drain Current Ratio	V_{DS} = 20V, V_{GS} = 0		0.95	1.0	0.90	1.0	0.85	1.0	
$\|V_{GS1}-V_{GS2}\|$	Differential Gate-Source Voltage	V_{DS} = 20V, I_D = 200 μA			15		20		25	mV
$\Delta\|V_{GS1}-V_{GS2}\|$	Gate-Source Voltage Differential Change With Temperature		T = 25°C to −55°C		4.0		6.0		8.0	mV
			T = 25°C to 125°C		5.0		7.5		10.0	mV
g_{fs1}/g_{fs2}	Transconductance Ratio		f = 1 kHz	0.95	1.0	0.90	1.0	0.85	1.0	

2N4091-93/PN4091-93 N-Channel JFETs

General Description

The 2N4091/PN4091 thru 2N4093/PN4093 series of N-channel JFETs is characterized for analog switch applications requiring low ON resistance and moderate capacitance. This series is qualified for JAN, JANTX level processing per MIL-S-19500/431.



Absolute Maximum Ratings (25°C)

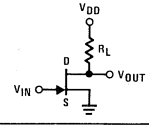
Reverse Gate-Drain or Gate-Source Voltage	−40V
Gate Current	10 mA
Total Device Dissipation at 25°C Case Temperature	
(Derate 10 mW/°C) 2N series	1.8 W
(Derate 3 mW/°C) PN Series, T_A = 25°C	350 mW
Storage Temperature Range	
2N series	−55°C to +200°C
PN series	−55°C to +150°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

Electrical Characteristics (25°C unless otherwise noted)

PARAMETER		CONDITIONS			2N4091/PN4091 MIN	2N4091/PN4091 MAX	2N4092/PN4092 MIN	2N4092/PN4092 MAX	2N4093/PN4093 MIN	2N4093/PN4093 MAX	UNITS
BV_{GSS}	Gate-Source Breakdown Voltage	I_G = −1 μA, V_{DS} = 0			−40		−40		−40		V
I_{DGO}	Drain Reverse Current	V_{GS} = −20V, I_S = 0		2N Series		200		200		200	pA
				PN Series		1		1		1	nA
				150°C		400		400		400	
$I_{D(off)}$	Drain Cutoff Current	V_{DS} = 20V	V_{GS} = −6V	2N Series						200	pA
				PN Series						1	nA
				150°C						400	
			V_{GS} = −8V	2N Series				200			pA
				PN Series				1			nA
				150°C				400			
			V_{GS} = −12V	2N Series		200					pA
				PN Series		1					nA
				150°C		400					
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 20V, I_D = 1 nA			−5	−10	−2	−7	−1	−5	V
I_{DSS}	Saturation Drain Current	V_{DS} = 20V, V_{GS} = 0, (Note 1)			30		15		8		mA
$V_{DS(on)}$	Drain-Source ON Voltage	V_{GS} = 0	I_D = 2.5 mA							0.2	V
			I_D = 4 mA					0.2			
			I_D = 6.6 mA			0.2					
$r_{DS(on)}$	Static Drain-Source ON Resistance	V_{GS} = 0, I_D = 1 mA				30		50		80	Ω
$r_{ds(on)}$	Drain Source ON Resistance	V_{GS} = 0, I_D = 0		f = 1 kHz		30		50		80	Ω
C_{iss}	Common-Source Input Capacitance	V_{DS} = 20V, V_{GS} = 0		f = 1 MHz		16		16		16	pF
C_{rss}	Common-Source Reverse Transfer Capacitance	V_{DS} = 0, V_{GS} = −20V				5		5		5	
t_d	Turn ON Delay Time	V_{DD} = 3V, $V_{GS(on)}$ = 0				15		15		20	ns
t_r	Rise Time		$I_{D(on)}$	$V_{GS(off)}$	R_L	10		20		40	
t_{off}	Turn OFF Time	2N/PN4091	6.6 mA	−12V	425 Ω	40		60		80	
		2N/PN4092	4 mA	−8V	770 Ω						
		2N/PN4093	2.5 mA	−6V	1120 Ω						

*JEDEC registered data

Note 1: Pulse width = 300 μs; duty cycle ≤ 3%.



Input Pulse
Rise time < 1 ns
Fall time < 1 ns
Pulse width = 1 μs
Pulse duty cycle ≤ 10%
Pulse generator impedance = 50 Ω

Sampling Scope
Rise time = 0.4 ns
Input resistance = 10 MΩ
Input capacitance = 1.7 pF

2N4117-19/2N4117A-19A N-Channel JFETs

General Description

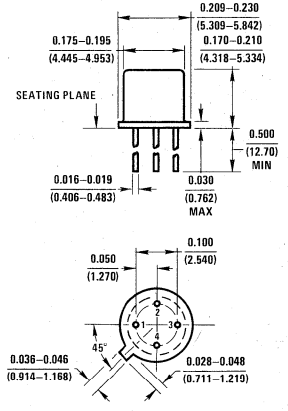
The 2N4117 thru 2N4119/A series of N-channel JFETs is designed for ultra low leakage ($I_{GSS} < 1$ pA) amplifier applications.

Typical $I_G < 0.1$ pA at $V_{DG} = 10V$, $I_D = 10\ \mu A$. Perfect for all smoke detector applications.

Absolute Maximum Ratings (25°C)

Gate-Drain or Gate-Source Voltage	−40V
Gate-Current	50 mA
Total Device Dissipation (Derate 2 mW/°C to +175°C)	300 mW
Storage Temperature Range	−65°C to +175°C
Lead Temperature (1/16" from case for 10 seconds)	255°C

TO-72



PIN	FET
1	S
2	D
3	G
4	Case

Electrical Characteristics (25°C unless otherwise noted)

PARAMETER		CONDITIONS		2N4117/ 2N4117A		2N4118/ 2N4118A		2N4119/ 2N4119A		UNITS
				MIN	MAX	MIN	MAX	MIN	MAX	
I_{GSS}	Gate Reverse Current 2N4117 Series Only	$V_{GS} = -20V$, $V_{DS} = 0$			−10		−10		−10	pA
			150°C		−25		−25		−25	nA
I_{GSS}	Gate Reverse Current 2N4117A Series Only	$V_{GS} = -20V$, $V_{DS} = 0$			−1		−1		−1	pA
			150°C		−2.5		−2.5		−2.5	nA
BV_{GSS}	Gate-Source Breakdown Voltage	$I_G = -1\ \mu A$, $V_{DS} = 0$		−40		−40		−40		V
$V_{GS(off)}$	Gate-Source Cutoff Voltage	$V_{DS} = 10V$, $I_D = 1$ nA		−0.6	−1.8	−1	−3	−2	−6	V
I_{DSS}	Saturation Drain Current	$V_{DS} = 10V$, $V_{GS} = 0$		0.03	0.09	0.08	0.24	0.20	0.60	mA
g_{fs}	Common-Source Forward Transconductance	$V_{DS} = 10V$, $V_{GS} = 0$	f = 1 kHz	70	210	80	250	100	330	μmho
g_{os}	Common-Source Output Conductance				3		5		10	
C_{iss}	Common-Source Input Capacitance		f = 1 MHz		3		3		3	pF
C_{rss}	Common-Source Reverse Transfer Capacitance				1.5		1.5		1.5	

2N4338-41 N-Channel JFETs

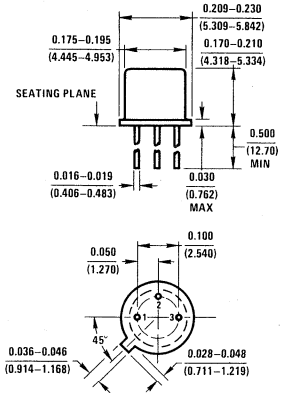
General Description

The 2N4338 thru 2N4341 series of N-channel JFETs is characterized for low to medium frequency amplifier applications. Tight selections of $V_{GS(off)}$, I_{DSS}, g_{fs} results in consistent characteristics in all applications.

Absolute Maximum Ratings (25°C)

Gate-Drain or Gate-Source Voltage	−50V
Gate Current	50 mA
Total Device Dissipation, T_A = 25°C (Derate 2 mW/°C to +175°C)	300 mW
Storage Temperature Range	−65°C to +200°C
Maximum Operating Temperature	175°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-18 2N Series



PIN	FET
1	S
2	D
3	G

Electrical Characteristics (25°C unless otherwise specified)

PARAMETER		CONDITIONS		2N4338		2N4339		2N4340		2N4341		UNITS
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
I_{GSS}	Gate Reverse Current	V_{GS} = −30V, V_{DS} = 0			−0.1		−0.1		−0.1		−0.1	nA
			150°C		−0.1		−0.1		−0.1		−0.1	μA
BV_{GSS}	Gate-Source Breakdown Voltage	I_G = −1 μA, V_{DS} = 0		−50		−50		−50		−50		V
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 15V, I_D = 0.1 μA		−0.3	−1	−0.6	−1.8	−1	−3	−2	−6	
$I_{D(off)}$	Drain Cutoff Current	V_{DS} = 15V V_{GS} = ( )			0.05 (−5)		0.05 (−5)		0.05 (−5)		0.07 (−10)	nA (V)
I_{DSS}	Saturation Drain Current	V_{DS} = 15V, V_{GS} = 0		0.2	0.6	0.5	1.5	1.2	3.6	3	9	mA
g_{fs}	Common-Source Forward Transconductance	V_{DS} = 15V, V_{GS} = 0	f = 1 kHz	600	1800	800	2400	1300	3000	2000	4000	μmho
g_{os}	Common-Source Output Conductance				5		15		30		60	
r_{ds}	Drain-Source ON Resistance	V_{DS} = 0, V_{GS} = 0			2500		1700		1500		800	Ω
C_{iss}	Common-Source Input Capacitance	V_{DS} = 15V, V_{GS} = 0	f = 1 MHz		7		7		7		7	pF
C_{rss}	Common-Source Reverse Transfer Capacitance				3		3		3		3	
NF	Noise Figure	V_{DS} = 15V, V_{GS} = 0 R_{gen} = 1M, BW = 200 Hz	f = 1 kHz		1		1		1		1	dB

2N4391-3/PN4391-3 N-Channel JFETs

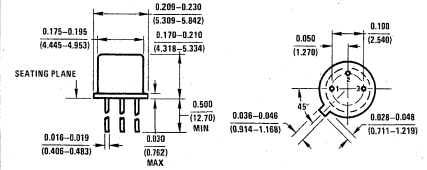
General Description

The 2N4391/PN4391 thru 2N4393/PN4393 series of N-channel JFETs is characterized by low ON resistance, moderate capacitance and low noise. Applications include low ON resistance, high speed switches and high gain, low noise amplifiers.

Absolute Maximum Ratings (25°C)

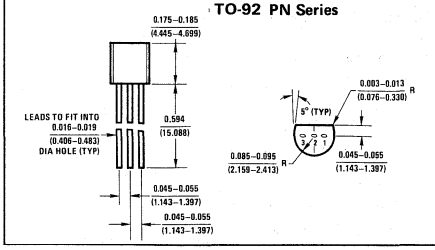
Reverse Gate-Drain or Gate-Source Voltage	−40V
Gate Current	50 mA
Total Device Dissipation at 25°C Case Temperature	
(Derate 10 mW/°C) 2N Series	1.8 W
(Derate 3 mW/°C) PN Series, T_A = 25°C	350 mW
Storage Temperature Range	
2N Series	−55°C to +200°C
PN Series	−55°C to +150°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-18 2N Series



PIN	FET
1	S
2	D
3	G

TO-92 PN Series



PIN	FET
1	G
2	S
3	D

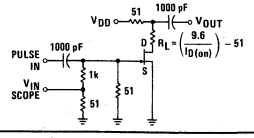
Electrical Characteristics* (25°C unless otherwise noted)

PARAMETER		CONDITIONS			2N4391/ PN4391		2N4392/ PN4392		2N4393/ PN4393		UNITS
					MIN	MAX	MIN	MAX	MIN	MAX	
I_{GSS}	Gate Reverse Current	V_{GS} = −20V, V_{DS} = 0		2N Series		100		100		100	pA
				PN Series		1		1		1	nA
				150°C		−200		−200		−200	
BV_{GSS}	Gate-Source Breakdown Voltage	I_G = −1 μA, V_{DS} = 0			−40		−40		−40		V
$I_{D(off)}$	Drain Cutoff Current	V_{DS} = 20V	V_{GS} = −5V	2N Series						100	pA
				PN Series						1	nA
				150°C						200	
			V_{GS} = −7V	2N Series				100			pA
				PN Series				1			nA
				150°C				200			
			V_{GS} = −12V	2N Series		100					pA
				PN Series		1					nA
				150°C		200					
$V_{GS(f)}$	Gate-Source Forward Voltage	I_G = 1 mA, V_{DS} = 0, (Note 2)				1		1		1	V
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 20V, I_D = 1 nA			−4	−10	−2	−5	−0.5	−3	
I_{DSS}	Saturation Drain Current	V_{DS} = 20V, V_{GS} = 0, (Note 1)			50	150	25	75	5	30	mA
$V_{DS(on)}$	Drain-Source ON Voltage	V_{GS} = 0	I_D = 3 mA							0.4	V
			I_D = 6 mA					0.4			
			I_D = 12 mA			0.4					
$r_{DS(on)}$	Static Drain-Source ON Resistance	V_{GS} = V, I_D = 1 mA				30		60		100	Ω
$r_{ds(on)}$	Drain-Source ON Resistance	V_{GS} = V, I_D = 0		f = 1 kHz		30		60		100	Ω
C_{iss}	Common-Source Input Capacitance	V_{DS} = 20V, V_{GS} = 0		f = 1 MHz		14		14		14	pF
C_{rss}	Common-Source Reverse Transfer Capacitance	V_{DS} = 0	V_{GS} = −5V							3.5	
			V_{GS} = −7V					3.5			
			V_{GS} = −12V			3.5					
t_d	Turn ON Delay Time	V_{DD} = 10V, $V_{GS(on)}$ = 0				15		15		15	ns
t_r	Rise Time		$I_{D(on)}$	$V_{GS(off)}$		5		5		5	
t_{off}	Turn OFF Delay Time	2N/PN4391	12 mA	−12V		20		35		50	
t_f	Fall Time	2N/PN4392	6 mA	−7V		15		20		30	
		2N/PN4393	3 mA	−5V							

Note 1: Pulse test required, pulse width = 300 μs, duty cycle ≤ 3%.

Note 2: Not tested on PN series.

*JEDEC registered data



Input Pulse
Rise time < 0.5 ns
Fall time < 0.5 ns
Pulse duty cycle = 1%

Sampling scope
Rise time = 0.4 ns
Input resistance = 50 Ω

2N4416/2N4416A N-Channel JFETs

General Description

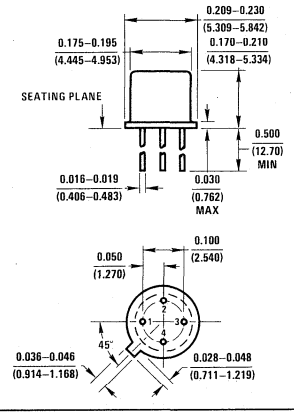
The 2N4416/2N4416A N-channel JFET is designed for VHF/UHF amplifier, mixer and oscillator applications.

Qualified for JAN, JANTX, JANTXV level processing per MIL-19500/428.

Absolute Maximum Ratings (25°C)

Gate-Drain or Gate-Source Voltage	
2N4416	−30V
2N4416A	−35V
Gate Current	10 mA
Total Device Dissipation	
(Derate 1.7 mW/°C)	300 mW
Storage Temperature Range	−65°C to +200°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-72



PIN	FET N (25)
1	S
2	D
3	G
4	Case

Electrical Characteristics (25°C unless otherwise noted)

PARAMETER		CONDITIONS		MIN	MAX	UNITS
I_{GSS}	Gate Reverse Current	V_{GS} = −20V, V_{DS} = 0			−0.1	nA
			150°C		−0.1	μA
BV_{GSS}	Gate-Source Breakdown Voltage	I_G = −1 μA, V_{DS} = 0	2N4416	−30		V
			2N4416A	−35		
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 15V, I_D = 1 nA	2N4416		−6	V
			2N4416A	−2.5	−6	
I_{DSS}	Drain Current at Zero Gate Voltage, (Note 1)	V_{DS} = 15V, V_{GS} = 0		5	15	mA
g_{fs}	Common-Source Forward Transconductance, (Note 1)		f = 1 kHz	4500	7500	μmho
g_{os}	Common-Source Output Conductance				50	μmho
C_{rss}	Common-Source Reverse Transfer Capacitance		f = 1 MHz		0.8	pF
C_{iss}	Common-Source Input Capacitance				4	pF
C_{oss}	Common-Source Output Capacitance				2	

High Frequency Characteristics

PARAMETER		CONDITIONS	100 MHz		400 MHz		UNITS
			MIN	MAX	MIN	MAX	
g_{iss}	Common-Source Input Conductance	V_{DS} = 15V, V_{GS} = 0		100		1000	μmho
b_{iss}	Common-Source Input Susceptance			2500		10,000	μmho
g_{oss}	Common-Source Output Conductance			75		100	μmho
b_{oss}	Common-Source Output Susceptance			1000		4000	μmho
g_{fs}	Common-Source Forward Transconductance, (Note 1)				4000		μmho
G_{ps}	Common-Source Power Gain	V_{DS} = 15V, I_D = 5 mA	18		10		dB
NF	Noise Figure	V_{DS} = 15V, I_D = 5 mA, R_G = 1 kΩ		2		4	dB

Note 1: Pulse test duration = 2 ms.

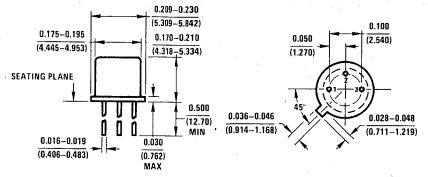
2N4856-61/PN4856-61 N-Channel JFETs

General Description

The 2N4856/PN4856 thru 2N4861/PN4861 series of N-channel JFETs is designed for analog switch applications requiring low ON resistance and moderate capacitance.

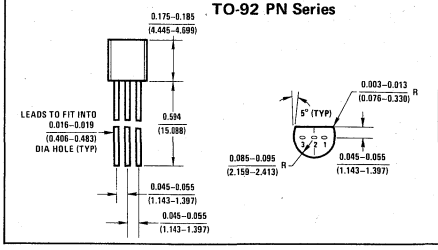
Qualified for JAN, JANTX, JANTXV level processing per MIL-S-19500/385. 2N series only.

TO-18 2N Series



PIN	FET
1	S
2	D
3	G

TO-92 PN Series



PIN	FET
1	G
2	S
3	D

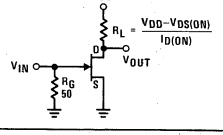
Absolute Maximum Ratings (25°C)

Reverse Gate-Drain or Gate-Source Voltage
2N4856/PN4856–2N4858/PN4858 –40V
Reverse Gate-Drain or Gate-Source Voltage
2N4859/PN4859–2N4861/PN4861 –30V
Gate Current 50 mA
Total Device Dissipation at 25°C Case Temperature
(Derate 10 mW/°C) 2N Series 1.8 W
(Derate 3 mW/°C) PN series, T_A = 25°C 350 mV
Storage Temperature Range
2N Series –65°C to +200°C
PN Series –65°C to +150°C
Lead Temperature (1/16" from case for 10 seconds) 300°C

Electrical Characteristics (25°C unless otherwise noted)

PARAMETER		CONDITIONS		2N4856,59/ PN4856,59		2N4857,60/ PN4857,60		2N4858,61/ PN4858,61		UNITS
				MIN	MAX	MIN	MAX	MIN	MAX	
BV_{GSS}	Gate-Source Breakdown Voltage	I_G = –1 μA, V_{DS} = 0	2N/PN4856-58	–40		–40		–40		V
			2N/PN4859-61	–30		–30		–30		
I_{GSS}	Gate Reverse Current	V_{GS} = –20V, V_{DS} = 0	2N Series		–250		–250		–250	pA
			PN Series		–1		–1		–1	nA
		V_{GS} = –15V, V_{DS} = 0	150°C		–500		–500		–500	
$I_{D(off)}$	Drain Cutoff Current	V_{DS} = 15V, V_{GS} = –10V	2N Series		250		250		250	pA
			PN Series		1		1		1	nA
			150°C		500		500		500	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 15V, I_D = 0.5 nA		–4	–10	–2	–6	–0.8	–4	V
I_{DSS}	Saturation Drain Current	V_{DS} = 15V, V_{GS} = 0, (Note 1)		50		20	100	8	80	mA
$V_{DS(on)}$	Drain-Source ON Voltage	V_{GS} = 0	I_D = 20 mA		0.75					V
			I_D = 10 mA				0.50			
			I_D = 5 mA						0.50	
$r_{ds(on)}$	Drain-Source ON Resistance	V_{GS} = 0, I_D = 0	f = 1 kHz		25		40		60	Ω
C_{iss}	Common-Source Input Capacitance	V_{DS} = 0, V_{GS} = –10V	f = 1 MHz		18		18		18	pF
C_{rss}	Common-Source Reverse Transfer Capacitance				8		8		8	
t_d	Turn ON Delay Time	V_{DD} = 10V, $V_{GS(on)}$ = 0,			6		6		10	ns
t_r	Rise Time	$I_{D(on)}$ $V_{GS(off)}$ R_L			3		4		10	ns
t_{off}	Turn OFF Time	2N/PN4856,59 20 mA –10V 464 Ω 2N/PN4857,60 10 mA –6V 953 Ω 2N/PN4858,61 5 mA –4V 1910 Ω			25		50		100	ns

Note 1: Pulse test required, pulse width = 100 μs, duty cycle ≤ 10%.



Input Pulse
Rise time = 0.25 ns
Fall time = 0.75 ns
Pulse width = 100 ns
Pulse duty cycle < 10%

Sampling scope
Rise time = 0.75 ns
Input resistance = 1 MΩ
Input capacitance = 2.5 pF

2N5114-16 P-Channel JFETs

General Description

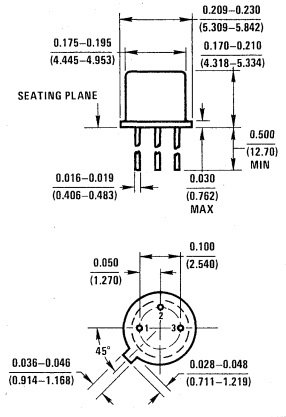
The 2N5114 thru 2N5116 series of P-channel JFETs is designed for low ON resistance analog switch applications.

Qualified for JAN, JANTX, JANTXV level processing per MIL-S-19500/476.

Absolute Maximum Ratings (25°C)

Reverse Gate-Drain or Gate-Source Voltage	30V
Gate Current	50 mA
Total Device Dissipation, Free-Air (Derate 3 mW/°C)	500 mW
Storage Temperature Range	−65°C to +200°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-18

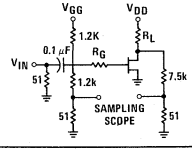


PIN	FET
1	S
2	G
3	D

Electrical Characteristics (25°C unless otherwise noted)

PARAMETER		CONDITIONS		2N5114 MIN	2N5114 MAX	2N5115 MIN	2N5115 MAX	2N5116 MIN	2N5116 MAX	UNITS
BV_{GSS}	Gate-Source Breakdown Voltage	I_G = 1 μA, V_{DS} = 0		30		30		30		V
I_{GSS}	Gate Reverse Current	V_{GS} = 20V, V_{DS} = 0			500		500		500	pA
			150°C		1.0		1.0		1.0	μA
$I_{D(off)}$	Drain Cutoff Current	V_{DS} = −15V, V_{GS} = 2N5114 = 12V, 2N5115 = 7V, 2N5116 = 5V			−500		−500		−500	pA
			150°C		−1.0		−1.0		−1.0	μA
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = −15V, I_D = −1 nA		5	10	3	6	1	4	V
I_{DSS}	Saturation Drain Current	V_{GS} = 0, V_{DS} = 2N5114 = −18V, 2N5115 = −15V		−30	−90	−15	−60	−5	−25	mA
$V_{GS(f)}$	Forward Gate-Source Voltage	I_G = −1 mA, V_{DS} = 0			−1		−1		−1	V
$V_{DS(on)}$	Drain-Source ON Voltage	V_{GS} = 0, I_D = 2N5114 = −15 mA, 2N5115 = −7 mA, 2N5116 = −3 mA			−1.3		−0.8		−0.6	V
$r_{DS(on)}$	Static Drain-Source ON Resistance	V_{GS} = 0, I_D = −1 mA			75		100		150	Ω
$r_{ds(on)}$	Drain-Source ON Resistance	V_{GS} = 0, I_D = 0	f = 1 kHz		75		100		150	Ω
C_{iss}	Common-Source Input Capacitance	V_{DS} = −15, V_{GS} = 0	f = 1 MHz		25		25		25	pF
C_{rss}	Common-Source Reverse Transfer Capacitance	V_{DS} = 0, V_{GS} = 2N5114 = 12V, 2N5115 = 7V, 2N5116 = 5V			7		7		7	pF

		2N5114	2N5115	2N5116						
t_d	Turn ON Delay Time	V_{DD}	−10V	−6V	−6V		6		10		12	ns
t_r	Rise Time	V_{GG}	20V	12V	8V		10		20		30	ns
t_{off}	Turn OFF Time	R_L	430Ω	910Ω	2000Ω		6		8		10	ns
t_f	Fall Time	R_G	100Ω	220Ω	390Ω		15		30		50	ns
		$I_{D(on)}$	−15 mA	−7 mA	−3 mA							



Input Pulse
Rise time < 1 ns
Fall time < 1 ns
Pulse width = 100 ns
Repetition rate = 1 MHz

Sampling Scope
Rise time = 0.4 ns
Input resistance = 10 MΩ
Input capacitance = 1.5 pF

2N5196-99 N-Channel Monolithic Dual JFETs

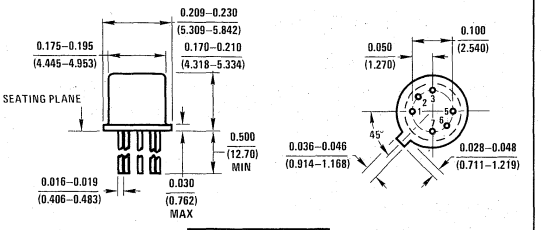
General Description

The 2N5196 thru 2N5199 series of N-channel monolithic dual JFETs is designed for low to medium frequency differential amplifiers requiring low leakage and tight match.

Absolute Maximum Ratings (25°C)

Gate-Drain or Gate-Source Voltage	−50V
Gate Current	50 mA
Device Dissipation (Each Side), T_A = 85°C (Derate 2.56 mW/°C)	250 mW
Total Device Dissipation, T_A = 85°C (Derate 4.3 mW/°C)	500 mW
Storage Temperature Range	−65°C to +200°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-71



PIN	FET (12)
1	S1
2	D1
3	G1
5	S2
6	D2
7	G2

Electrical Characteristics (25°C unless otherwise noted)

PARAMETER		CONDITIONS		MIN	MAX	UNITS
I_{GSS}	Gate Reverse Current	V_{GS} = −30V, V_{DS} = 0			−25	pA
			150°C		−50	nA
BV_{GSS}	Gate-Source Breakdown Voltage	I_G = −1 μA, V_{DS} = 0		−50		
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 20V, I_D = 1 nA		−0.7	−4	V
V_{GS}	Gate-Source Voltage	V_{DG} = 20V, I_D = 200 μA		−0.2	−3.8	
I_G	Gate Operating Current				−15	pA
			125°C		−15	nA
I_{DSS}	Saturation Drain Current	V_{DS} = 20V, V_{GS} = 0, (Note 1)		0.7	7	mA
g_{fs}	Common-Source Forward Transconductance	V_{DS} = 20V, V_{GS} = 0, (Note 1)	f = 1 kHz	1000	4000	μmho
g_{fs}	Common-Source Forward Transconductance	V_{DG} = 20V, I_D = 200 μA, (Note 1)		700	1600	
g_{os}	Common-Source Output Conductance	V_{DS} = 20V, V_{GS} = 0			50	
g_{os}	Common-Source Output Conductance	V_{DG} = 20V, I_D = 200 μA			4	
C_{iss}	Common-Source Input Capacitance	V_{DS} = 20V, V_{GS} = 0	f = 1 MHz		6	pF
C_{rss}	Common-Source Reverse Transfer Capacitance				2	
NF	Spot Noise Figure		f = 100 Hz, R_G = 10 MΩ		0.5	dB
e_n	Equivalent Input Noise Voltage		f = 1 kHz		0.020	$\frac{\mu V}{\sqrt{Hz}}$

Matching Characteristics

PARAMETER		CONDITIONS		2N5196 MIN	2N5196 MAX	2N5197 MIN	2N5197 MAX	2N5198 MIN	2N5198 MAX	2N5199 MIN	2N5199 MAX	UNITS
$\lvert I_{G1}-I_{G2}\rvert$	Differential Gate Current	V_{DG} = 20V, I_D = 200 μA	125°C		5		5		5		5	nA
$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio	V_{DS} = 20V, V_{GS} = 0V, (Note 1)		0.95	1	0.95	1	0.95	1	0.95	1	
$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio, (Note 1)	V_{DG} = 20V, I_D = 200 μA	f = 1 kHz	0.97	1	0.97	1	0.95	1	0.95	1	
$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage				5		5		10		15	mV
$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Differential Voltage Change with Temperature, (Note 2)		T_A = 25°C, T_B = 125°C		5		10		20		40	μV/°C
			T_A = −55°C, T_B = 25°C		5		10		20		40	
$\lvert g_{os1}-g_{os2}\rvert$	Differential Output Conductance		f = 1 kHz		1		1		1		1	μmho

Note 1: Pulse test required, pulse width = 300 μs, duty cycle ≤ 3%.

Note 2: Measured at end points, T_A and T_B.

2N5245-47 N-Channel JFETs

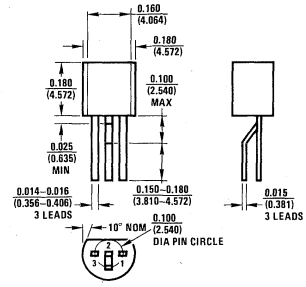
General Description

The 2N5245 thru 2N5247 series of N-channel JFETs is designed for common-source or common-gate VHF/UHF amplifier, mixer and oscillator applications to 400 MHz.

Absolute Maximum Ratings

Drain-Gate Voltage	30V
Source Gate Voltage	30V
Drain Current	30 mA
Forward Gate Current	50 mA
Total Device Dissipation @ 25°C	360 mW
(Derate above 25°C)	2.88 mW/°C
Operating Junction Temperature Range	−65°C to +150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-92



PIN	FET
1	D
2	S
3	G

Electrical Characteristics (25°C unless otherwise noted)

PARAMETER		CONDITIONS		2N5245 MIN	2N5245 MAX	2N5246 MIN	2N5246 MAX	2N5247 MIN	2N5247 MAX	UNITS
I_{GSS}	Gate Reverse Current	V_{GS} = −20V, V_{DS} = 0			−1		−1		−1	nA
			T_A = 100°C		−500		−500		−500	
BV_{GSS}	Gate-Source Breakdown Voltage	I_G = −1 μA, V_{DS} = 0		−30		−30		−30		V
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 15V, I_D = 10 nA		−1	−6	−0.5	−4	−1.5	−8	
I_{DSS}	Saturation Drain Current	V_{DS} = 15V, V_{GS} = 0, (Note 1)		5	15	1.5	7	8	24	mA
g_{fs}	Common-Source Forward Transconductance	V_{DS} = 15V, V_{GS} = 0	f = 1 kHz	4.5	7.5	3.0	6.0	4.5	8.0	mmho
g_{os}	Common-Source Output Conductance		f = 1 kHz		50		50		70	μmho
$Re(y_{fs})$	Common-Source Forward Transconductance		f = 400 MHz	4.0		2.5		4.0		mmho
$Re(y_{os})$	Common-Source Output Conductance		f = 100 MHz		75		75		100	μmho
			f = 400 MHz		100		100		150	
$Re(y_{is})$	Common-Source Input Conductance		f = 100 MHz		100		100		100	
C_{iss}	Common-Source Input Capacitance		f = 1 MHz		4.5		4.5		4.5	pF
C_{rss}	Common-Source Reverse Transfer Capacitance		f = 1 MHz		1		1		1	
NF	Noise Figure	V_{DS} = 15V, I_D = 5 mA, R_G = 1 kΩ	f = 100 MHz		2		2		2	dB
		V_{DS} = 15V, I_D = 5 mA, R_G = 1 kΩ	f = 400 MHz		4		4		4	
G_{ps}	Common-Source Power Gain	V_{DS} = 15V, I_D = 5 mA, R_G = 1 kΩ	f = 100 MHz	18		18		18		
		V_{DS} = 15V, I_D = 5 mA, R_G = 1 kΩ	f = 400 MHz	10		10		10		

Note 1: Pulse Test PW 300 μs, duty cycle ≤ 3%.

2N5358-60 N-Channel JFETs

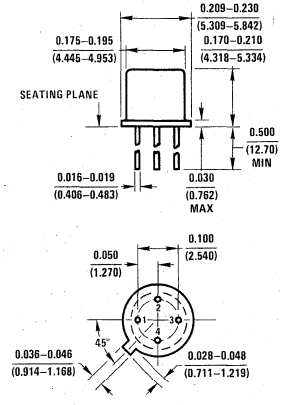
General Description

The 2N5358 thru 2N5360 series of N-channel JFETs is characterized for general purpose audio and RF amplifiers requiring tightly specified I_{DSS} ranges.

Absolute Maximum Ratings (25°C)

Gate-Drain or Gate-Source Voltage	−40V
Gate Current	10 mA
Total Device Dissipation (25°C Free-Air Temperature)	300 mW
Power Derating (to +175°C)	2 mW/°C
Storage Temperature Range	−65°C to +200°C
Operating Temperature Range	−65°C to +175°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-72



PIN	FET
1	S
2	D
3	G
4	Case

Electrical Characteristics (25°C unless otherwise noted)

PARAMETER		CONDITIONS		2N5358		2N5359		2N5360		UNITS
				MIN	MAX	MIN	MAX	MIN	MAX	
I_{GSS}	Gate Reverse Current	V_{DS} = 0, V_{GS} = −20V			−100		−100		−100	pA
			T = 150°C		−100		−100		−100	nA
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 15V, I_D = 100 nA		−0.5	−3.0	−0.8	−4.0	−0.8	−4.0	V
BV_{GSS}	Gate-Source Breakdown Voltage	V_{DS} = 0, I_G = −10 μA		−40		−40		−40		V
I_{DSS}	Saturation Drain Current	V_{DS} = 15V, V_{GS} = 0, (Note 1)		0.5	1.0	0.8	1.6	1.5	3.0	mA
V_{GS}	Gate-Source Voltage	V_{DS} = 15V, I_D = (Note 2)		−0.3	−1.5	−0.4	−2.0	−0.5	−2.5	V
g_{fs}	Common-Source Forward Transconductance	V_{DS} = 15V, V_{GS} = 0	f = 1 kHz	1000	3000	1200	3600	1400	4200	μmho
$\|Y_{fs}\|$	Common-Source Forward Transadmittance		f = 100 MHz	800		900		1400		
g_{oss}	Common-Source Output Conductance		f = 1 kHz		10		10		20	
C_{rss}	Common-Source Reverse Transfer Capacitance		f = 1 MHz		2		2		2	pF
C_{iss}	Common-Source Input Capacitance				6		6		6	
NF	Noise Figure		f = 100 Hz, R_G = 1 MΩ		2.5		2.5		2.5	dB

Note 1: Pulse test duration = 300 μs. Duty cycle ≤ 3%.
Note 2: I_D test conditions for Test 5: 2N5358 = 50 μA; 2N5359 = 80 μA; 2N5360 = 150 μA.

2N5361-64 N-Channel JFETs

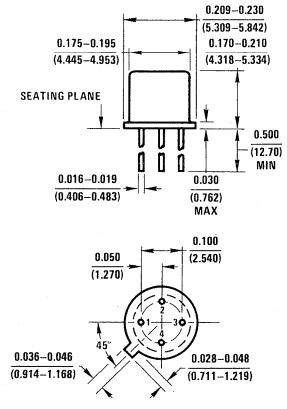
General Description

The 2N5361 thru 2N5364 series of N-channel JFETs is characterized for general purpose audio and RF amplifiers requiring tightly specified I_{DSS} ranges.

Absolute Maximum Ratings (25°C)

Gate-Drain or Gate-Source Voltage	−40V
Gate Current	10 mA
Total Device Dissipation (25°C Free-Air Temperature)	300 mW
Power Derating (to +175°C)	2 mW/°C
Storage Temperature Range	−65°C to +200°C
Operating Temperature Range	−65°C to +175°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-72



PIN	FET
1	S
2	D
3	G
4	Case

Electrical Characteristics (25°C unless otherwise noted)

PARAMETER		CONDITIONS		2N5361		2N5362		2N5363		2N5364		UNITS
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
I_{GSS}	Gate Reverse Current	V_{DS} = 0, V_{GS} = −20V			−100		−100		−100		−100	pA
			T = 150°C		−100		−100		−100		−100	nA
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 15V, I_D = 100 nA		−1.0	−6.0	−2.0	−7.0	−2.5	−8.0	−2.5	−8.0	V
BV_{GSS}	Gate-Source Breakdown Voltage	V_{DS} = 0, I_G = −10 μA		−40		−40		−40		−40		
I_{DSS}	Saturation Drain Current	V_{DS} = 15V, V_{GS} = 0, (Note 1)		2.5	5.0	4.0	8.0	7.0	14.0	9.0	18.0	mA
V_{GS}	Gate-Source Voltage	V_{DS} = 15V, I_D = (Note 2)		−1.0	−5.0	−1.3	−5.0	−2.0	−6.0	−2.0	−6.0	V
g_{fs}	Common-Source Forward Transconductance	V_{DS} = 15V, V_{GS} = 0	f = 1 kHz	1500	4500	2000	5500	2500	6000	2700	6500	μmho
Y_{fs}	Common-Source Forward Transadmittance		f = 100 MHz	1700		1900		2100		2200		
g_{oss}	Common-Source Output Conductance		f = 1 kHz		20		40		40		60	
C_{rss}	Common-Source Reverse Transfer Capacitance		f = 1 MHz		2		2		2		2	pF
C_{iss}	Common-Source Input Capacitance				6		6		6		6	
NF	Noise Figure		f = 100 Hz, R_G = 1 MΩ		2.5		2.5		2.5		2.5	dB

Note 1: Pulse test duration = 300 μs.

Note 2: I_D test conditions for Test 6: 2N5361 = 250 μA; 2N5362 = 400 μA; 2N5363 = 700 μA; 2N5364 = 900 μA.

2N5397, 2N5398 N-Channel JFETs

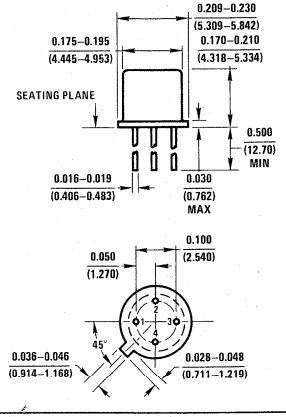
General Description

The 2N5397 thru 2N5398 series of N-channel JFETs is designed for VHF/UHF common-source or common-gate amplifiers, mixers and oscillators.

Absolute Maximum Ratings (25°C)

Gate-Drain or Gate-Source Voltage	−25V
Gate Current	10 mA
Total Device Dissipation (Derate 1.7 mW/°C)	300 mW
Storage Temperature Range	−65°C to +200°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-72



PIN	FET
1	S
2	D
3	G
4	Case

Electrical Characteristics (25°C unless otherwise noted)

PARAMETER		CONDITIONS		2N5397 MIN	2N5397 MAX	2N5398 MIN	2N5398 MAX	UNITS
I_{GSS}	Gate Reverse Current	V_{GS} = −15V, V_{DS} = 0			−0.1		−0.1	nA
			150°C		−0.1		−0.1	μA
BV_{GSS}	Gate-Source Breakdown Voltage	V_{DS} = 0, I_G = −1 μA		−25		−25		V
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 10V, I_D = 1 nA		−1.0	−6.0	−1.0	−6.0	V
I_{DSS}	Saturation Drain Current	V_{DS} = 10V, V_{DS} = 0		10	30	5	40	mA
$V_{GS(f)}$	Gate-Source Forward Voltage	V_{DS} = 0, I_G = 1 mA			1		1	V
g_{fs}	Common-Source Forward Transconductance, (Note 1)	V_{DS} = 10V, I_D = 10 mA	f = 1 kHz	6000	10,000			μmho
		V_{DS} = 10V, V_{GS} = 0				5500	10,000	
g_{os}	Common-Source Output Conductance	V_{DS} = 10V, I_D = 10 mA			200			
		V_{DS} = 10V, V_{GS} = 0					400	
C_{rss}	Common-Source Reverse Transfer Capacitance	V_{DS} = 10V, I_D = 10 mA	f = 1 MHz		1.2			pF
		V_{DS} = 10V, V_{GS} = 0					1.3	
C_{iss}	Common-Source Input Capacitance	V_{DG} = 10V, I_D = 10 mA			5.0			
		V_{DS} = 10V, V_{GS} = 0					5.5	
g_{iss}	Common-Source Input Conductance	V_{DG} = 10V, I_D = 10 mA	f = 450 MHz		2000			μmho
		V_{DS} = 10V, V_{GS} = 0					3000	
g_{oss}	Common-Source Output Conductance	V_{DG} = 10V, I_D = 10 mA			400			
		V_{DS} = 10V, V_{GS} = 0					500	
g_{fs}	Common-Source Forward Transconductance, (Note 1)	V_{DG} = 10V, I_D = 10 mA		5500	9000			
		V_{DS} = 10V, V_{GS} = 0				5000	10,000	
G_{ps}	Common-Source Power Gain (Neutralized)	V_{DG} = 10V, I_D = 10 mA		15				dB
NF	Common-Source, Spot Noise Figure (Neutralized)				3.5			

Note 1: Pulse test duration = 2 ms.

2N5432-34 N-Channel JFETs

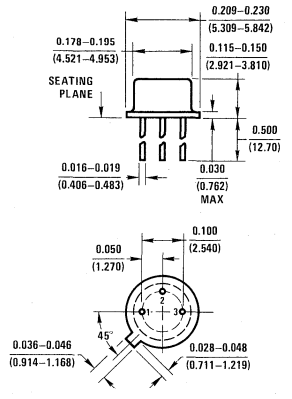
General Description

The 2N5432 thru 2N5434 series of N-channel JFETs is designed for analog switch applications requiring very low ON resistance.

Absolute Maximum Ratings (25°C)

Reverse Gate-Drain or Gate-Source Voltage	−25V
Gate Current	100 mA
Drain Current	400 mA
Total Device Dissipation at 25°C Free-Air Temperature, (Note 1)	300 mW
Storage Temperature Range	−65°C to +200°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-52



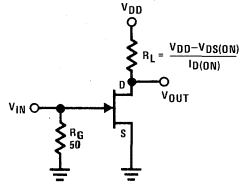
PIN	FET (07)
1	S
2	D
3	G

Electrical Characteristics (25°C unless otherwise noted)

PARAMETER		CONDITIONS		2N5432		2N5433		2N5434		UNITS
				MIN	MAX	MIN	MAX	MIN	MAX	
I_{GSS}	Gate Reverse Current	V_{GS} = −15V, V_{DS} = 0			−200		−200		−200	pA
			150°C		−200		−200		−200	nA
BV_{GSS}	Gate-Source Breakdown Voltage	I_G = −1 μA, V_{DS} = 0		−25		−25		−25		V
$I_{D(off)}$	Drain Cutoff Current	V_{DS} = 5V, V_{GS} = −10V			200		200		200	pA
			150°C		200		200		200	nA
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 5V, I_D = 3 nA		−4	−10	−3	−9	−1	−4	V
I_{DSS}	Saturation Drain Current	V_{DS} = 15V, V_{GS} = 0, (Note 2)		150		100		30		mA
$r_{DS(on)}$	Static Drain-Source ON Resistance	V_{GS} = 0, I_D = 10 mA		2	5		7		10	Ω
$V_{DS(on)}$	Drain-Source ON Voltage				50		70		100	mV
$r_{ds(on)}$	Drain-Source ON Resistance	V_{GS} = 0, I_D = 0	f = 1 kHz		5		7		10	Ω
C_{iss}	Common-Source Input Capacitance	V_{DS} = 0, V_{GS} = −10V	f = 1 MHz		30		30		30	pF
C_{rss}	Common-Source Reverse Transfer Capacitance				15		15		15	
t_d	Turn ON Delay Time	V_{DD} = 1.5V, $V_{GS(on)}$ = 0, $V_{GS(off)}$ = −12V, $I_{D(on)}$ = 10 mA			4		4		4	ns
t_r	Rise Time				1		1		1	
t_{off}	Turn OFF Delay Time				6		6		6	
t_f	Fall Time				30		30		30	

Note 1: Derate linearly at the rate of 2.3 mW/°C.

Note 2: Pulse test required pulse width 300 μs, duty cycle ≤ 3%.



Input Pulse
Rise time = 0.25 ns
Fall time = 0.75 ns
Pulse width = 200 ns
Pulse rate = 550 pps

Sampling Scope
Rise time = 0.4 ns
Input resistance = 10M
Input Capacitance = 1.5 pF

2N5457-59 N-Channel JFETs

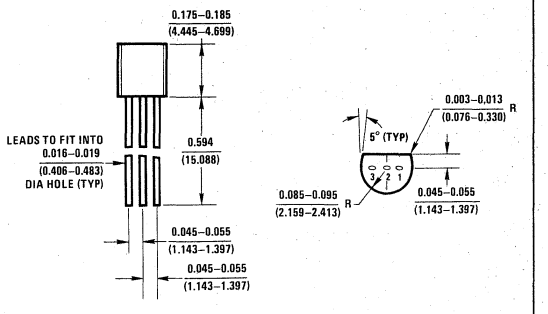
General Description

The 2N5457 thru 2N5459 series of N-channel JFETs is designed for general purpose small-signal amplifier and moderate ON resistance analog switch applications.

Absolute Maximum Ratings

Drain-Source Voltage	25V
Drain-Gate Voltage	25V
Source-Gate Voltage	25V
Total Device Dissipation at 25°C	310 mW
(Derate above 25°C)	2.82 mW/°C
Operating Junction Temperature	135°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-92



PIN	FET
1	G
2	S
3	D

Electrical Characteristics (25°C unless otherwise noted)

PARAMETER		CONDITIONS		2N5457			2N5458			2N5459			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
I_{GSS}	Gate Reverse Current	V_{GS} = −15V, V_{DS} = 0			−0.01	−1.0		−0.01	−1.0		−0.01	−1.0	nA
			T_A = 100°C			−200			−200			−200	
BV_{GSS}	Gate-Source Breakdown Voltage	I_G = −10 μA, V_{DS} = 0		−25	−60		−25	−60		−25	−60		V
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 15V, I_D = 10 nA		−0.5		−6.0	−1.0		−7.0	−2.0		−8.0	
I_{DSS}	Saturation Drain Current	V_{DS} = 15V, V_{GS} = 0, (Note 1)		1.0		5.0	2.0		9.0	4.0		16	mA
g_{fs}	Common-Source Forward Transconductance	V_{DS} = 15V, V_{GS} = 0	f = 1 kHz	1,000		5,000	1,500		5,500	2,000		6,000	μmho
g_{os}	Common-Source Output Conductance				10	50		15	50		20	50	
C_{iss}	Common-Source Input Capacitance		f = 1 MHz		4.5	7.0		4.5	7.0		4.5	7.0	pF
C_{rss}	Common-Source Reverse Transfer Capacitance				1.0	3.0		1.0	3.0		1.0	3.0	
NF	Noise Figure	V_{DS} = 15V, V_{GS} = 0, R_G = 1 MΩ, NBW = 1 Hz	f = 1 kHz		0.04	3.0		0.04	3.0		0.04	3.0	dB

Note 1: Pulse test PW ≤ 630 ms; duty cycle ≤ 10%.

2N5460-62 P-Channel JFETs

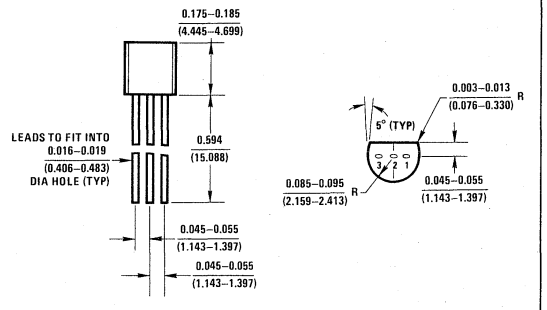
General Description

The 2N5460 thru 2N5462 series of P-channel JFETs is designed for general purpose amplifier applications.

Absolute Maximum Ratings (25°C)

Gate-Drain or Gate-Source Voltage	40V
Gate Current	10 mA
Total Device Dissipation	310 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-92



PIN	FET
1	G
2	S
3	D

Electrical Characteristics (25°C unless otherwise specified)

PARAMETER		CONDITIONS		2N5460		2N5461		2N5462		UNITS
				MIN	MAX	MIN	MAX	MIN	MAX	
I_{GSS}	Gate Reverse Current	V_{GS} = 20V, V_{DS} = 0			5		5		5	nA
			180°C		1		1		1	μA
BV_{GSS}	Gate-Source Breakdown Voltage	I_G = 10 μA, V_{DS} = 0		40		40		40		V
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = −15V, I_D = 0.1 μA		0.75	6.0	1.0	7.5	1.8	9.0	
V_{GS}	Gate-Source Voltage	V_{DS} = −15V	I_D = −0.1 mA	0.5	4.0					V
			I_D = −0.2 mA			0.8	4.5			
			I_D = −0.4 mA					1.5	6.0	
I_{DSS}	Saturation Drain Current	V_{DS} = 15V, V_{GS} = 0		1.0	5.0	2.0	9.0	4.0	16	mA
g_{fs}	Common-Source Forward Transconductance, (Note 3)	V_{DS} = −15V, V_{GS} = 0	f = 1 kHz	1000	4000	1500	4000	2000	6000	μmho
g_{os}	Common-Source Output Conductance				75		75		75	
C_{iss}	Common-Source Input Capacitance	V_{DS} = −15V, V_{GS} = 0	f = 1 MHz		7.0		7.0		7.0	pF
C_{rss}	Common-Source Reverse Transfer Capacitance				2.0		2.0		2.0	
NF	Noise Figure	V_{DS} = −15V, V_{GS} = 0, R_{gen} = 1M, BW = 1 Hz	f = 100 Hz		2.5		2.5		2.5	dB
e_n	Equivalent Input Noise Voltage				115		115		115	$\frac{nV}{\sqrt{Hz}}$

2N5484-86 N-Channel JFETs

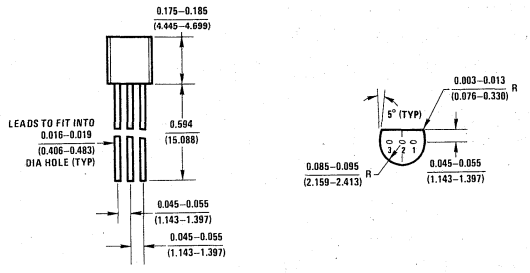
General Description

The 2N5484 thru 2N5486 series of N-channel JFETs is designed for VHF/UHF amplifier, mixer and oscillator applications.

Absolute Maximum Ratings (25°C)

Drain-Gate Voltage	25V
Source Gate Voltage	25V
Drain Current	30 mA
Forward Gate Current	10 mA
Total Device Dissipation @ 25°C	310 mW
(Derate above 25°C)	2.82 mW/°C
Operating Junction Temperature Range	−65°C to +150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-92



PIN	FET
1	G
2	S
3	D

Electrical Characteristics (25°C unless otherwise noted)

PARAMETER		CONDITIONS		2N5484		2N5485		2N5486		UNITS
				MIN	MAX	MIN	MAX	MIN	MAX	
I_{GSS}	Gate Reverse Current	V_{GS} = −20V, V_{DS} = 0			−1.0		−1.0		−1.0	nA
			T_A = 100°C		−200		−200		−200	
BV_{GSS}	Gate-Source Breakdown Voltage	I_G = −1 μA, V_{DS} = 0		−25		−25		−25		V
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 15V, I_D = 10 nA		−0.3	−3.0	−0.5	−4.0	−2.0	−6.0	
I_{DSS}	Saturation Drain Current	V_{DS} = 15V, V_{GS} = 0, (Note 1)		1.0	5.0	4.0	10	8.0	20	mA
g_{fs}	Common-Source Forward Transconductance	V_{DS} = 15V, V_{GS} = 0	f = 1 kHz	3000	6000	3500	7000	4000	8000	μmhos
g_{os}	Common-Source Output Conductance				50		60		75	
$Re(y_{fs})$	Common-Source Forward Transconductance		f = 100 MHz	2500						
			f = 400 MHz			3000		3500		
$Re(y_{os})$	Common-Source Output Conductance		f = 100 MHz		75					
			f = 400 MHz				100		100	
$Re(y_{is})$	Common-Source Input Conductance		f = 100 MHz		100					
			f = 400 MHz				1000		1000	
C_{iss}	Common-Source Input Capacitance				5.0		5.0		5.0	pF
C_{rss}	Common-Source Reverse Transfer Capacitance		f = 1 MHz		1.0		1.0		1.0	
C_{oss}	Common-Source Output Capacitance				2.0		2.0		2.0	
NF	Noise Figure	V_{DS} = 15V, V_{GS} = 0, R_G = 1 MΩ	f = 1 kHz		2.5		2.5		2.5	dB
		V_{DS} = 15V, I_D = 1 mA, R_G = 1 kΩ	f = 100 MHz		3.0					
		V_{DS} = 15V, I_D = 4 mA, R_G = 1 kΩ					2.0		2.0	
			f = 400 MHz				4.0		4.0	
G_{ps}	Common-Source Power Gain	V_{DS} = 15V, I_D = 1 mA	f = 100 MHz	16	25					
		V_{DS} = 15V, I_D = 4 mA				18	30	18	30	
			f = 400 MHz			10	20	10	20	

Note 1: Pulse test pulse width 300 μs, duty cycle ≤ 3%.

2N5515-24 N-Channel Monolithic Dual JFETs

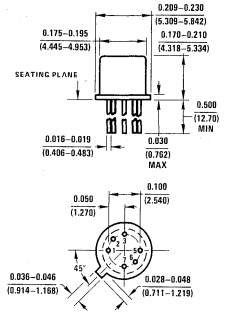
General Description

The 2N5515 thru 2N5524 series of N-channel monolithic dual JFETs is designed for low to medium frequency differential amplifiers requiring very low noise and high common-mode rejection.

Absolute Maximum Ratings (25°C)

Gate-Drain or Gate-Source Voltage	−40V
Gate Current	50 mA
Device Dissipation (Each Side), T_A = 85°C (Derate 2 mW/°C)	250 mW
Total Device Dissipation, T_A = 85°C (Derate 3 mW/°C)	375 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-71



PIN	FET (12)
1	S1
2	D1
3	G1
5	S2
6	D2
7	G2

Electrical Characteristics (25°C unless otherwise noted)

PARAMETER		CONDITIONS		MIN	MAX	UNITS
I_{GSS}	Gate Reverse Current	V_{GS} = −30V, V_{DS} = 0			−250	pA
			150°C		−250	nA
BV_{GSS}	Gate-Source Breakdown Voltage	I_G = −1 μA, V_{DS} = 0		−40		V
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 20V, I_D = 1 nA		−0.7	−4	V
V_{GS}	Gate-Source Voltage	V_{DG} = 20V, I_D = 200 μA		−0.2	−3.8	V
I_G	Gate Operating Current				−100	pA
			125°C		−100	nA
I_{DSS}	Saturation Drain Current	V_{DS} = 20V, V_{GS} = 0, (Note 1)		0.5	7.5	mA
g_{fs}	Common-Source Forward Transconductance	V_{DS} = 20V, V_{GS} = 0, (Note 1)	f = 1 kHz	1000	4000	μmho
g_{fs}	Common-Source Forward Transconductance	V_{DG} = 20V, I_D = 200 μA, (Note 1)		500	1000	μmho
g_{os}	Common-Source Output Conductance	V_{DS} = 20V, V_{GS} = 0			10	μmho
g_{os}	Common-Source Output Conductance	V_{DG} = 20V, I_D = 200 μA			1	μmho
C_{iss}	Common-Source Input Capacitance	V_{DS} = 20V, V_{GS} = 0	f = 1 MHz		25	pF
C_{rss}	Common-Source Reverse Transfer Capacitance				5	pF
e_n	Equivalent Input Noise Voltage	V_{DG} = 20V, I_D = 200 μA	f = 10 Hz 2N5515–2N5519		30	$\frac{nV}{\sqrt{Hz}}$
			f = 10 Hz 2N5520–2N5524		15	$\frac{nV}{\sqrt{Hz}}$
			f = 1 kHz		10	$\frac{nV}{\sqrt{Hz}}$

Matching Characteristics

PARAMETER		CONDITIONS		2N5515, 2N5520 MIN	2N5515, 2N5520 MAX	2N5516, 2N5521 MIN	2N5516, 2N5521 MAX	2N5517, 2N5522 MIN	2N5517, 2N5522 MAX	2N5518, 2N5523 MIN	2N5518, 2N5523 MAX	2N5519, 2N5524 MIN	2N5519, 2N5524 MAX	UNITS
$\lvert I_{G1}-I_{G2}\rvert$	Differential Gate Current	V_{DG} = 20V, I_D = 200 μA	125°C		10		10		10		10		10	nA
$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio	V_{DS} = 20V, V_{GS} = 0, (Note 1)		0.95	1	0.95	1	0.95	1	0.95	1	0.90	1	
$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage	V_{DG} = 20V, I_D = 200 μA			5		5		10		15		15	mV
$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Voltage Differential Drift, (Note 1)		T_A = 25°C, T_B = 125°C		5		10		20		40		80	μV/°C
			T_A = −55°C, T_B = 25°C		5		10		20		40		80	μV/°C
$\lvert g_{os1}-g_{os2}\rvert$	Differential Output Conductance		f = 1 kHz		0.1		0.1		0.1		0.1		0.1	μmho
$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio, (Note 1)			0.97	1	0.97	1	0.95	1	0.95	1	0.90	1	
CMRR	Common-Mode Rejection Ratio, (Note 2)	V_{DD} = 10 to 20V, I_D = 200 μA		100		100		90						dB

Note 1: Pulse test required, pulse width = 300 μs, duty cycle ≤ 3%.

Note 2: CMRR = 20 $\log_{10} \Delta V_{DD}/\Delta\lvert V_{GS1}-V_{GS2}\rvert$, ($\Delta V_{DD}$ = 10V).

2N5545-47 N-Channel Monolithic Dual JFETs

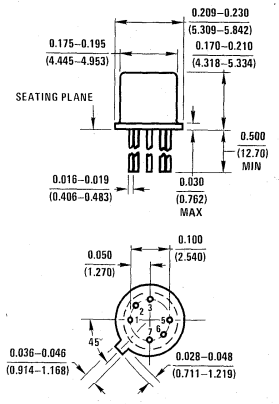
General Description

The 2N5545 thru 2N5547 series of monolithic dual JFETs is designed for low to medium frequency differential amplifiers requiring matched gate-source voltage, high common-mode rejection, and low output conductance.

Absolute Maximum Ratings (25°C)

Gate-Drain or Gate-Source Voltage	−50V
Gate Current	30 mA
Device Dissipation (Each Side), T_A = 25°C (Derate 1.67 mW/°C)	250 mW
Total Device Dissipation, T_A = 25°C (Derate 2.67 mW/°C)	400 mW
Storage Temperature Range	−65°C to +200°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-71



PIN	FET (12)
1	S1
2	D1
3	G1
5	S2
6	D2
7	G2

Electrical Characteristics (25°C unless otherwise noted)

PARAMETER		CONDITIONS		MIN	MAX	UNITS
I_{GSS}	Gate Reverse Current	V_{GS} = −30V, V_{DS} = 0			−100	pA
			150°C		−150	nA
BV_{GSS}	Gate-Source Breakdown Voltage	I_G = −1 μA, V_{DS} = 0		−50		V
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 15V, I_D = 0.5 nA		−0.5	−4.5	
I_G	Gate Operating Current	V_{DG} = 15V, I_D = 200 μA			−50	pA
I_{DSS}	Saturation Drain Current	V_{DS} = 15V, V_{GS} = 0		0.5	8	mA
g_{fs}	Common-Source Forward Transconductance	V_{DS} = 15V, V_{GS} = 0	f = 1 kHz	1500	6000	μmho
g_{os}	Common-Source Output Conductance				25	
C_{iss}	Common-Source Input Capacitance		f = 1 MHz		6	pF
C_{rss}	Common-Source Reverse Transfer Capacitance				2	
NF	Spot Noise Figure	V_{DG} = 15V, I_D = 200 μA	f = 10 Hz, R_G = 1 MΩ			dB
	2N5545				3.5	
	2N5546				5	
e_n	Equivalent Input Noise Voltage		f = 10 Hz			$\frac{nV}{\sqrt{Hz}}$
	2N5545				180	
	2N5546				200	

Matching Characteristics

PARAMETER		CONDITIONS		2N5545		2N5546		2N5547		UNITS
				MIN	MAX	MIN	MAX	MIN	MAX	
$\lvert I_{G1}-I_{G2}\rvert$	Differential Gate Current	V_{DG} = 15V, I_D = 200 μA	125°C		5		5		5	nA
$\frac{I_{DSS1}}{I_{DSS2}}$	Drain Current Ratio at Zero Gate Voltage	V_{DS} = 15V, V_{GS} = 0		0.95	1	0.90	1	0.90	1	
$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage	V_{DG} = 15V	I_D = 50 μA		5		10		15	mV
			I_D = 200 μA		5		10		15	
$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Voltage Differential Drift, (Note 1)	V_{DG} = 15V, I_D = 200 μA	T_A = 25°C, T_B = 125°C		10		20		40	μV/°C
			T_A = −55°C, T_B = 25°C		10		20		40	
$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio		f = 1 kHz	0.97	1	0.95	1	0.90	1	
$\lvert g_{os1}-g_{os2}\rvert$	Differential Output Conductance				1		2		3	μmho

Note 1: Measured at end points, T_A and T_B.

2N5564-66/NPD5564-66 N-Channel Monolithic Dual JFETs

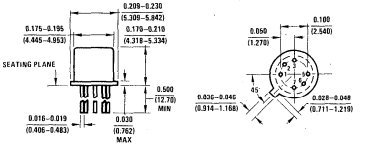
General Description

The 2N/NPD5564 thru 2N/NPD5566 series of N-channel monolithic dual JFETs is designed for broadband low noise differential amplifier or applications requiring dual matched moderate ON resistance analog switches.

Absolute Maximum Ratings (25°C)

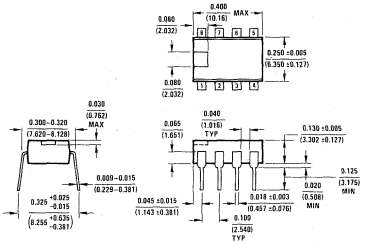
Gate-to-Gate Voltage	±40V
Gate-Drain or Gate-Source Voltage	−40V
Gate Current	50 mA
Device Dissipation (Each Side), T_A = 25°C (Derate 2.2 mW/°C)	325 mW
Total Device Dissipation, T_A = 25°C (Derate 3.3 mW/°C)	650 mW
Storage Temperature Range	−65°C to +200°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-71



PIN	FET
1	S1
2	D1
3	G1
5	S2
6	D2
7	G2

Molded Dual-In-Line Package (N)



PIN	FET
1	S1
2	D1
3	NC
4	G1
5	S2
6	D2
7	NC
8	G2

Electrical Characteristics (25°C unless otherwise noted)

	PARAMETER	CONDITIONS		MIN	MAX	UNITS
I_{GSS}	Gate-Reverse Current	V_{GS} = −20V, V_{DS} = 0			−100	pA
			150°C		−200	nA
BV_{GSS}	Gate-Source Breakdown Voltage	I_G = −1μA, V_{DS} = 0		−40		V
$V_{GS(OFF)}$	Gate-Source Cutoff Voltage	V_{DS} = 15V, I_D = 1 nA		−0.5	−3	
$V_{GS(f)}$	Gate-Source Voltage	V_{DS} = 0V, I_G = 2 mA			1.0	
I_{DSS}	Saturation Drain Current	V_{DS} = 15V, V_{GS} = 0, (Note 1)		5	30	mA
$r_{DS(ON)}$	Static Drain Source "ON" Resistance	I_D = 1 mA, V_{GS} = 0			100	Ω
g_{fs}	Common-Source Forward Transconductance (Note 1)	V_{DG} = 15V, I_D = 2 mA	f = 1 kHz	7500	12,500	μmho
			f = 100 MHz	7000		
g_{os}	Common-Source Output Conductance		f = 1 kHz		45	
C_{rss}	Common-Source Reverse Transfer Capacitance		f = 1 MHz		3	pF
C_{iss}	Common-Source Input Capacitance				12	
NF	Spot Noise Figure		f = 10 Hz, R_g = 1M		1.0	dB
e_n	Equivalent Input Noise Voltage		f = 10 Hz		50	$\frac{nV}{\sqrt{Hz}}$

Matching Characteristics

PARAMETER		CONDITIONS		NPD/2N5564		NPD/2N5565		NPD/2N5566		UNITS
				MIN	MAX	MIN	MAX	MIN	MAX	
$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio	V_{DS} = 15V, V_{GS} = 0, (Note 1)		0.95	1	0.95	1	0.95	1	
$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage	V_{DS} = 15V, I_D = 2 mA			5		10		20	mV
$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (Note 2)		T_A = 25°C, T_B = 125°C		10		25		50	μV/°C
			T_A = −55°C, T_B = 25°C		10		25		50	
$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio		f = 1 kHz	0.95	1	0.90	1	0.90	1	

Note 1: Pulse test required, pulse width 300 μs, duty cycle ≤ 3%.

Note 2: Measured at end points, T_A and T_B.

2N5638-40 N-Channel JFETs

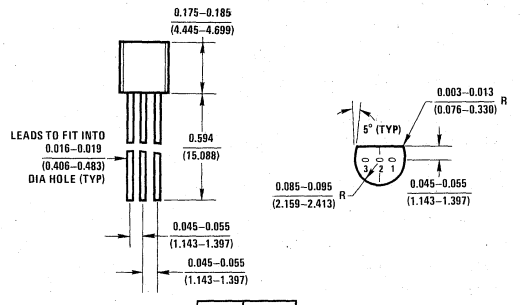
General Description

The 2N5638 thru 2N5640 series of N-channel JFETs is designed for analog switch applications requiring low ON resistance and moderate capacitance.

Absolute Maximum Ratings (25°C)

Drain-Source Breakdown Voltage	30V
Drain-Gate Breakdown Voltage	30V
Source-Gate Breakdown Voltage	30V
Forward Gate Current	10 mA
Total Device Dissipation at 25°C	310 mW
Derate above 25°C	2.82 mW/°C
Operating Junction Temperature Range	−65°C to +135°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-92

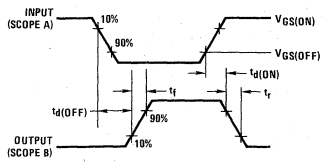


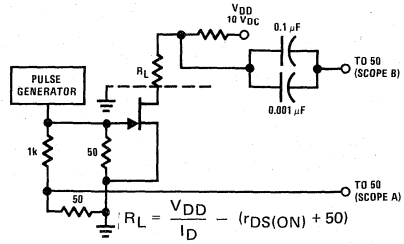
PIN	FET
1	G
2	S
3	D

Electrical Characteristics (25°C unless otherwise noted)

	PARAMETER	CONDITIONS			2N5638 MIN	2N5638 MAX	2N5639 MIN	2N5639 MAX	2N5640 MIN	2N5640 MAX	UNITS
BV_{GSS}	Gate Reverse Breakdown Voltage	$I_G = -10\,\mu A$, $V_{DS} = 0$			−30		−30		−30		V
I_{GSS}	Gate Reverse Current	$V_{GS} = -15V$, $V_{DS} = 0$				−1.0		−1.0		−1.0	nA
				$T_A = 100°C$		−1.0		−1.0		−1.0	μA
$I_{D(off)}$	Drain Cutoff Current	$V_{DS} = 15V$	$V_{GS} = -12V$, 2N5638 $V_{GS} = -8V$, 2N5639 $V_{GS} = -6V$, 2N5640			1.0		1.0		1.0	nA
				$T_A = 100°C$		1.0		1.0		1.0	μA
I_{DSS}	Saturation Drain Current	$V_{DS} = 20V$, $V_{GS} = 0$, (Note 1)			50		25		5.0		mA
$V_{DS(on)}$	Drain-Source ON Voltage	$V_{GS} = 0$	$I_D = 12$ mA, 2N5638 $I_D = 6$ mA, 2N5634 $I_D = 3$ mA, 2N5640			0.5		0.5		0.5	V
$r_{DS(on)}$	Static Drain-Source ON Resistance	$V_{GS} = 0$, $I_D = 1$ mA				30		60		100	Ω
$r_{ds(on)}$	Drain-Source ON Resistance	$V_{GS} = 0$, $I_D = 0$		f = 1 kHz		30		60		100	Ω
C_{iss}	Common-Source Input Capacitance	$V_{GS} = -12V$, $V_{DS} = 0$		f = 1 MHz		10		10		10	pF
C_{rss}	Common-Source Reverse Transfer Capacitance					4.0		4.0		4.0	pF
$t_{d(on)}$	Turn ON Delay Time	$V_{DD} = 10V$, $V_{GS(on)} = 0$, $V_{GS(off)} = -10V$, $R_G = 50\Omega$	$I_{D(on)} = 12$ mA, 2N5638			4.0		6.0		8.0	ns
t_r	Rise Time		$I_{D(on)} = 6$ mA, 2N5639			5.0		8.0		10	ns
t_d	Turn OFF Delay Time		$I_{D(on)} = 3$ mA, 2N5640			5.0		10		15	ns
t_f	Fall Time					10		20		30	ns

Note 1: Pulse test PW ≤ 300 μs, duty cycle ≤ 3%.





$$R_L = \frac{V_{DD}}{I_D} - (r_{DS(ON)} + 50)$$

Scope Tektronix 567A or equivalent

2N5902-09 N-Channel Monolithic Dual JFETs

General Description

The 2N5902 thru 2N5909 N-channel monolithic dual JFETs is designed for ultra-low leakage ($I_G < 1$ pA) differential amplifier applications.

Absolute Maximum Ratings (25°C)

Gate-to-Gate Voltage	±40V
Gate-Drain or Gate-Source Voltage	−40V
Gate Current	10 mA
Device Dissipation (Each Side), T_A = 25°C (Derate 3 mW/°C)	367 mW
Total Device Dissipation, T_A = 25°C (Derate 4 mW/°C)	500 mW
Storage Temperature Range	−65°C to +200°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

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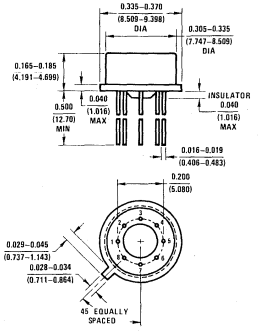

PIN	FET
1	S
2	D
3	G
4	Case
5	S
6	D
7	G
8	Sub

Electrical Characteristics (25°C unless otherwise noted)

	PARAMETER	CONDITIONS		2N5902-5 MIN	2N5902-5 MAX	2N5906-9 MIN	2N5906-9 MAX	UNITS
I_{GSS}	Gate Reverse Current	V_{GS} = −20V, V_{DS} = 0			−5		−2	pA
			125°C		−10		−5	nA
BV_{GSS}	Gate-Source Breakdown Voltage	I_G = −1 μA, V_{DS} = 0		−40		−40		V
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 10V, I_D = 1 nA		−0.6	−4.5	−0.6	−4.5	V
V_{GS}	Gate-Source Voltage	V_{DG} = 10V, I_D = 30 μA			−4		−4	V
I_G	Gate Operating Current				−3		−1	pA
			125°C		−3		−1	nA
I_{DSS}	Saturation Drain Current	V_{DS} = 10V, V_{GS} = 0		30	500	30	500	μA
g_{fs}	Common-Source Forward Transconductance		f = 1 kHz	70	250	70	250	μmho
g_{os}	Common-Source Output Conductance				5		5	
C_{iss}	Common-Source Input Capacitance		f = 1 MHz		3		3	pF
C_{rss}	Common-Source Reverse Transfer Capacitance				1.5		1.5	
g_{fs}	Common-Source Forward Transconductance	V_{DG} = 10V, I_D = 30 μA		50	150	50	150	μmho
g_{os}	Common-Source Output Conductance		f = 1 kHz		1		1	
e_n	Equivalent Short-Circuit Input Noise Voltage	V_{DS} = 10V, V_{GS} = 0			0.2		0.1	$\frac{\mu V}{\sqrt{Hz}}$
NF	Spot Noise Figure		f = 100 Hz, R_G = 10M		3		1	dB

Matching Characteristics

	PARAMETER	CONDITIONS		2N5902, 2N5906 MIN	2N5902, 2N5906 MAX	2N5903, 2N5907 MIN	2N5903, 2N5907 MAX	2N5904, 2N5908 MIN	2N5904, 2N5908 MAX	2N5905, 2N5909 MIN	2N5905, 2N5909 MAX	UNITS
$\lvert I_{G1}-I_{G2}\rvert$	Differential Gate Current	V_{DG} = 10V, I_D = 30 μA, T_A = 125°C	2N5902-5		2.0		2.0		2.0		2.0	nA
			2N5906-9		0.2		0.2		0.2		0.2	
$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio	V_{DS} = 10V, V_{GS} = 0		0.95	1	0.95	1	0.95	1	0.95	1	
$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio	V_{DG} = 10V, I_D = 30 μA	f = 1 kHz	0.97	1	0.97	1	0.95	1	0.95	1	
$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage				5		5		10		15	mV
$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (Measured at End Points T_A and T_B)		T_A = 25°C, T_B = 125°C		5		10		20		40	μV/°C
			T_A = −55°C, T_B = 25°C		5		10		20		40	
$\lvert g_{os1}-g_{os2}\rvert$	Differential Output Conductance		f = 1 kHz		0.2		0.2		0.2		0.2	μmho

2N5911, 2N5912 N-Channel Monolithic Dual JFETs

General Description

The 2N5911 thru 2N5912 series of N-channel monolithic dual JFETs is designed for wideband, low noise differential amplifiers.

Absolute Maximum Ratings (25°C)

Gate-to-Gate Voltage	±25V
Gate-Drain or Gate-Source Voltage	−25V
Gate Current	50 mA
Device Dissipation (Each Side), (Derate 3 mW/°C)	367 mW
Total Device Dissipation, (Derate 4 mW/°C)	500 mW
Storage Temperature Range	−65°C to +200°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

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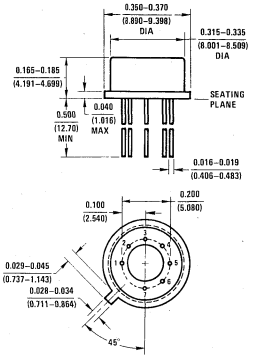

PIN	FET
1	S
2	D
3	G
4	Case
5	S
6	D
7	G

Electrical Characteristics (25° unless otherwise noted)

PARAMETER		CONDITIONS		MIN	MAX	UNITS
I_{GSS}	Gate Reverse Current	V_{GS} = −15V, V_{DS} = 0			−100	pA
			150°C		−250	nA
BV_{GSS}	Gate Reverse Breakdown Voltage	I_G = −1 μA, V_{DS} = 0		−25		V
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 10V, I_D = 1 nA		−1	−5	
V_{GS}	Gate-Source Voltage	V_{DG} = 10V, I_D = 5 mA		−0.3	−4	
I_G	Gate Operating Current				−100	pA
			125°C		−100	nA
I_{DSS}	Saturation Drain Current	V_{DS} = 10V, V_{GS} = 0V, (Note 1)		7	40	mA
g_{fs}	Common-Source Forward Transconductance	V_{DG} = 10V, I_D = 5 mA	f = 1 kHz	5000	10,000	μmho
g_{fs}	Common-Source Forward Transconductance		f = 100 MHz	5000	10,000	
g_{os}	Common-Source Output Conductance		f = 1 kHz		100	
g_{oss}	Common-Source Output Conductance		f = 100 MHz		150	
C_{iss}	Common-Source Input Capacitance		f = 1 MHz		5	pF
C_{rss}	Common-Source Reverse Transfer Capacitance				1.2	
e_n	Equivalent Short-Circuit Input Noise Voltage		f = 10 kHz		20	$\frac{nV}{\sqrt{Hz}}$
NF	Spot Noise Figure		f = 10 kHz, R_G = 100k		1	dB

Matching Characteristics

PARAMETER		CONDITIONS		2N5911 MIN	2N5911 MAX	2N5912 MIN	2N5912 MAX	UNITS
$\lvert I_{G1}-I_{G2}\rvert$	Differential Gate Current	V_{DG} = 10V, I_D = 5 mA	125°C		20		20	nA
$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio	V_{DS} = 10V, V_{GS} = 0, (Note 1)		0.95	1	0.95	1	
$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage	V_{DG} = 10V, I_D = 5 mA			10		15	mV
$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (Measured at End Points, T_A and T_B)		T_A = 25°C, T_B = 125°C		20		40	μV/°C
			T_A = −55°C, T_B = 25°C		20		40	
$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio		f = 1 kHz	0.95	1	0.95	1	

Note 1: Pulse width 300 μs, duty cycle ≤ 3%.

2N5949-53 N-Channel JFETs

General Description

The 2N5949 thru 2N5953 series of N-channel JFETs is characterized for low frequency to VHF amplifiers requiring tightly specified I_{DSS} ranges.

Absolute Maximum Ratings (25°C)

Reverse Gate-Drain or Gate-Source Voltage	30V
Gate Current	10 mA
Total Device Dissipation at 25°C Case Temperature (Derate 2.88 mW/°C)	360 mW
Total Device Dissipation at 25°C Lead Temperature (Derate 4 mW/°C)	500 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (1/16" from case for 10 seconds)	260°C

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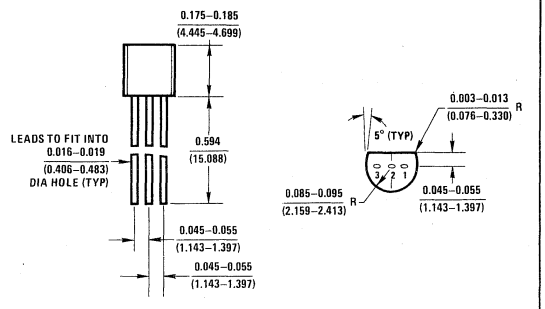


PIN	FET
1	S
2	D
3	G

Electrical Characteristics (25°C unless otherwise noted)

PARAMETER		CONDITIONS		2N5949		2N5950		2N5951		2N5952		2N5953		UNITS
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
I_{GSS}	Gate Reverse Current	V_{GS} = −15V, V_{DS} = 0			−1		−1		−1		−1		−1	nA
			T_A = 100°C		−200		−200		−200		−200		−200	
BV_{GSS}	Gate-Source Breakdown Voltage	I_G = −1 μA, V_{DS} = 0		−30		−30		−30		−30		−30		V
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 15V, I_D = 100 nA		−3	−7	−2.5	−6	−2	−5	−1.3	−3.5	−0.8	−3	V
V_{GS}	Gate-Source Voltage	V_{DS} = 15V	I_D = 1.2 mA	−2.25	−6									V
			I_D = 1 mA			−1.8	−5							
			I_D = 0.7 mA					−1.3	−4.5					
			I_D = 0.4 mA							−0.75	−3			
			I_D = 0.25 mA									−0.5	−2.5	
I_{DSS}	Saturation Drain Current	V_{DS} = 15V, V_{GS} = 0,	(Note 1)	12	18	10	15	7	13	4	8	2.5	5	mA
$r_{ds(on)}$	Drain-Source ON Resistance	V_{GS} = 0, I_D = 0	f = 1 kHz		200		210		250		300		375	Ω
g_{fs}	Common-Source Forward Transconductance	V_{DS} = 15V, V_{GS} = 0	f = 1 kHz	3.5	7.5	3.5	7.5	3.5	6.5	2	6.5	2	6.5	mmho
g_{os}	Common-Source Output Conductance				75		75		75		50		50	μmho
$Re(Y_{os})$	Common-Source Output Conductance	V_{DS} = 15V, V_{GS} = 0	f = 100 MHz		75		75		75		75		50	μmho
$Re(Y_{fs})$	Common-Source Transconductance			3.0	7.5	3.0	7.5	3.0	6.5	1.0	6.5	1.0	6.5	mmho
$Re(Y_{is})$	Common-Source Input Conductance				250		250		250		250		250	μmho
C_{iss}	Common-Source Input Capacitance	V_{DS} = 15V, V_{GS} = 0	f = 1 MHz		6		6		6		6		6	pF
C_{rss}	Common-Source Reverse Transfer Capacitance				2		2		2		2		2	pF
NF	Noise Figure	V_{DS} = 15V, V_{GS} = 0	f = 100 MHz, R_G = 1 kΩ		5		5		5		5		5	dB
			f = 1 kHz, R_G = 1 MΩ		2		2		2		2		2	
e_n	Equivalent Input Noise Voltage	V_{DS} = 15V, V_{GS} = 0	f = 1 kHz		100		100		100		100		100	$\frac{nV}{\sqrt{Hz}}$

Note 1: Pulse width 300 μs, duty cycle ≤ 3%.

2N6483-85 N-Channel Monolithic Dual JFETs

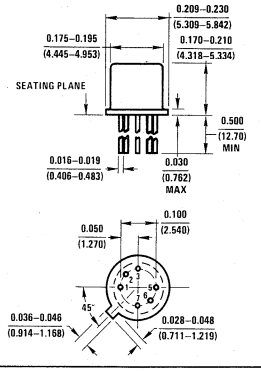
General Description

The 2N6483 thru 2N6485 series of N-channel monolithic dual JFETs is designed for low to medium frequency low noise differential amplifier applications requiring tight match and high common-mode rejection.

Absolute Maximum Ratings (25°C)

Gate-Drain or Gate-Source Voltage	−50V
Gate Current	50 mA
Device Dissipation (Each Side), T_A = 85°C (Derate 2.56 mW/°C)	250 mW
Total Device Dissipation, T_A = 85°C (Derate 4.3 mW/°C)	500 mW
Storage Temperature Range	−65°C to +200°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-71



PIN	FET (12)
1	S1
2	D1
3	G1
5	S2
6	D2
7	G2

Electrical Characteristics (25°C unless otherwise noted)

PARAMETER		CONDITIONS		MIN	MAX	UNITS
I_{GSS}	Gate Reverse Current	V_{GS} = −30V, V_{DS} = 0			−200	pA
			150°C		−200	nA
BV_{GSS}	Gate-Source Breakdown Voltage	I_G = −1 μA, V_{DS} = 0		−50		V
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 20V, I_D = 1 nA		−0.7	−4	
V_{GS}	Gate-Source Voltage	V_{DG} = 20V, I_D = 200 μA		−0.2	−3.8	
I_G	Gate Operating Current				−100	pA
			125°C		−100	nA
I_{DSS}	Saturation Drain Current	V_{DS} = 20V, V_{GS} = 0, (Note 1)		0.5	7.5	mA
g_{fs}	Common-Source Forward Transconductance	V_{DS} = 20V, V_{GS} = 0, (Note 1)	f = 1 kHz	1000	4000	μmho
g_{fs}	Common-Source Forward Transconductance	V_{DG} = 20V, I_D = 200 μA, (Note 1)		500	1500	
g_{os}	Common-Source Output Conductance	V_{DS} = 20V, V_{GS} = 0			10	
g_{os}	Common-Source Output Conductance	V_{DG} = 20V, I_D = 200 μA			1	
C_{iss}	Common-Source Input Capacitance	V_{DS} = 20V, V_{GS} = 0	f = 1 MHz		20	pF
C_{rss}	Common-Source Reverse Transfer Capacitance				3.5	
e_n	Equivalent Input Noise Voltage	V_{DS} = 20V, I_D = 200 μA	f = 100 Hz		5	$\frac{nV}{\sqrt{Hz}}$
			f = 10 Hz		10	

Matching Characteristics

PARAMETER		CONDITIONS		2N6483		2N6484		2N6485		UNITS
				MIN	MAX	MIN	MAX	MIN	MAX	
$\lvert I_{G1}-I_{G2}\rvert$	Differential Gate Current	V_{DG} = 20V, I_D = 200 μA	125°C		10		10		10	nA
$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio	V_{DS} = 20V, V_{GS} = 0, (Note 1)		0.95	1.0	0.95	1.0	0.95	1.0	
$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio, (Note 1)	V_{DG} = 20V, I_D = 200 μA	f = 1 kHz	0.95	1.0	0.95	1.0	0.95	1.0	
$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage				50		10		15	mV
$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Differential Voltage Change with Temperature, (Note 2)		T_A = 25°C, T_B = 125°C		5		10		25	μV/°C
			T_A = −55°C, T_B = 25°C		5		10		25	
$\lvert g_{os1}-g_{os2}\rvert$	Differential Output Conductance		f = 1 kHz		0.1		0.1		0.1	μmho
CMRR	Common-Mode Reject Ratio			100		100		100		dB

Note 1: Pulse test required, pulse width 300 μs, duty cycle ≤ 3%.
Note 2: Measured at end points, T_A and T_B.

J108-10 N-Channel JFETs

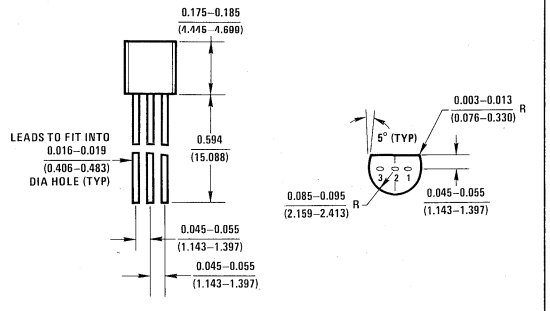
General Description

The J108 thru J110 series of N-channel JFETs is designed for analog switch applications requiring very low ON resistance.

Absolute Maximum Ratings (25°C)

Gate-Drain or Gate-Source Voltage	−25V
Gate Current	50 mA
Total Device Dissipation (25°C Free-Air Temperature)	350 mW
Power Derating (to +125°C)	3.5 mW/°C
Storage Temperature Range	−55°C to +150°C
Operating Temperature Range	−55°C to +150°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-92



PIN	FET
1	G
2	S
3	D

Electrical Characteristics (25°C unless otherwise noted)

PARAMETER		CONDITIONS		J108			J109			J110			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
I_{GSS}	Gate Reverse Current	V_{DS} = 0, V_{GS} = −15V, (Note 1)				−3			−3			−3	nA
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 5V, I_D = 1 μA		−3		−10	−2		−6	−0.5		−4	V
BV_{GSS}	Gate-Source Breakdown Voltage	V_{DS} = 0, I_G = −1 μA		−25			−25			−25			V
I_{DSS}	Saturation Drain Current	V_{DS} = 15V, V_{GS} = 0, (Note 2)		80			40			10			mA
$I_{D(off)}$	Drain Cutoff Current	V_{DS} = 5V, V_{GS} = −10V, (Note 1)				3			3			3	nA
$r_{DS(on)}$	Drain Source ON Resistance	$V_{DS} \leq 0.1V$, V_{GS} = 0				8			12			18	Ω
$C_{dg(off)}$	Drain Gate OFF Capacitance	V_{DS} = 0, V_{GS} = −10V	f = 1 MHz			15			15			15	pF
$C_{sg(off)}$	Source Gate OFF Capacitance					15			15			15	pF
$C_{dg(on)}$ + $C_{sg(on)}$	Drain Gate Plus Source Gate ON Capacitance	V_{DS} = V_{GS} = 0				85			85			85	pF
$t_{d(on)}$	Turn ON Delay Time	Switching Time Test Conditions			4			4			4		ns
t_r	Rise Time		J108 J109 J110		1			1			1		ns
$t_{d(off)}$	Turn OFF Delay Time	V_{DD} 1.5V 1.5V 1.5V V_{GS} −12V −7V −5V			6			6			6		ns
t_f	Fall Time	R_L 150Ω 150Ω 150Ω			30			30			30		ns

Note 1: Approximately doubles for every 10°C increase in T_A.
Note 2: Pulse test duration = 300 μs, duty cycle ≤ 3%.

J111-13 N-Channel JFETs

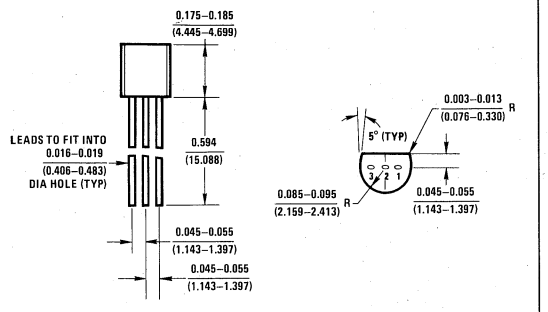
General Description

The J111 thru J113 series of N-channel JFETs is designed for analog switch applications requiring low ON resistance and moderate capacitance.

Absolute Maximum Ratings (25°C)

Gate-Drain or Gate-Source Voltage	−35V
Gate Current	50 mA
Total Device Dissipation (25°C Free-Air Temperature)	350 mW
Power Derating (to +125°C)	3.5 mW/°C
Storage Temperature Range	−55°C to +150°C
Operating Temperature Range	−55°C to +150°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-92



PIN	FET
1	G
2	S
3	D

Electrical Characteristics (25°C unless otherwise noted)

PARAMETER		CONDITIONS		J111			J112			J113			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
I_{GSS}	Gate Reverse Current	V_{DS} = 0, V_{GS} = −15V, (Note 1)				−1			−1			−1	nA
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 5V, I_D = 1 μA		−3		−10	−1		−5	−0.5		−3	V
BV_{GSS}	Gate-Source Breakdown Voltage	V_{DS} = 0, I_G = −1 μA		−35			−35			−35			V
I_{DSS}	Saturation Drain Current	V_{DS} = 15V, V_{GS} = 0, (Note 2)		20			5			2			mA
$I_{D(off)}$	Drain Cutoff Current	V_{DS} = 5V, V_{GS} = −10V, (Note 1)				1			1			1	nA
$r_{DS(on)}$	Drain Source ON Resistance	$V_{DS} \leq 0.1V$, V_{GS} = 0				30			50			100	Ω
$C_{dg(off)}$	Drain Gate OFF Capacitance	V_{DS} = 0, V_{GS} = −10V	f = 1 MHz			5			5			5	pF
$C_{sg(off)}$	Source Gate OFF Capacitance					5			5			5	
$C_{dg(on)}$ + $C_{sg(on)}$	Drain Gate Plus Source Gate ON Capacitance	V_{DS} = V_{GS} = 0				28			28			28	
$t_{d(on)}$	Turn ON Delay Time	Switching Time Test Conditions			7			7			7		ns
t_r	Rise Time	V_{DD} 10V 10V 10V			6			6			6		
$t_{d(off)}$	Turn OFF Delay Time	V_{GS} −12V −7V −5V			20			20			20		
t_f	Fall Time	R_L 800Ω 1600Ω 3200Ω			15			15			15		

Note 1: Approximately doubles for every 10°C increase in T_A.
Note 2: Pulse test duration = 300 μs, duty cycle ≤ 3%.

J174-77 P-Channel JFETs

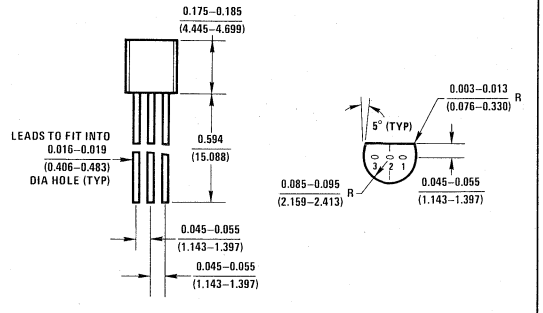
General Description

The J174 thru J177 series of P-channel JFETs is designed for low ON resistance analog switch applications.

Absolute Maximum Ratings (25°C)

Gate-Drain or Gate-Source Voltage, (Note 1)	30V
Gate Current	50 mA
Total Device Dissipation (25°C Free-Air Temperature)	350 mW
Power Derating (to +125°C)	3.5 mW/°C
Storage Temperature Range	−55°C to +150°C
Operating Temperature Range	−55°C to +150°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-92



PIN	FET
1	S
2	G
3	D

Electrical Characteristics (25°C unless otherwise noted)

PARAMETER		CONDITIONS		J174			J175			J176			J177			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
I_{GSS}	Gate Reverse Current	V_{DS} = 0, V_{GS} = 20V, (Note 2)				1			1			1			1	nA
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = −15V, I_D = −10 nA		5		10	3		6	1		4	0.8		2.25	V
BV_{GSS}	Gate-Source Breakdown Voltage	V_{DS} = 0, I_G = 1 μA		30			30			30			30			
I_{DSS}	Saturation Drain Current	V_{DS} = −15V, V_{GS} = 0, (Note 3)		−20		−100	−7		−60	−2		−25	−1.5		−20	mA
$I_{D(off)}$	Drain Cutoff Current	V_{DS} = −15V, V_{GS} = 10V, (Note 2)				−1			−1			−1			−1	nA
$r_{DS(on)}$	Drain Source ON Resistance	$V_{DS} \leq$ 0.1V, V_{GS} = 0				85			125			250			300	Ω
$C_{dg(off)}$	Drain Gate OFF Capacitance	V_{DS} = 0, V_{GS} = 10V	f = 1 MHz		5.5			5.5			5.5			5.5		pF
$C_{sg(off)}$	Source Gate OFF Capacitance				5.5			5.5			5.5			5.5		
$C_{dg(on)}$ + $C_{sg(on)}$	Drain Gate Plus Source Gate ON Capacitance	V_{DS} = V_{GS} = 0			40			40			40			40		
$t_{d(on)}$	Turn ON Delay Time	Switching Time Test Conditions			2			5			15			20		ns
t_r	Rise Time		J174 J175 J176 J177		5			10			20			25		
$t_{d(off)}$	Turn OFF Delay Time	V_{DD}	−10V −6V −6V −6V		5			10			15			20		
t_f	Fall Time	$V_{GS(off)}$	12V 8V 6V 3V		10			20			20			25		
		R_L	560Ω 12 kΩ 5.6 kΩ 10 kΩ													

Note 1: Geometry is symmetrical. Units may be operated with source and drain leads interchanged.

Note 2: Approximately doubles for every 10°C increase in T_A.

Note 3: Pulse test duration = 300 μs; duty cycle ≤ 3%.

J201-03 N-Channel JFETs

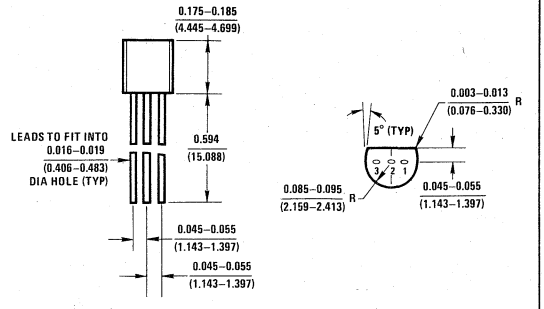
General Description

The J201 thru J203 series of N-channel JFETs is designed for low to medium frequency amplifiers requiring low input current and input noise voltage.

Absolute Maximum Ratings (25°C)

Gate-Drain or Gate-Source Voltage, (Note 1)	−40V
Gate Current	50 mA
Total Device Dissipation (25°C Free-Air Temperature)	350 mW
Power Derating (to +125°C)	3.5 mW/°C
Storage Temperature Range	−55°C to +150°C
Operating Temperature Range	−55°C to +150°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-92



PIN	FET
1	G
2	S
3	D

Electrical Characteristics (25°C unless otherwise noted)

PARAMETER		CONDITIONS		J201			J202			J203			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
I_{GSS}	Gate Reverse Current	V_{DS} = 0, V_{GS} = −20V, (Note 2)				−100			−100			−100	pA
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 20V, I_D = 10 nA		−0.3		−1.5	−0.8		−4.0	−2.0		−10.0	V
BV_{GSS}	Gate-Source Breakdown Voltage	V_{DS} = 0, I_G = −1 μA		−40			−40			−40			
I_{DSS}	Saturation Drain Current	V_{DS} = 20V, V_{GS} = 0, (Note 3)		0.2		1.0	0.9		4.5	4.0		20	mA
I_G	Gate Current	V_{DG} = 20V, I_D = $I_{DSS(MIN)}$			−35			−35			−35		pA
g_{fs}	Common-Source Forward Transconductance, (Note 3)	V_{DS} = 20V, V_{GS} = 0	f = 1 kHz	500			1000			1500			μmho
g_{os}	Common-Source Output Conductance				1			3.5			10		
C_{iss}	Common-Source Input Capacitance		f = 1 MHz		5			5			5		pF
C_{rss}	Common-Source Reverse Transfer Capacitance				2			2			2		
e_n	Equivalent Short-Circuit Input Noise Voltage	V_{DS} = 10V, V_{GS} = 0	f = 1 kHz		10			10			10		$\frac{nV}{\sqrt{Hz}}$

Note 1: Geometry is symmetrical. Units may be operated with source and drain leads interchanged.
Note 2: Approximately doubles for every 10°C increase in T_A.
Note 3: Pulse test duration = 2 ms.

J210-12 N-Channel JFETs

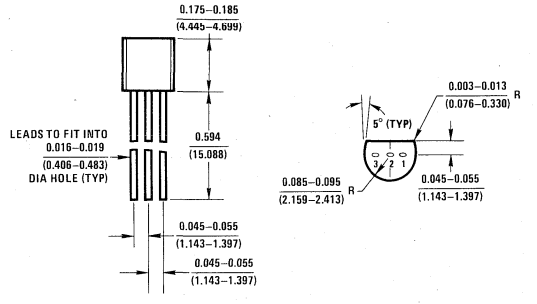
General Description

The J210 thru J212 series of N-channel JFETs is characterized for low to medium frequency amplifiers requiring high transconductance and low input capacitance.

Absolute Maximum Ratings (25°C)

Gate-Drain or Gate-Source Voltage	−25V
Gate Current	10 mA
Total Device Dissipation (25°C Free-Air Temperature)	350 mW
Power Derating (to +125°C)	3.5 mW/°C
Storage Temperature Range	−55°C to +150°C
Operating Temperature Range	−55°C to +150°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-92



PIN	FET
1	G
2	S
3	D

Electrical Characteristics (25°C unless otherwise noted)

PARAMETER		CONDITIONS		J210			J211			J212			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
I_{GSS}	Gate Reverse Current	V_{DS} = 0, V_{GS} = −15V, (Note 1)				−100			−100			−100	pA
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 15V, I_D = 1 nA		−1		−3	−2.5		−4.5	−4		−6	V
BV_{GSS}	Gate-Source Breakdown Voltage	V_{DS} = 0, I_G = −1 μA		−25			−25			−25			
I_{DSS}	Saturation Drain Current	V_{DS} = 15V, V_{GS} = 0, (Note 2)		2		15	7		20	15		40	mA
I_G	Gate Current	V_{DG} = 10V, I_D = 1 mA			−10			−10			−10		pA
g_{fs}	Common-Source Forward Transconductance, (Note 2)	V_{DS} = 15V, V_{GS} = 0	f = 1 kHz	4000		12000	7000		12000	7000		12000	μmho
g_{os}	Common-Source Output Conductance					150			200			200	
C_{iss}	Common-Source Input Capacitance		f = 1 MHz		5.0			5.0			5.0		pF
C_{rss}	Common-Source Reverse Transfer Capacitance				1.5			1.5			1.5		
e_n	Equivalent Short-Circuit Input Noise Voltage		f = 1 kHz		10			10			10		$\frac{nV}{\sqrt{Hz}}$

Note 1: Approximately doubles for every 10°C increase in T_A.
Note 2: Pulse test duration = 2 ms.

J270, J271 P-Channel JFETs

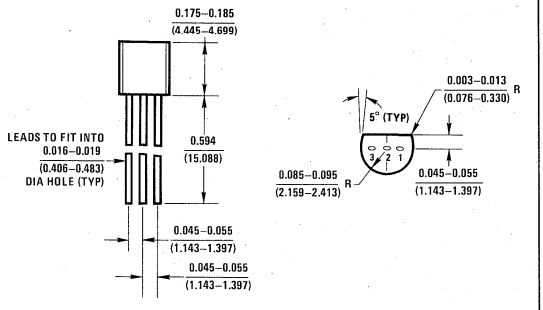
General Description

The J270 thru J271 series of P-channel JFETs is characterized for low to medium frequency small-signal amplifiers which require high transconductance and low input noise voltage.

Absolute Maximum Ratings (25°C)

Gate-Drain or Gate-Source Voltage, (Note 1)	30V
Gate Current	−50 mA
Total Device Dissipation (25°C Free-Air Temperature)	350 mW
Power Derating (to +125°C)	3.5 mW/°C
Storage Temperature Range	−55°C to +150°C
Operating Temperature Range	−55°C to +150°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-92



PIN	FET
1	S
2	G
3	D

Electrical Characteristics (25°C unless otherwise noted)

PARAMETER		CONDITIONS		J270 MIN	J270 TYP	J270 MAX	J271 MIN	J271 TYP	J271 MAX	UNITS
I_{GSS}	Gate Reverse Current	V_{DS} = 0, V_{GS} = 20V, (Note 2)				200			200	pA
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = −15V, I_D = −1 nA		0.5		2.0	1.5		4.5	V
BV_{GSS}	Gate-Source Breakdown Voltage	V_{DS} = 0, I_G = 1 μA		30			30			V
I_{DSS}	Saturation Drain Current	V_{DS} = −15V, V_{GS} = 0, (Note 3)		−2		−15	−6		−50	mA
I_G	Gate Current	V_{DG} = −15V, I_D = $I_{DSS(MIN)}$			15			60		pA
g_{fs}	Common-Source Forward Transconductance, (Note 3)	V_{DS} = −15V, V_{GS} = 0	f = 1 kHz	6000		15000	8000		18000	μmho
g_{os}	Common-Source Output Conductance					200			500	μmho
C_{iss}	Common-Source Input Capacitance		f = 1 MHz		20			20		pF
C_{rss}	Common-Source Reverse Transfer Capacitance				5			5		pF
e_n	Equivalent Short-Circuit Input Noise Voltage	V_{DS} = −10V, I_D = $I_{DSS(MIN)}$	f = 1 kHz		10			10		$\frac{nV}{\sqrt{Hz}}$

Note 1: Geometry is symmetrical. Units may be operated with source and drain leads interchanged.
Note 2: Approximately doubles for every 10°C increase in T_A.
Note 3: Pulse test duration = 2 ms.

J300 N-Channel JFET

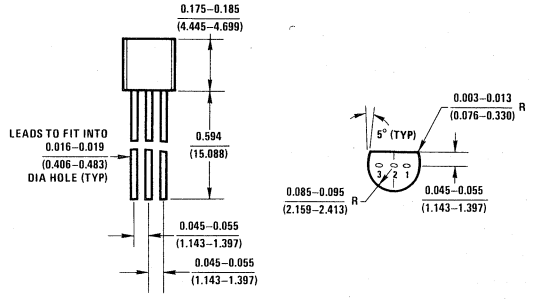
General Description

The J300 N-channel JFET is designed for VHF/UHF common-source or common-gate amplifier, oscillator and mixer applications.

Absolute Maximum Ratings (25°C)

Gate-Drain or Gate-Source Voltage	−25V
Gate Current	10 mA
Total Device Dissipation (25°C Free-Air Temperature)	350 mW
Power Derating (to +125°C)	3.5 mW/°C
Storage Temperature Range	−55°C to +150°C
Operating Temperature Range	−55°C to +150°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-92



PIN	FET
1	G
2	S
3	D

Electrical Characteristics (25°C unless otherwise noted)

PARAMETER		CONDITIONS		J300 MIN	J300 TYP	J300 MAX	UNITS
I_{GSS}	Gate Reverse Current	V_{GS} = −15V, V_{DS} = 0, (Note 1)				−500	pA
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 10V, I_D = 1 nA		−1		−6	V
BV_{GSS}	Gate-Source Breakdown Voltage	V_{DS} = 0, I_G = −1 μA		−25			
I_{DSS}	Saturation Drain Current	V_{DS} = 10V, V_{GS} = 0, (Note 2)		6		30	mA
$V_{GS(f)}$	Gate-Source Forward Voltage	I_G = 1 mA, V_{DS} = 0				1	V
g_{fs}	Common-Source Forward Transconductance, (Note 2)	V_{DG} = 10V, I_D = 5 mA	f = 1 kHz	4500		9000	μmho
g_{os}	Common-Source Output Transconductance					200	
C_{iss}	Common-Source Input Capacitance	V_{DG} = 10V, I_D = 5 mA	f = 1 MHz		3.5	5.5	pF
C_{rss}	Common-Source Reverse Transfer Capacitance				0.8	1.7	
C_{oss}	Common-Source Output Capacitance				1.5		
$\|y_{fs}\|$	Common-Source Forward Transadmittance	V_{DG} = 15V, I_D = 5 mA	f = 100 MHz		6200		μmho
			f = 450 MHz		6000		
$\|y_{fg}\|$	Common-Gate Forward Transadmittance		f = 100 MHz		6000		
			f = 450 MHz		5500		
G_{fg}	Common-Gate Power Gain		f = 100 MHz, (Note 3)		17		dB
NF	Noise Figure (Single Sideband)				2		

Note 1: Approximately doubles for every 10°C increase in T_A.
Note 2: Pulse test duration = 2 ms.
Note 3: Typical values for performance at 100 MHz in a common-gate circuit operating 3 dB bandwidth is 2 MHz.

J304, J305 N-Channel JFETs

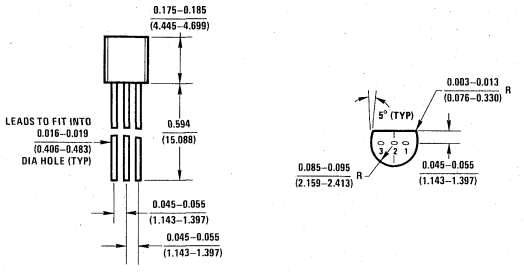
General Description

The J304 thru J305 N-channel JFETs are designed for low input capacitance VHF amplifier, oscillator and mixer applications.

Absolute Maximum Ratings (25°C)

Gate-Drain or Gate-Source Voltage	−30V
Gate Current	10 mA
Total Device Dissipation (25°C Free-Air Temperature)	350 mW
Power Derating (to +125°C)	3.5 mW/°C
Storage Temperature Range	−55°C to +150°C
Operating Temperature Range	−55°C to +150°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-92



PIN	FET
1	G
2	S
3	D

Electrical Characteristics (25°C unless otherwise noted)

PARAMETER		CONDITIONS		J304 MIN	J304 TYP	J304 MAX	J305 MIN	J305 TYP	J305 MAX	UNITS
I_{GSS}	Gate Reverse Current	V_{DS} = 0, V_{GS} = −20V, (Note 1)				−100			−100	pA
$V_{GS(off)}$	Gate Source Cutoff Voltage	V_{DS} = 15V, I_D = 1 nA		−2		−6	−0.5		−3	V
BV_{GSS}	Gate Source Breakdown Voltage	V_{DS} = 0, I_G = −1 μA		−30			−30			V
I_{DSS}	Saturation Drain Current	V_{DS} = 15V, V_{GS} = 0, (Note 2)		5		15	1		8	mA
g_{fs}	Common-Source Forward Transconductance, (Note 2)	V_{DS} = 15V, V_{GS} = 0	f = 1 kHz	4500		7500	3000			μmho
g_{os}	Common-Source Output Transconductance					50			50	μmho
C_{iss}	Common-Source Input Capacitance		f = 1 MHz		3.0			3.0		pF
C_{rss}	Common-Source Reverse Transfer Capacitance				0.8			0.8		pF
C_{oss}	Common-Source Output Capacitance				1.0			1.0		pF
g_{fs}	Common-Source Forward Transconductance	V_{DS} = 15V, V_{GS} = 0	f = 100 MHz					3000		μmho
			f = 400 MHz		4200					μmho
g_{oss}	Common-Source Output Conductance		f = 100 MHz		60			60		μmho
			f = 400 MHz		80					μmho
b_{oss}	Common-Source Output Susceptance		f = 100 MHz		800			800		μmho
			f = 400 MHz		3600					μmho
g_{iss}	Common-Source Input Conductance		f = 100 MHz		80			80		μmho
			f = 400 MHz		800					μmho
b_{iss}	Common-Source Input Susceptance		f = 100 MHz		2000			2000		μmho
			f = 400 MHz		7500					μmho
G_{ps}	Common-Source Power Gain	V_{DS} = 15V, I_D = 5 mA	f = 100 MHz		20					dB
			f = 400 MHz		11					dB
NF	Noise Figure (Single Sideband)	V_{DS} = 15V, I_D = 5 mA, R_G = 1 kΩ	f = 100 MHz		1.7					dB
			f = 400 MHz		3.8					dB

Note 1: Approximately doubles for every 10°C increase in T_A.
Note 2: Pulse test duration = 2 ms.

J308-10 N-Channel JFETs

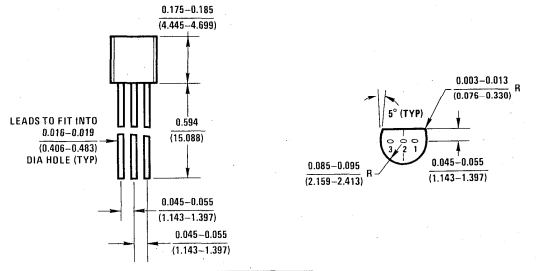
General Description

The J308 thru J310 series of N-channel JFETs is designed for VHF amplifier, oscillator and mixer applications.

Absolute Maximum Ratings

Drain-Gate Voltage	25V
Source-Gate Voltage	25V
Forward Gate Current	10 mA
Total Device Dissipation @ 25°C	350 mW
(Derate above 25°C)	3.5 mW/°C
Storage Temperature Range	−55°C to +150°C
Operating Junction Temperature Range	−55°C to +150°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-92



PIN	FET
1	G
2	S
3	D

Electrical Characteristics (25°C unless otherwise noted)

PARAMETER		CONDITIONS		J308			J309			J310			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
BV_{GSS}	Gate-Source Breakdown Voltage	V_{DS} = 0, I_G = −1 μA		−25			−25			−25			V
I_{GSS}	Gate Reverse Current	V_{GS} = −15V, V_{DS} = 0				−1.0			−1.0			−1.0	nA
			T = 125°C			−1.0			−1.0			−1.0	μA
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 10V, I_D = 1 nA		−1.0		−6.5	−1.0		−4.0	−2.0		−6.5	V
I_{DSS}	Saturation Drain Current	V_{GS} = 0, V_{DS} = 10V, (Note 1)		12		60	12		30	24		60	mA
$V_{GS(f)}$	Gate-Source Forward Voltage	V_{DS} = 0, I_G = 1 mA				1.0			1.0			1.0	V
g_{fs}	Common-Source Forward Transconductance	V_{DS} = 10V, I_D = 10 mA	f = 1 kHz	8000		20000	10000		20000	8000		18000	μmhos
g_{os}	Common-Source Output Conductance					200			150			200	
g_{fg}	Common-Gate Forward Transconductance				13000			13000			12000		
g_{og}	Common-Gate Output Conductance				150			100			150		
C_{gd}	Gate-Drain Capacitance	V_{GS} = −10V, V_{DS} = 0	f = 1 MHz		1.8	2.5		1.8	2.5		1.8	2.5	pF
C_{gs}	Gate-Source Capacitance				4.3	5.0		4.3	5.0		4.3	5.0	
e_n	Equivalent Short-Circuit Input Noise Voltage	V_{DS} = 10V, I_D = 10 mA	f = 100 Hz		10			10			10		$\frac{nV}{\sqrt{Hz}}$
$Re_{(y_{fs})}$	Common-Source Forward Transconductance	V_{DS} = 10V, I_D = 10 mA	f = 100 MHz		12			12			12		mmho
$Re_{(y_{ig})}$	Common-Gate Input Conductance				12			12			12		
$Re_{(y_{is})}$	Common-Source Input Conductance				0.7			0.7			0.5		
$Re_{(y_{os})}$	Common-Source Output Conductance				0.25			0.25			0.25		
G_{pg}	Common-Gate Power Gain				16			16			16		dB
NF	Noise Figure				1.5			1.5			1.5		

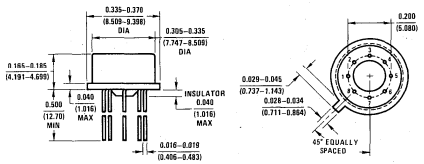
Note 1: Pulse test PW 300 μs, duty cycle ≤ 3%.

NDF9401-10 N-Channel Monolithic Cascode Dual JFETs

General Description

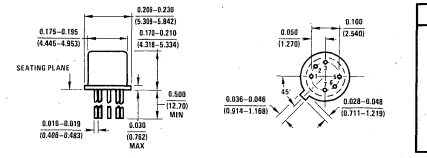
The NDF9401 thru NDF9410 series of N-channel monolithic cascode duals is designed for broadband low noise differential amplifier applications requiring tight match, low capacitance, and very high common-mode rejection.

TO-99 NDF9401–NDF9405 Series



PIN	FET
1	S
2	D
3	G
4	Case
5	S
6	D
7	G
8	Sub

TO-71 NDF9406–NDF9410 Series



PIN	FET
1	S1
2	D1
3	G1
5	S2
6	D2
7	G2

Absolute Maximum Ratings (25°C)

Gate-Drain or Gate-Source Voltage	−50V
Gate Current	10 mA
Device Dissipation (Each Side), T_A = 85°C (Derate 2 mW/°C)	250 mW
Total Device Dissipation, T_A = 85°C (Derate 3 mW/°C)	375 mW
Storage Temperature Range	−65°C to +200°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

Electrical Characteristics (25°C unless otherwise noted)

PARAMETER		CONDITIONS		MIN	MAX	UNITS
I_{GSS}	Gate Reverse Current	V_{GS} = −30V, V_{DS} = 0			−10	pA
			150°C		−25	nA
BV_{GSS}	Gate-Source Breakdown Voltage	I_G = −1 μA, V_{DS} = 0		−50		V
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 20V, I_D = 1 μA		0.5	4.0	
I_G	Gate Operating Current	V_{DG} = 35V, I_D = 200 μA			−5	pA
			125°C		−10	nA
I_{DSS}	Saturation Drain Current	V_{DS} = 20V, V_{GS} = 0, (Note 1)		0.5	10	mA
g_{fs}	Common-Source Forward Transconductance	V_{DG} = 20V, I_D = 200 μA, (Note 1)	f = 1 kHz	900	2000	μmho
g_{os}	Common-Source Output Conductance	V_{DG} = 20V, I_D = 200 μA			1	
C_{iss}	Common-Source Input Capacitance	V_{DS} = 20V, V_{GS} = 0	f = 1 MHz		6	pF
C_{rss}	Common-Source Reverse Transfer Capacitance				0.1	
e_n	Equivalent Input Noise Voltage	V_{DG} = 20V, I_D = 200 μA	f = 10 Hz		30	$\frac{nV}{\sqrt{Hz}}$

Matching Characteristics

PARAMETER		CONDITIONS		NDF9401, NDF9406		NDF9402, NDF9407		NDF9403, NDF9408		NDF9404, NDF9409		NDF9405, NDF9410		UNITS
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$\lvert I_{G1}-I_{G2}\rvert$	Differential Gate Current	V_{DG} = 20V, I_D = 200 μA	125°C		1		1		1		1		1	nA
$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio	V_{DS} = 20V, V_{GS} = 0, (Note 1)		0.95	1	0.95	1	0.95	1	0.95	1	0.90	1	
$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage	V_{DG} = 20V, I_D = 200 μA			5		5		10		15		25	mV
$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Voltage Differential Drift, (Note 1)		T_A = 25°C, T_B = 125°C		5		10		10		10		25	μV/°C
			T_A = −55°C, T_B = 25°C		5		10		10		10		25	
$\lvert g_{os1}-g_{os2}\rvert$	Differential Output Conductance		f = 1 kHz		0.1		0.1		0.1		0.1		0.1	μmho
$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio, (Note 1)			0.97	1	0.97	1	0.95	1	0.95	1	0.90	1	
CMRR	Common-Mode Rejection Ratio	V_{DD} = 10–20V, I_D = 200 μA, (Note 2)		120		120		110		110		100		dB

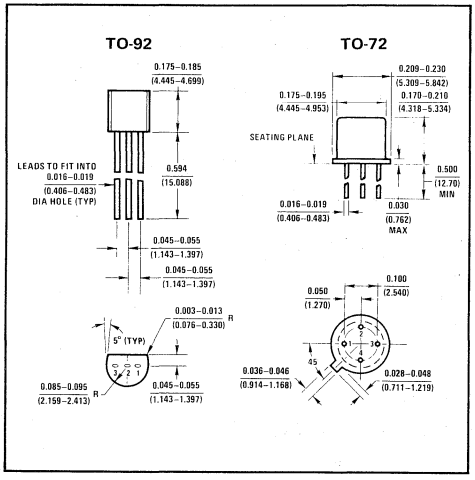
Note 1: Pulse test required, pulse width = 300 μs, duty cycle ≤ 3%.

Note 2: CMRR = 20 $\log_{10} \Delta V_{DD}/\Delta\lvert V_{GS1}-V_{GS2}\rvert$, ($\Delta V_{DD}$ = 10V).

NF5101-03/PF5101-03 N-Channel JFETs

General Description

The NF5101-3 (TO-72) and PF5101-3 (TO-92) are N-channel silicon Junction Field-Effect Transistors designed for ultra-low noise preamplifier applications, particularly hydrophones, particle detectors, high quality mic/phono/tape, video, vidicon and I-R sensor preamplifiers.



Absolute Maximum Ratings

Drain-Gate Voltage	40V
Reverse Gate-Source Voltage	40V
Forward Gate Current	10 mA
Device Dissipation @ 25°C	310 mW
Derate Above 25°C	2.82 mW/°C
Operating Temperature Range	−65 to +150°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

Electrical Characteristics

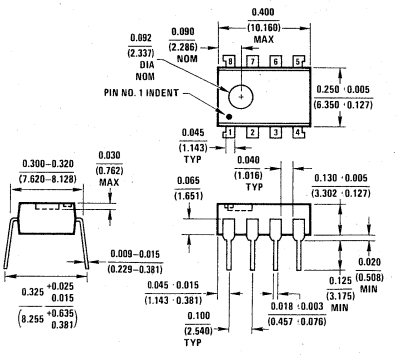
PARAMETER		CONDITIONS		PF/NF5101			PF/NF5102			PF/NF5103			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
BV_{GSS}	Gate-Source Breakdown Voltage	$I_G = 1\mu A$, $V_{DS} = 0V$		40			40			40			V
I_{GSS}	Gate Reverse Current	$V_{GS} = -15V$, $T_A = 25°C$				0.2			0.2			0.2	nA
		$V_{DS} = 0V$ $T_A = 125°C$				0.5			0.5			0.5	μA
$V_{GS(OFF)}$	Gate-Source Cutoff Voltage	$V_{DS} = 15V$, $I_D = 1$ nA		0.5		1.1	0.7		1.6	1.2		2.7	V
I_{DSS}	Saturation Drain Current	$V_{DS} = 15V$, $V_{GS} = 0V$, Pulsed $300\mu s \leq 2\%$		1.0		12	4.0		20	10		40	mA
g_{fs}	Common-Source Transconductance	$V_{DG} = 15V$	$I_D = 0.5$ mA	3.5	5		3.5	5		3.5	4.5		mmho
			$I_D = 2$ mA				7.5	9		7.5	9		mmho
g_{os}	Common-Source Output Conductance	$V_{DG} = 15V$, $I_D = 0.5$ mA			5	25		5	25		5	25	μmho
C_{iss}	Common-Source Input Capacitance	$V_{DG} = 15V$, $V_{GS} = 0V$			12	16		12	16		12	16	pF
C_{rss}	Common-Source Reverse Transfer Capacitance	$V_{DG} = 15V$, $V_{GS} = 0V$			4	6		4	6		4	6	pF
NF	Common-Source Spot Noise Figure	$V_{DG} = 15V$, $I_D = 0.5$ mA, $R_G = 20$ kΩ, f = 10 Hz			1.5			1.5			1.5		dB
e_n	Equivalent Short Circuit Input Noise Voltage	$V_{DG} = 10V$, f = 10 Hz	$I_D = 0.5$ mA		7	20		8	20		10	25	$nV/\sqrt{Hz}$
			$I_D = 2$ mA						15			20	$nV/\sqrt{Hz}$
		$V_{DG} = 10V$, f = 1 kHz	$I_D = 0.5$ mA			3.5			3.5			3.5	$nV/\sqrt{Hz}$
			$I_D = 2$ mA						3			3	$nV/\sqrt{Hz}$

NPD8301-03 N-Channel Monolithic Dual JFETs

General Description

The NPD8301 thru NPD8303 series of N-channel monolithic dual JFETs is designed for low cost, high performance differential amplifiers requiring tightly matched gate-source voltage, low drift, high common-mode rejection, and low output conductance.

Molded Dual-In-Line Package (N)



PIN	FET
1	S1
2	D1
3	NC
4	G1
5	S2
6	D2
7	NC
8	G2

Absolute Maximum Ratings (25°C)

Gate-to-Gate Voltage	±40V
Gate-Drain or Gate-Source Voltage	−40V
Gate Current	50 mA
Total Package Dissipation (25°C Free-Air)	350 mW
Power Derating (to +125°C)	3.5 mW/°C
Storage Temperature Range	−55°C to +125°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

Electrical Characteristics (25°C unless otherwise noted)

PARAMETER		CONDITIONS		NPD8301			NPD8302			NPD8303			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
I_{GSS}	Gate Reverse Current	V_{DS} = 0, V_{GS} = −20V, (Note 1)				−100			−100			−100	pA
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 20V, I_D = 1 nA		−0.5		−3.5	−0.5		−3.5	−0.5		−3.5	V
BV_{GSS}	Gate-Source Breakdown Voltage	V_{DS} = 0, I_G = −1 μA		−40			−40			−40			V
I_{DSS}	Saturation Drain Current	V_{DS} = 20V, V_{GS} = 0, (Note 2)		0.5		6.0	0.5		6.0	0.5		6.0	mA
I_G	Gate Current, (Note 1)	V_{DG} = 20V, I_D = 200 μA				−100			−100			−100	pA
V_{GS}	Gate-Source Voltage			−0.3		−4.0	−0.3		−4.0	−0.3		−4.0	V
g_{fs}	Common-Source Forward Transconductance	V_{DS} = 20V, V_{GS} = 0	f = 1kHz	1000		4000	1000		4000	1000		4000	μmho
		V_{DG} = 20V, I_D = 200 μA		700		1200	700		1200	700		1200	
g_{os}	Common-Source Output Conductance	V_{DS} = 20V, V_{GS} = 0				20			20			20	
		V_{DS} = 20V, I_D = 200 μA				5			5			5	
C_{iss}	Common-Source Input Capacitance	V_{DS} = 20V, V_{GS} = 0	f = 1 MHz		4.5			4.5			4.5		pF
C_{rss}	Common-Source Reverse Transfer Capacitance				1.2			1.2			1.2		
e_n	Equivalent Short-Circuit Input Noise Voltage	V_{DS} = 20V, I_D = 200 μA	f = 100 Hz		15			15			15		$\frac{nV}{\sqrt{Hz}}$
$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage	V_{DG} = 20V, I_D = 200 μA				5			10			15	mV
$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Differential Drift	V_{DG} = 20V, I_D = 200 μA, T_A = 25°C to T_B = 85°C				10			15			25	μV/°C
CMRR	Common-Mode Rejection Ratio	V_{DD} = 10V to V_{DD} = 20V, I_D = 200 μA, (Note 3)		70	80			80			80		dB

Note 1: Approximately doubles for every 10°C increase in T_A.
Note 2: Pulse test duration = 300 μs; duty cycle ≤ 3%.
Note 3: CMRR = 20 $\log_{10}$ [$\Delta V_{DD}/\Delta\lvert V_{GS1}-V_{GS2}\rvert$], ΔV_{DD} = 10V.

4

U308-10 N-Channel JFETs

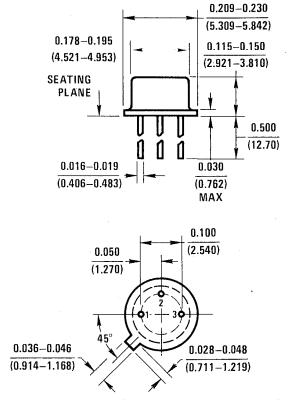
General Description

The U308 thru U310 series of N-channel JFETs is designed for VHF amplifier, oscillator and mixer applications.

Absolute Maximum Ratings (25°C)

Gate-Drain or Gate-Source Voltage	−25V
Gate Current	20 mA
Total Power Dissipation	500 mW
Power Derating	4 mW/°C
Storage Temperature Range	−65°C to +200°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-52



PIN	FET
1	S
2	D
3	G

Electrical Characteristics (25°C unless otherwise noted)

PARAMETER		CONDITIONS		U308			U309			U310			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
I_{GSS}	Gate Reverse Current	V_{GS} = −15V				−150			−150			−150	pA
		V_{GS} = 0	T = 125°C			−150			−150			−150	nA
BV_{GSS}	Gate-Source Breakdown Voltage	I_G = −1 μA, V_{DS} = 0		−25			−25			−25			V
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 10V, I_D = 1 nA		−1.0		−6.0	−1.0		−4.0	−2.5		−6.0	
I_{DSS}	Saturation Drain Current	V_{DS} = 10V, V_{GS} = 0, (Note 1)		12		60	12		30	24		60	mA
$V_{GS(f)}$	Gate-Source Forward Voltage	I_G = 10 mA, V_{DS} = 0				1.0			1.0			1.0	V
g_{fg}	Common-Gate Forward Transconductance, (Note 1)	V_{DS} = 10V, I_D = 10 mA	f = 1 kHz	10		20	10		20	10		18	mmho
g_{ogs}	Common-Gate Output Conductance					150			150			150	μmho
C_{gd}	Drain-Gate Capacitance	V_{DS} = 10V, V_{GS} = −10V	f = 1 MHz			2.5			2.5			2.5	pF
C_{gs}	Gate-Source Capacitance					5.0			5.0			5.0	
e_n	Equivalent Short-Circuit Input Noise Voltage	V_{DS} = 10V, I_D = 10 mA	f = 100 Hz		10			10			10		$\frac{nV}{\sqrt{Hz}}$
g_{fg}	Common-Gate Forward Transconductance	V_{DS} = 10V, I_D = 10 mA	f = 100 MHz		12			12			12		mmho
			f = 450 MHz		11			11			11		
g_{ogs}	Common-Gate Output Conductance		f = 100 MHz		0.18			0.18			0.18		
			f = 450 MHz		0.7			0.7			0.7		
G_{pg}	Common-Gate Power Gain		f = 100 MHz		15			15			15		dB
			f = 450 MHz		10			10			10		
NF	Noise Figure		f = 100 MHz		1.5			1.5			1.5		
			f = 450 MHz		3.2			3.2			3.2		

Note 1: Pulse test duration = 2 ms.

Section 5

Analog Switches

5

R_{ON} (Ω)	V_A/I (V)	PART NUMBER	LOGIC INPUT	V_S (V) TYP	t_{ON}/t_{OFF} TYP
Dual SPST					
10	±10	AH0141/DG141	TTL	−18, 12	0.8/1.1μs
30	±10	AH0133/DG133	TTL	−18, 12	0.5/0.9μs
80	±10	AH0134/DG134	TTL	−18, 12	0.5/0.9μs
15	±7.5	AH0151/DG151	TTL	±15	0.8/1.1μs
50	±7.5	AH0152/DG152	TTL	±15	0.5/0.9μs
*30	±7.5	AM181/DG181	TTL	±15, 5	180/150 ns
*75	±10	AM182/DG182	TTL	±15, 5	300/150 ns
Triple SPST					
*100	15 mA	AH5015	15V TTL		150/300 ns
*150	5 mA	AH5016	TTL		150/300 ns
200-600	±10V	MM455/MM555	PMOS		
Quad SPST					
200-600	±10	AH0015	TTL	−20, 10, 5	100/400 ns
*200	±10	LF11201	TTL	±15	90/500 ns
*200	±10	LF11202	TTL	±15	90/500 ns
*200	±10	LF11331	TTL	±15	90/500 ns
*200	±10	LF11332	TTL	±15	90/500 ns
*200	±10	LF11333	TTL	±15	90/500 ns
*250	±10	LF13201	TTL	±15	90/500 ns
*250	±10	LF13202	TTL	±15	90/500 ns
*250	±10	LF13331	TTL	±15	90/500 ns
*250	±10	LF13332	TTL	±15	90/500 ns
*250	±10	LF13333	TTL	±15	90/500 ns
280	±7.5	CD4066	CMOS	±7.5	
850	±7.5	CD4016	CMOS	±7.5	
*100	15 mA	AH5011/AM9711	15V TTL		150/300 ns
*100	10 mA	AM97C11	CMOS		150/300 ns
*150	5 mA	AH5012/AM9712	TTL		150/300 ns
*150	3 mA	AM97C12	CMOS		150/300 ns
*30	±7.5	AM193	TTL	±15, 5	180/150 ns
*75	±10	AM194	TTL	±15, 5	300/150 ns
200-600	±10	MM452/MM552	PMOS		150/300 ns

R_{ON} (Ω)	V_A/I (V)	PART NUMBER	LOGIC INPUT	V_S (V) TYP	t_{ON}/t_{OFF} TYP
SPDT					
10	±10	AH0146/DG146	TTL	−18, 12	0.8/1.1μs
30	±10	AH0144/DG144	TTL	−18, 12	0.5/0.9μs
80	±10	AH0143/DG143	TTL	−18, 12	0.5/0.9μs
15	±7.5	AH0161/DG161	TTL	±15	0.8/1.1μs
50	±7.5	AH0162/DG162	TTL	±15	0.5/0.9μs
100	±9	AH2114 (Sw. 1)	15V TTL	±15	35/600 ns
		(Sw. 2)			1.2μs/50 ns
*30	±7.5	AM187/DG187	TTL	±15, 5	180/150 ns
*75	±10	AM188/DG188	TTL	±15, 5	300/150 ns
Dual SPDT					
*30	±7.5	AM190/DG190	TTL	±15, 5	180/150 ns
*75	±10	AM191/DG191	TTL	±15, 5	300/150 ns
Triple SPDT					
280	±7.5	CD4053	CMOS	±7.5	
Dual DPST					
10	±10	AH0140/DG140	TTL	−18, 12	0.8/1.1μs
30	±10	AH0129/DG129	TTL	−18, 12	0.5/0.9μs
80	±10	AH0126/DG126	TTL	−18, 12	0.5/0.9μs
15	±7.5	AH0153/DG153	TTL	±15	0.8/1.1μs
50	±7.5	AH0154/DG154	TTL	±15	0.5/0.9μs
200-600	±10	AH0019	TTL	−20, 10, 5	100/400 ns
*30	±7.5	AM184/DG184	TTL	±15.5	180/150 ns
*75	±10	AM185/DG185	TTL	±15.5	300/150 ns
DPDT					
10	±10	AH0145/DG145	TTL	−18, 12	0.8/1.1μs
30	±10	AH0139/DG139	TTL	−18, 12	0.5/0.9μs
80	±10	AH0142/DG142	TTL	−18, 12	0.5/0.9μs
15	±7.5	AH0163/DG163	TTL	±15	0.8/1.1μs
50	±7.5	AH0164/DG164	TTL	±15	0.5/0.9μs
200-600	±10	AH0014	TTL	−20, 10, 5	350/400 ns

R_{ON} (Ω)	V_A/I (V)	PART NUMBER	LOGIC INPUT	V_S (V) TYP	t_{ON}/t_{OFF} TYP
MULTIPLEXERS					
2-Channel Differential					
200-600	±10	MM450/MM550	PMOS		
3-Channel					
*100	15 mA	AH5013	15V TTL		150/300 ns
*150	5 mA	AH5014	TTL		150/300 ns
4-Channel					
*100	15 mA	AH5009/AM9709	15V TTL		150/300 ns
*100	10 mA	AM97C09	CMOS		150/300 ns
*150	5 mA	AH5010/AM9710	TTL		150/300 ns
*150	3 mA	AM97C10	CMOS		150/300 ns
200-600	±10	MM451/MM551	PMOS		
4-Channel Differential					
280	±7.5	CD4052	CMOS	±7.5	
200-600	±10	MM454/MM554	PMOS	−24, 12	
*350	12,−15	LF11509	TTL	±15	1/0.2μs
6-Channel					
250-1500	50 mA	AM2009/MM4504/ MM5504	TTL		
8-Channel					
250-400	±5	AM3705	TTL	−15, 5	
*350	12,−15	LF11508	TTL	±15	1/0.2μs
8-Channel Differential					
*350	12,−15	LF11507	TTL	±15	1/0.2μs
16-Channel					
*350	12,−15	LF11506	TTL	±15	1/0.2μs

Notes:

R_{ON} max @ T_A = 25°C

V_A/I = maximum voltage or current to be safely switched

Part number = basic number/alternate number (i.e., AM181/DG181). May be ordered by either number.

*Preferred devices

Definition of Terms

Driver Leakage Current: The sum of the currents into the source and drain switch terminals, with both held at the same specified voltage.

Logic "1" Input Voltage: The voltage level which is guaranteed to be interpreted by the device as a logical "true" signal.

Logic "0" Input Voltage: The voltage level which is guaranteed to be interpreted by the device as a logical "false" signal.

Logic Input Slew Rate: The voltage difference between the logic "1" and logic "0" states divided by the transition time.

Switch Leakage Current: The current seen when a specified voltage is applied between drain and source of a channel that is logically turned off.

Switch "ON" Resistance: The equivalent resistance from source to drain, tested by forcing a specified current and measuring the resultant voltage drop.

Switch Turn "OFF" Time: The interval between the time that the logic input passes through the threshold voltage and the time that the output goes to a specified voltage level in the test circuit.

Switch Turn "ON" Time: The interval between the time that the logic input passes through the threshold voltage and the time that the output goes to 90% of its final value in the specified test circuit.

AH0014/AH0014C* DPDT, AH0015/AH0015C Quad SPST, AH0019/AH0019C* Dual DPST-TTL/DTL Compatible MOS Analog Switches

General Description

This series of TTL/DTL compatible MOS analog switches feature high speed with internal level shifting and driving. The package contains two monolithic integrated circuit chips: the MOS analog chip is similar to the MM450 type which consists of four MOS analog switch transistors; the second chip is a bipolar I.C. gate and level shifter. The series is available in both hermetic dual-in-line package and flatpack.

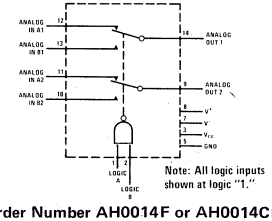
Features

- Large analog voltage switching ±10V
- Fast switching speed 500 ns
- Operation over wide range of power supplies
- Low ON resistance 200Ω
- High OFF resistance $10^{11}\Omega$
- Fully compatible with DTL or TTL logic
- Includes gating and level shifting

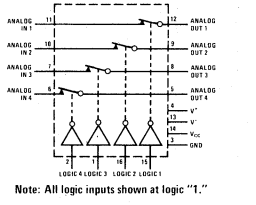
These switches are particularly suited for use in both military and industrial applications such as commutators in data acquisition systems, multiplexers, A/D and D/A converters, long time constant integrators, sample and hold circuits, modulators/demodulators, and other analog signal switching applications. For information on other National analog switches and analog interface elements, see listing on last page.

The AH0014, AH0015 and AH0019 are specified for operation over the −55°C to +125°C military temperature range. The AH0014C, AH0015C and AH0019C are specified for operation over the −25°C to +85°C temperature range.

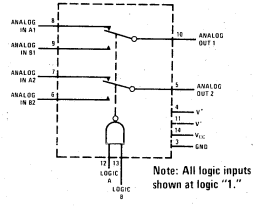
Block and Connection Diagrams



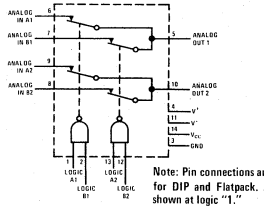
Order Number AH0014F or AH0014CF
See Package 23
Quad SPST



Order Number AH0015D or AH0015CD
See Package 15



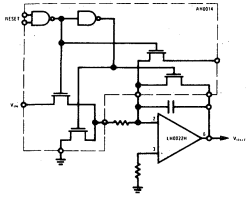
Order Number AH0014D or AH0014CD
See Package 14
Dual DPST



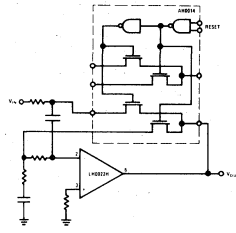
Order Number AH0019F or AH0019CF
See Package 23
Order Number AH0019D or AH0019CD
See Package 14

Typical Applications

Integrator



Reset Stabilized Amplifier



*Previously called NH0014/NH0014C and NH0019/NH0019C

Absolute Maximum Ratings

V_{CC} Supply Voltage	7.0V
V^- Supply Voltage	−30V
V^+ Supply Voltage	+30V
V^+/V^- Voltage Differential	40V
Logic Input Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
AH0014, AH0015, AH0019	−55°C to +125°C
AH0014C, AH0015C, AH0019C	−25°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C

Electrical Characteristics (Notes 1 and 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = 4.5V	2.0			V
Logical "0" Input Voltage	V_{CC} = 4.5V			0.8	V
Logical "1" Input Current	V_{CC} = 5.5V V_{IN} = 2.4V			5	μA
Logical "1" Input Current	V_{CC} = 5.5V V_{IN} = 5.5V			1	mA
Logical "0" Input Current	V_{CC} = 5.5V V_{IN} = 0.4V		0.2	0.4	mA
Power Supply Current Logical "1" Input – each gate (Note 3)	V_{CC} = 5.5V V_{IN} = 4.5V		0.85	1.6	mA
Power Supply Current Logical "0" Input – each gate (Note 3)	V_{CC} = 5.5V V_{IN} = 0V				
AH0014, AH0014C			1.5	3.0	mA
AH0015, AH0015C			0.22	0.41	mA
AH0019, AH0019C			0.22	0.41	mA
Analog Switch ON Resistance – each gate	V_{IN} (Analog) = +10V		75	200	Ω
	V_{IN} (Analog) = −10V		150	600	Ω
Analog Switch OFF Resistance			10^{11}		Ω
Analog Switch Input Leakage Current – each input (Note 4)	V_{IN} = −10V				
AH0014, AH0015, AH0019	T_A = 25°C		25	200	pA
	T_A = 125°C		25	200	nA
AH0014C, AH0015C, AH0019C	T_A = 25°C		0.1	10	nA
	T_A = 70°C		30	100	nA
Analog Switch Output Leakage Current – each output (Note 4)	V_{OUT} = −10V				
AH0014, AH0015, AH0019	T_A = 25°C		40	400	pA
	T_A = 125°C		40	400	nA
AH0014C, AH0015C, AH0019C	T_A = 25°C		0.05	10	nA
	T_A = 70°C		4	50	nA
Analog Input (Drain) Capacitance	1 MHz @ Zero Bias		8	10	pF
Output Source Capacitance	1 MHz @ Zero Bias		11	13	pF
Analog Turn-OFF Time – t_{OFF}	See test circuit; T_A = 25°C		400	500	ns
Analog Turn-ON Time – t_{ON}	See test circuit; T_A = 25°C				
AH0014, AH0014C			350	425	ns
AH0015, AH0015C			100	150	ns
AH0019, AH0019C			100	150	ns

Note 1: Min/max limits apply across the guaranteed temperature range of −55°C to +125°C for AH0014, AH0015, AH0019 and −25°C to +85°C for AH0014C, AH0015C, AH0019C. V^- = −20V. V^+ = +10V and an analog test current of 1 mA unless otherwise specified.

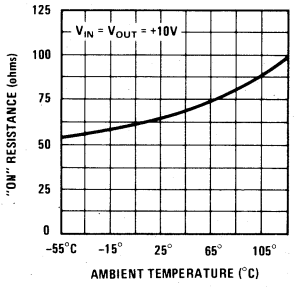
Note 2: All typical values are measured at T_A = 25°C with V_{CC} = 5.0V. V^+ = +10V, V^- = −22V.

Note 3: Current measured is drawn from V_{CC} supply.

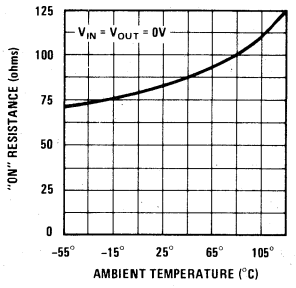
Note 4: All analog switch pins except measurement pin are tied to V^+.

Analog Switch Characteristics (Note 2)

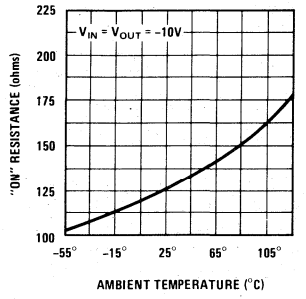
R_{ON} vs Temperature



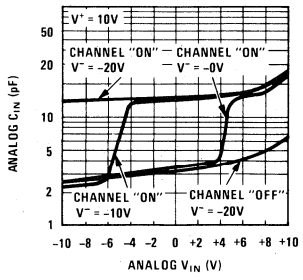
R_{ON} vs Temperature



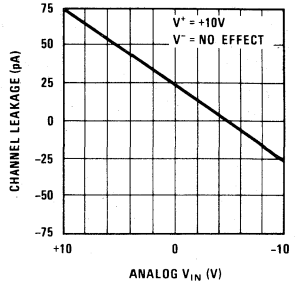
R_{ON} vs Temperature



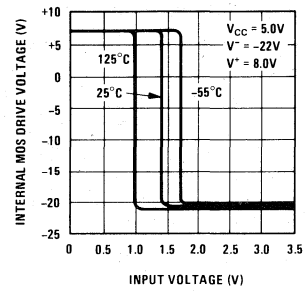
C_{IN} vs V_{IN}



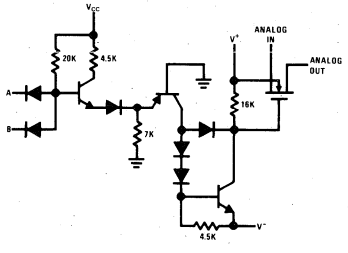
Leakage vs V_{IN} (Channel "OFF")



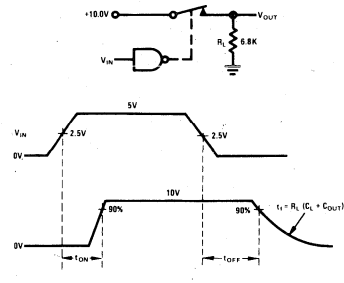
Driver Gate V_{IN} vs V_{OUT}



Schematic (Single Driver Gate and MOS Switch Shown)

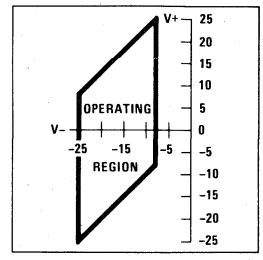


Analog Switching Time Test Circuit



Selecting Power Supply Voltage

The graph shows the boundary conditions which must be used for proper operation of the unit. The range of operation for power supply V^- is shown on the X axis. It must be between −25V and −8V. The allowable range for power supply V^+ is governed by supply V^-. With a value chosen for V^-, V^+ may be selected as any value along a vertical line passing through the V^- value and terminated by the boundaries of the operating region. A voltage difference between power supplies of at least 5V should be maintained for adequate signal swing.



AH0120, AH0130, AH0140, AH0150, AH0160 Series Analog Switches

General Description

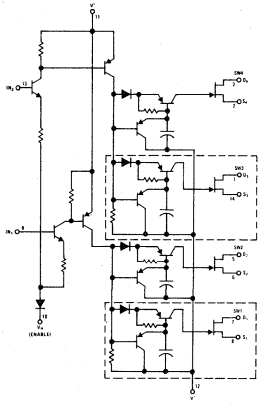
The AH0100 series represents a complete family of junction FET analog switches. The inherent flexibility of the family allows the designer to tailor the device selection to the particular application. Switch configurations available include dual DPST, dual SPST, DPDT, and SPDT. $r_{ds(ON)}$ ranges from 10 ohms through 100 ohms. The series is available in both 14 lead flat pack and 14 lead cavity DIP. Important design features include:

- TTL/DTL and RTL compatible logic inputs
- Up to 20V p-p analog input signal
- $r_{ds(ON)}$ less than 10Ω (AH0140, AH0141, AH0145, AH0146)
- Analog signals in excess of 1 MHz
- "OFF" power less than 1 mW
- Gate to drain bleed resistors eliminated
- Fast switching, t_{ON} is typically .4 μs, t_{OFF} is 1.0 μs
- Operation from standard op amp supply voltages, ±15V, available (AH0150/AH0160 series)
- Pin compatible with the popular DG 100 series.

The AH0100 series is designed to fulfill a wide variety of analog switching applications including commutators, multiplexers, D/A converters, sample and hold circuits, and modulators/demodulators. The AH0100 series is guaranteed over the temperature range −55°C to +125°C; whereas, the AH0100C series is guaranteed over the temperature range −25°C to +85°C.

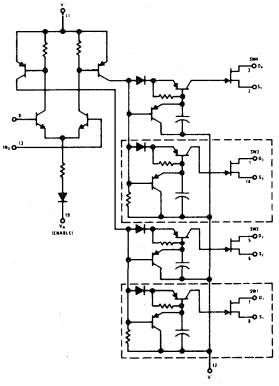
Schematic Diagrams

DUAL DPST and DUAL SPST



Note: Dotted line portions are not applicable to the dual SPST.

DPDT (diff.) and SPDT (diff.)

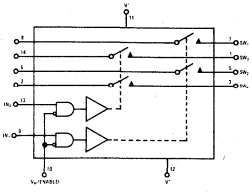


Note: Dotted line portions are not applicable to the SPDT (differential).

Logic and Connection Diagrams

Order any of the devices below using the part number with a D or F suffix. See Packages 14 and 23

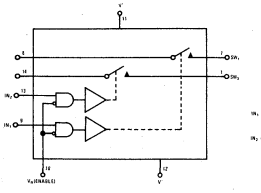
DUAL DPST



HIGH LEVEL (±10V)
AH0140 (10Ω)
AH0129 (30Ω)
AH0126 (80Ω)

MEDIUM LEVEL (±7.5V)
AH0153 (15Ω)
AH0154 (50Ω)

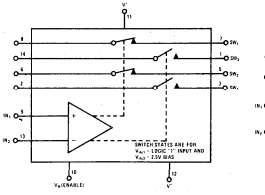
DUAL SPST



HIGH LEVEL (±10V)
AH0141 (10Ω)
AH0133 (30Ω)
AH0134 (80Ω)

MEDIUM LEVEL (±7.5V)
AH0151 (15Ω)
AH0152 (50Ω)

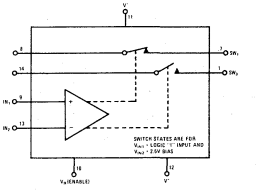
DUAL DPDT (Diff)



HIGH LEVEL (±10V)
AH0145 (10Ω)
AH0139 (30Ω)
AH0142 (80Ω)

MEDIUM LEVEL (±7.5)
AH0163 (15Ω)
AH0164 (50Ω)

SPDT (Diff)



HIGH LEVEL (±10V)
AH0146 (10Ω)
AH0144 (30Ω)
AH0143 (80Ω)

MEDIUM LEVEL (±7.5V)
AH0161 (15Ω)
AH0162 (50Ω)

Absolute Maximum Ratings

		High Level	Medium Level
Total Supply Voltage ($V^+ - V^-$)		36V	34V
Analog Signal Voltage ($V^+ - V_A$ or $V_A - V^-$)		30V	25V
Positive Supply Voltage to Reference ($V^+ - V_R$)		25V	25V
Negative Supply Voltage to Reference ($V_R - V^-$)		22V	22V
Positive Supply Voltage to Input ($V^+ - V_{IN}$)		25V	25V
Input Voltage to Reference ($V_{IN} - V_R$)		±6V	±6V
Differential Input Voltage ($V_{IN} - V_{IN2}$)		±6V	±6V
Input Current, Any Terminal		30 mA	30 mA
Power Dissipation			See Curve
Operating Temperature Range	AH0100 Series	−55°C to +125°C	
	AH0100C Series	−25°C to +85°C	
Storage Temperature Range		−65°C to +150°C	
Lead Temperature (Soldering, 10 sec)		300°C	

Electrical Characteristics for "HIGH LEVEL" Switches (Note 1)

PARAMETER	SYMBOL	DEVICE TYPE				CONDITIONS		LIMITS		UNITS
		DUAL DPST	DUAL SPST	DPDT (DIFF)	SPDT (DIFF)	$V^+ = 12.0V$, $V^- = -18.0V$, $V_R = 0.0V$		TYP	MAX	
Logic "1" Input Current	$I_{IN(ON)}$	All Circuits				Note 2	$T_A = 25°C$	2.0	60	µA
							Over Temp. Range		120	µA
Logic "0" Input Current	$I_{IN(OFF)}$	All Circuits				Note 2	$T_A = 25°C$	.01	.1	µA
							Over Temp. Range		2.0	µA
Positive Supply Current Switch ON	$I^+_{(ON)}$	All Circuits				One Driver ON Note 2	$T_A = 25°C$	2.2	3.0	mA
							Over Temp. Range		3.3	mA
Negative Supply Current Switch ON	$I^-_{(ON)}$	All Circuits				One Driver ON Note 2	$T_A = 25°C$	-1.0	-1.8	mA
							Over Temp. Range		-2.0	mA
Reference Input (Enable) ON Current	$I_{R(ON)}$	All Circuits				One Driver ON Note 2	$T_A = 25°C$	-1.0	-1.4	mA
							Over Temp. Range		-1.6	mA
Positive Supply Current Switch OFF	$I^+_{(OFF)}$	All Circuits				$V_{IN1} = V_{IN2} = 0.8V$	$T_A = 25°C$	1.0	10	µA
							Over Temp. Range		25	µA
Negative Supply Current Switch OFF	$I^-_{(OFF)}$	All Circuits				$V_{IN1} = V_{IN2} = 0.8V$	$T_A = 25°C$	-1.0	-10	µA
							Over Temp. Range		-25	µA
Reference Input (Enable) OFF Current	$I_{R(OFF)}$	All Circuits				$V_{IN1} = V_{IN2} = 0.8V$	$T_A = 25°C$	-1.0	-10	µA
							Over Temp. Range		-25	µA
Switch ON Resistance	$r_{ds(ON)}$	AH0126	AH0134	AH0142	AH0143	$V_D = 10V$, $I_D = 1$ mA	$T_A = 25°C$	45	80	Ω
							Over Temp. Range		150	Ω
Switch ON Resistance	$r_{ds(ON)}$	AH0129	AH0133	AH0139	AH0144	$V_D = 10V$, $I_D = 1$ mA	$T_A = 25°C$	25	30	Ω
							Over Temp. Range		60	Ω
Switch ON Resistance	$r_{ds(ON)}$	AH0140	AH0141	AH0145	AH0146	$V_D = 10V$, $I_F = 1$ mA	$T_A = 25°C$	8	10	Ω
							Over Temp. Range		20	Ω
Driver Leakage Current	$(I_D + I_S)_{ON}$	All Circuits				$V_D = V_S = -10V$	$T_A = 25°C$	.01	1	nA
							Over Temp. Range		100	nA
Switch Leakage Current	$I_{S(OFF)}$ OR $I_{D(OFF)}$	AH0126 AH0129	AH0134 AH0133	AH0142 AH0139	AH0143 AH0144	$V_{DS} = ±20V$	$T_A = 25°C$	0.8	1	nA
							Over Temp. Range		100	nA
Switch Leakage Current	$I_{S(OFF)}$ OR $I_{D(OFF)}$	AH0140	AH0141	AH0145	AH0146	$V_{DS} = ±20V$	$T_A = 25°C$	4	10	nA
							Over Temp. Range		1.0	µA
Switch Turn-ON Time	t_{ON}	AH0126 AH0129	AH0134 AH0133	AH0142 AH0139	AH0143 AH0144	See Test Circuit $V_A = ±10V$ $T_A = 25°C$		0.5	0.8	µs
Switch Turn-ON Time	t_{ON}	AH0140	AH0141	AH0145	AH0146	See Test Circuit $V_A = ±10V$ $T_A = 25°C$		0.8	1.0	µs
Switch Turn-OFF Time	t_{OFF}	AH0126 AH0129	AH0134 AH0133	AH0142 AH0139	AH0143 AH0144	See Test Circuit $V_A = ±10V$ $T_A = 25°C$		0.9	1.6	µs
Switch Turn-OFF Time	t_{OFF}	AH0140	AH0141	AH0145	AH0146	See Test Circuit $V_A = ±10V$ $T_A = 25°C$		1.1	2.5	µs

Note 1: Unless otherwise specified these limits apply for −55°C to +125°C for the AH0100 series and −25°C to +85°C for the AH0100C series. All typical values are for $T_A = 25°C$.

Note 2: For the DPST and Dual DPST, the ON condition is for $V_{IN} = 2.5V$; the OFF condition is for $V_{IN} = 0.8V$. For the differential switches and SW1 and 2 ON, $V_{IN2} = 2.5V$, $V_{IN1} = 3.0V$. For SW3 and 4 ON, $V_{IN2} = 2.5V$, $V_{IN1} = 2.0V$.

Electrical Characteristics for "MEDIUM LEVEL" Switches (Note 1)

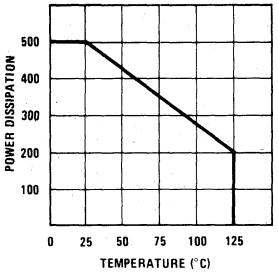
PARAMETER	SYMBOL	DEVICE TYPE				CONDITIONS		LIMITS		UNITS
		DUAL DPST	DUAL SPST	DUAL DPDT	SPDT (DIFF)	$V^+ = +15.0V$, $V^- = -15V$, $V_R = 0V$		TYP	MAX	
Logic "1" Input Current	$I_{IN(ON)}$	All Circuits				Note 2	$T_A = 25°C$	20	60	μA
							Over Temp. Range		120	μA
Logic "0" Input Current	$I_{IN(OFF)}$	All Circuits				Note 2	$T_A = 25°C$	.01	0.1	μA
							Over Temp. Range		2	μA
Positive Supply Current Switch ON	$I^+_{(ON)}$	All Circuits				One Driver ON Note 2	$T_A = 25°C$	2.2	3.0	mA
							Over Temp. Range		3.3	mA
Negative Supply Current Switch ON	$I^-_{(ON)}$	All Circuits				One Driver ON Note 2	$T_A = 25°C$	-1.0	-1.8	mA
							Over Temp. Range		-2.0	mA
Reference Input (Enable) ON Current	$I_{R(ON)}$	All Circuits				One Driver ON Note 2	$T_A = 25°C$	-1.0	-1.4	mA
							Over Temp. Range		-1.6	mA
Positive Supply Current Switch OFF	$I^+_{(OFF)}$	All Circuits				$V_{IN1} = V_{IN2} = 0.8V$	$T_A = 25°C$	1.0	10	μA
							Over Temp. Range		25	μA
Negative Supply Current Switch OFF	$I^-_{(OFF)}$	All Circuits				$V_{IN1} = V_{IN2} = 0.8V$	$T_A = 25°C$	-1.0	-10	μA
							Over Temp. Range		-25	μA
Reference Input (Enable) OFF Current	$I_{R(OFF)}$	All Circuits				$V_{IN1} = V_{IN2} = 0.8V$	$T_A = 25°C$	-1.0	-10	μA
							Over Temp. Range		-25	μA
Switch ON Resistance	$r_{ds(ON)}$	AH0153	AH0151	AH0163	AH0161	$V_D = 7.5V$ $I_D = 1$ mA	$T_A = 25°C$	10	15	Ω
							Over Temp. Range		30	Ω
Switch ON Resistance	$r_{ds(ON)}$	AH0154	AH0152	AH0164	AH0162	$V_D = 7.5V$ $I_D = 1$ mA	$T_A = 25°C$	45	50	Ω
							Over Temp. Range		100	Ω
Driver Leakage Current	$(I_D + I_S)_{ON}$	All Circuits				$V_D = V_S = -7.5V$	$T_A = 25°C$	.01	2	nA
							Over Temp. Range		500	nA
Switch Leakage Current	$I_{D(OFF)}$ OR $I_{S(OFF)}$	AH0153	AH0151	AH0163	AH0161	$V_{DS} = \pm 15V$	$T_A = 25°C$	5	10	nA
							Over Temp. Range		1.0	μA
Switch Leakage Current	$I_{D(OFF)}$ OR $I_{S(OFF)}$	AH0154	AH0152	AH0164	AH0162	$V_{DS} = \pm 15.0V$	$T_A = 25°C$	1.0	2.0	nA
							Over Temp. Range		200	nA
Switch Turn-ON Time	t_{ON}	AH0153	AH0151	AH0163	AH0161	See Test Circuit $V_A = \pm 7.5V$ $T_A = 25°C$		0.8	1.0	μs
Switch Turn-ON Time	t_{ON}	AH0154	AH0152	AH0164	AH0162	See Test Circuit $V_A = \pm 7.5V$ $T_A = 25°C$		0.5	0.8	μs
Switch Turn-OFF Time	t_{OFF}	AH0153	AH0151	AH0163	AH0161	See Test Circuit $V_A = \pm 7.5V$ $T_A = 25°C$		1.1	2.5	μs
Switch Turn-OFF Time	t_{OFF}	AH0154	AH0152	AH0164	AH0162	See Test Circuit $V_A = \pm 7.5V$ $T_A = 25°C$		0.9	1.5	μs

Note 1: Unless otherwise specified, these limits apply for −55°C to +125°C for the AH0100 series and −25°C to +85°C for the AH0100C series. All typical values are for $T_A = 25°C$.

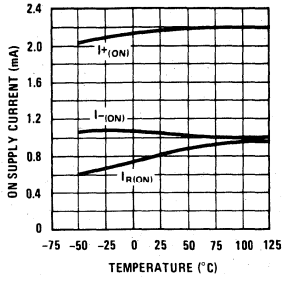
Note 2: For the DPST and Dual DPST, the ON condition is for $V_{IN} = 2.5V$; the OFF condition is for $V_{IN} = 0.8V$. For the differential switches and SW1 and 2 ON, $V_{IN2} = 2.5V$, $V_{IN1} = 3.0V$. For SW3 and 4 ON, $V_{IN2} = 2.5V$, $V_{IN1} = 2.0V$.

Typical Performance Characteristics

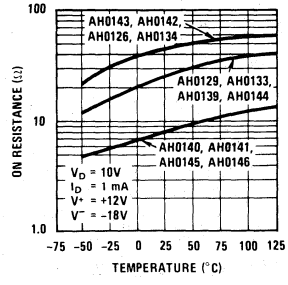
Power Dissipation vs Temperature



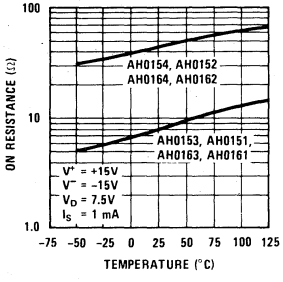
ON Supply Current vs Temperature



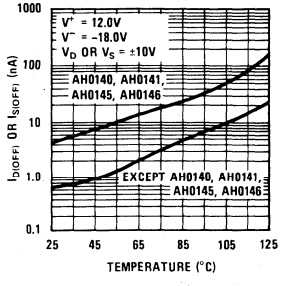
rds(ON) vs Temperature AH0120 thru AH0140 Series



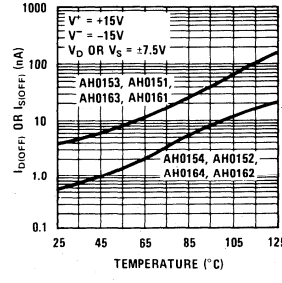
rds(ON) vs Temperature AH0150/AH0160 Series



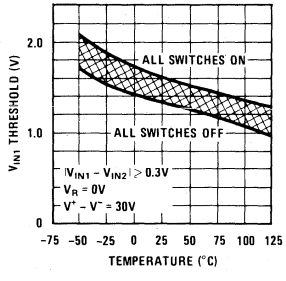
Leakage Current vs Temperature AH0120, AH0130, & AH0140



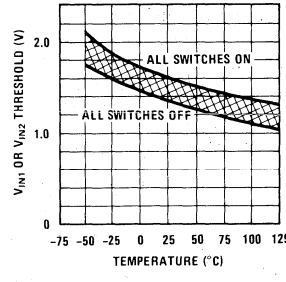
Leakage Current vs Temperature AH0150 & AH0160



Single Ended Switch Input Threshold vs Temperature

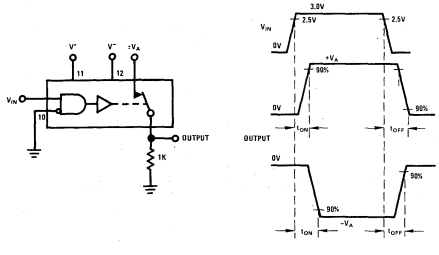


Differential Switch Input Threshold vs Temperature

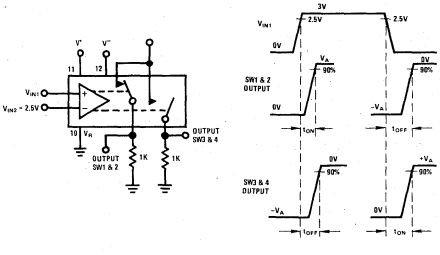


Switching Time Test Circuits

Single Ended Input



Differential Input



Applications Information

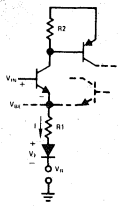
1. INPUT LOGIC COMPATIBILITY

A. Voltage Considerations

In general, the AH0100 series is compatible with most DTL, TTL, and RTL logic families. The ON-input threshold is determined by the V_{BE} of the input transistor plus the V_f of the diode in the emitter leg, plus I x R_1, plus V_R. At room temperature and V_R = 0V, the nominal ON threshold is: 0.7V+0.7V+0.2V, = 1.6V. Over temperature and manufacturing tolerances, the threshold may be as high as 2.5V and as low as 0.8V. The rules for proper operation are:

$V_{IN} - V_R \geq 2.5V$ All switches ON

$V_{IN} - V_R \leq 0.8V$ All switches OFF



B. Input Current Considerations

$I_{IN(ON)}$, the current drawn by the driver with V_{IN} = 2.5V is typically 20 μA at 25°C and is guaranteed less than 120 μA over temperature. DTL, such as the DM930 series can supply 180 μA at logic "1" voltages in excess of 2.5V. TTL output levels are comparable at 400 μA. The DTL and TTL can drive the AH0100 series directly. However, at low temperature, DC noise margin in the logic "1" state is eroded with DTL. A pull-up resistor of 10 kΩ is recommended when using DTL over military temperature range.

If more than one driver is to be driven by a DM930 series (6K) gate, an external pull-up resistor should be added. The value is given by:

$$R_P = \frac{11}{N-1} \text{ for } N > 2$$

where:

R_P = value of the pull-up resistor in kΩ

N = number of drivers.

C. Input Slew Rate

The slew rate of the logic input must be in excess of 0.3V/μs in order to assure proper operation of the analog switch. DTL, TTL, and RTL output rise times are far in excess of the minimum slew rate requirements. Discrete logic designs, however, should include consideration of input rise time.

2. ENABLE CONTROL

The application of a positive signal at the V_R terminal will open all switches. The V_R (ENABLE) signal must be capable of rising to within 0.8V of $V_{IN(ON)}$ in the OFF state and of sinking $I_{R(ON)}$ milliamps in the ON state (at $V_{IN(ON)} - V_R >$ 2.5V). The V_R terminal can be driven from most TTL and DTL gates.

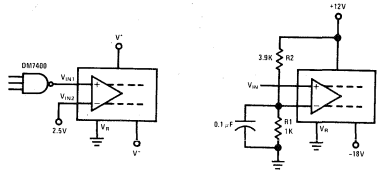
3. DIFFERENTIAL INPUT CONSIDERATIONS

The differential switch driver is essentially a differential amplifier. The input requirements for proper operation are:

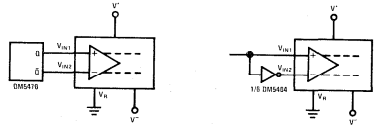
$$|V_{IN1} - V_{IN2}| \geq 0.3V$$

$$2.5 \leq (V_{IN1} \text{ or } V_{IN2}) - V_R \leq 5V$$

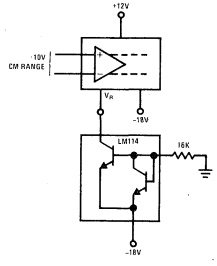
The differential driver may be furnished by a DC level as shown below. The level may be derived from a voltage divider to V^+ or the 5V V_{CC} of the DTL logic. In order to assure proper operation, the divider should be "stiff" with respect to I_{IN2}. Bypassing R1 with a 0.1 μF disc capacitor will prevent degradation of t_{ON} and t_{OFF}.



Alternatively, the differential driver may be driven from a TTL flip-flop or inverter.



Connection of a 1 mA current source between V_R and V^- will allow operation over a ±10V common mode range. Differential input voltage must be less than the 6V breakdown, and input threshold of 2.5V and 300mV differential overdrive still prevail.



4. ANALOG VOLTAGE CONSIDERATIONS

The rules for operating the AH0100 series at supply voltages other than those specified essentially breakdown into OFF and ON considerations. The OFF considerations are dictated by the maximum negative swing of the analog signal and the pinch off of the JFET switch. In the OFF state, the gate of the FET is at $V^- + V_{BE} + V_{SAT}$ or about 1.0V above the V^- potential. The maximum V_P of the FET switches is 7V. The most negative analog voltage, V_A, swing which can be accomodated for any given supply voltage is:

$$|V_A| \leq |V^-| - V_P - V_{BE} - V_{SAT} \text{ or}$$

$$|V_A| \leq |V^-| - 8.0 \text{ or } |V^-| \geq |V_A| + 8.0V$$

For the standard high level switches, $V_A \leq |-18| + 8 = -10V$. The value for V^+ is dictated by the maximum positive swing of the analog input voltage. Essentially the collector to base junction of the turn-on PNP must remain reversed biased for all positive value of analog input voltage. The base of the PNP is at $V^+ - V_{SAT} - V_{BE}$ or $V^+ - 1.0V$. The PNP's collector base junction should have at least 1.0V reverse bias. Hence, the most positive analog voltage swing which may be accommodated for a given value of V^+ is:

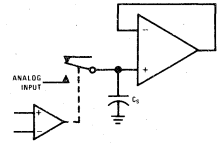
$$V_A \leq V^+ - V_{SAT} - V_{BE} - 1.0V \text{ or}$$

$$V_A \leq V^+ - 2.0V \text{ or } V^+ \geq V_A + 2.0V$$

For the standard high level switches, $V_A = 12 - 2.0V = +10V$.

5. SWITCHING TRANSIENTS

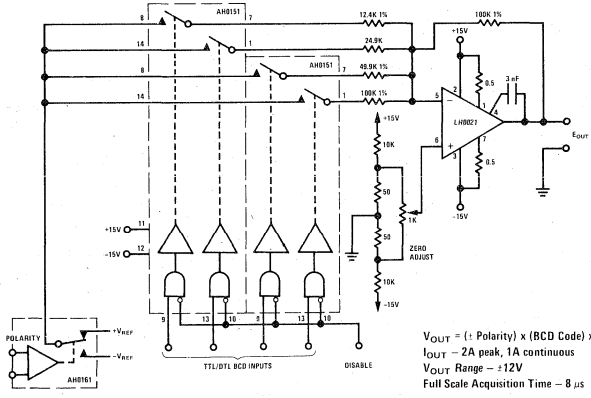
Due to charge stored in the gate-to-source and gate-to-drain capacitances of the FET switch, transients may appear in the output during switching. This is particularly true during the OFF to ON transition. The magnitude and duration of the transient may be minimized by making source and load impedance levels as small as practical.



Furthermore, transients may be minimized by operating the switches in the differential mode; i.e., the charge delivered to the load during the ON to OFF transition is, to a large extent, cancelled by the OFF to ON transition.

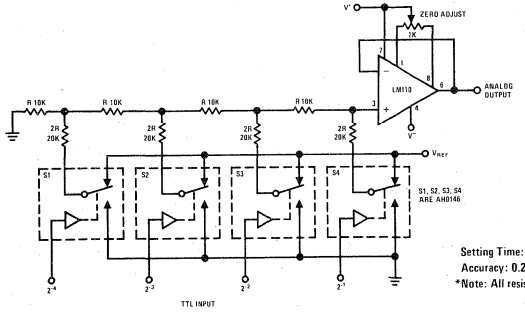
Typical Applications

Programmable One Amp Power Supply



V_{OUT} = (± Polarity) x (BCD Code) x V_{REF}
I_{OUT} – 2A peak, 1A continuous
V_{OUT} Range – ±12V
Full Scale Acquisition Time – 8 µs

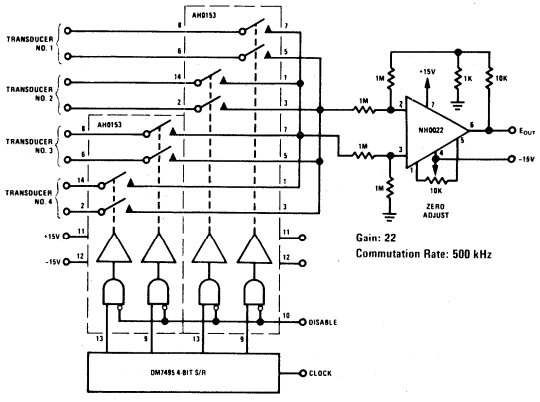
Four to Ten Bit D to A Converter (4 Bits Shown)



Setting Time: 1 µs
Accuracy: 0.2%
*Note: All resistors are 0.1%

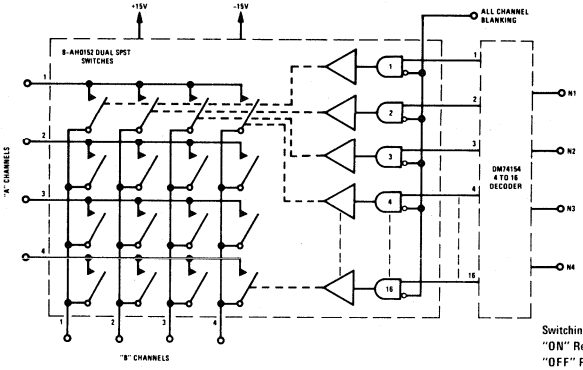
Typical Applications (Continued)

Four Channel Differential Transducer Commutator



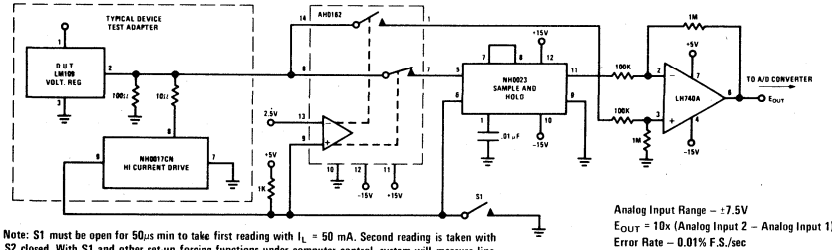
Gain: 22
Commutation Rate: 500 kHz

4 x 4 Cross Point Analog Switch



Switching Time – 800 ns
"ON" Resistance – 45Ω
"OFF" Resistance – 10^{10}Ω

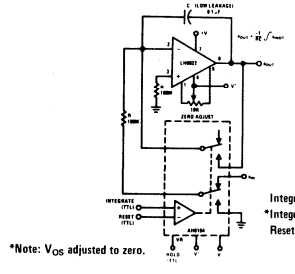
Delta Measurement System for Automatic Linear Circuit Tester



Analog Input Range – ±7.5V
E_{OUT} = 10x (Analog Input 2 – Analog Input 1)
Error Rate – 0.01% F.S./sec

Note: S1 must be open for 50μs min to take first reading with I_L = 50 mA. Second reading is taken with S2 closed. With S1 and other set-up forcing functions under computer control, system will measure line and load regulation on voltage regulators, voltage gain, offset current, CMRR and PSRR on op amps as well as other circuits requiring measurement of the change of a parameter with the change of a forcing function.

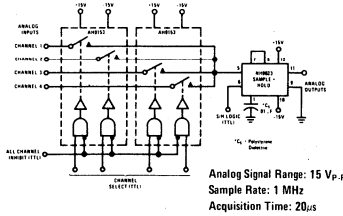
Precision Long Time Constant Integrator with Reset



Integration Internal = 10 sec
*Integration Error = 100μV
Reset Time: 30μs

*Note: V_{OS} adjusted to zero.

Four Channel Commutator



Analog Signal Range: 15 V_{P-P}
Sample Rate: 1 MHz
Acquisition Time: 20μs
Drift Rate: 0.5 mV/sec

AH2114/AH2114C DPST Analog Switch

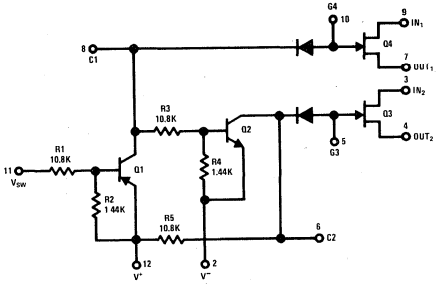
General Description

The AH2114 is a DPST analog switch circuit comprised of two junction FET switches and their associated driver. The AH2114 is designed to fulfill a wide variety of high level analog switching applications including multiplexers, A to D Converters, integrators, and choppers. Design features include:

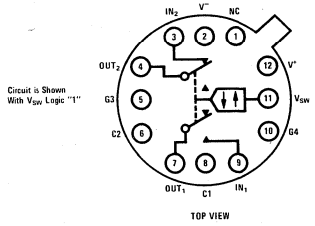
- Low ON resistance, typically 75Ω
- High OFF resistance, typically $10^{11}\Omega$
- Large output voltage swing, typically ±10V
- Powered from standard op-amp supply voltages of ±15V
- Input signals in excess of 1 MHz
- Turn-ON and turn-OFF times typically 1 μs

The AH2114 is guaranteed over the temperature range −55°C to +125°C whereas the AH2114C is guaranteed over the temperature range 0°C to +85°C.

Schematic and Connection Diagrams



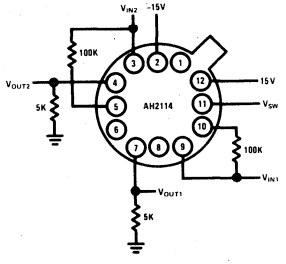
Metal Can Package

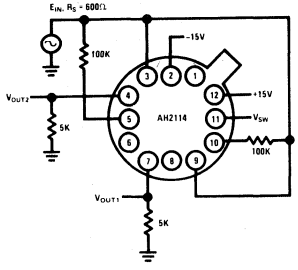


TOP VIEW

Order Number AH2114G or AH2114CG
See Package 3

AC Test Circuit and Waveforms





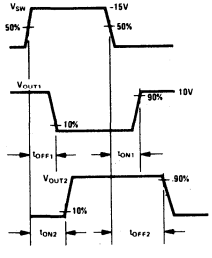


FIGURE 1.

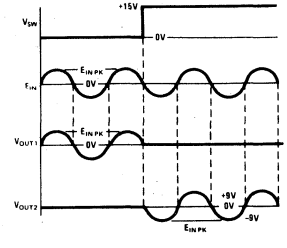


FIGURE 2.

Absolute Maximum Ratings

Vplus Supply Voltage	+25V
Vminus Supply Voltage	−25V
Vplus−Vminus Differential Voltage	40V
Logic Input Voltage	25V
Power Dissipation (Note 3)	1.36W
Operating Temperature Range	
AH2114	−55°C to +125°C
AH2114C	0°C to +85°C
Storage Temperature Range	−65°C to +125°C
Lead Temperature (Soldering, 10 sec)	300°C

Electrical Characteristics (Notes 1 and 2)

PARAMETER	CONDITIONS	AH2114			AH2114C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Static Drain-Source "On" Resistance	I_D = 1.0 mA, V_{GS} = 0V, T_A = 25°C		75	100		75	125	Ω
	I_D = 1.0 mA, V_{GS} = 0V			150			160	Ω
Drain-Gate Leakage Current	V_{DS} = 20V, V_{GS} = −7V, T_A = 25°C		0.2	1.0		0.2	5.0	nA
				60			60	nA
FET Gate-Source Breakdown Voltage	I_G = 1.0 μA, V_{DS} = 0V	35			35			V
Drain-Gate Capacitance	V_{DG} = 20V, I_S = 0, f = 1.0 MHz, T_A = 25°C		4.0	5.0		4.0	5.0	pF
Source-Gate Capacitance	V_{DG} = 20V, I_D = 0, f = 1.0 MHz, T_A = 25°C		4.0	5.0		4.0	5.0	pF
Input 1 Turn-ON Time	V_{IN1} = 10V, T_A = 25°C (See Figure 1)		35	60		35	60	ns
Input 2 Turn-ON Time	V_{IN2} = 10V, T_A = 25°C (See Figure 1)		1.2	1.5		1.2	1.2	μs
Input 1 Turn-OFF Time	V_{IN1} = 10V, T_A = 25°C (See Figure 1)		0.6	0.75		0.6	0.75	μs
Input 2 Turn-OFF Time	V_{IN2} = 10V, T_A = 25°C (See Figure 1)		50	80		50	80	ns
DC Voltage Range	T_A = 25°C (See Figure 2)	±9.0	±10.0		±9.0	±10.0		V
AC Voltage Range	T_A = 25°C (See Figure 2)	±9.0	±10.0		±9.0	±10.0		V

Note 1: Unless otherwise specified these specifications apply for pin 12 connected to +15V, pin 2 connected to −15V, −55°C to 125°C for the AH2114, and 0°C to 85°C for the AH2114C.

Note 2: All typical values are for T_A = 25°C.

Note 3: Derate linearly at 100°C/W above 25°C.

Monolithic N-Channel Junction FET Switches With High Speed Drivers

AM181/AM281, AM182/AM282 dual driver with SPST switches
AM184/AM284, AM185/AM285 dual driver with DPST switches
AM187/AM287, AM188/AM288 single driver with SPDT switches
AM190/AM290, AM191/AM291 dual driver with SPDT switches

General Description

These devices combine N-channel junction FETs and bipolar transistors on a single chip for the first time in a new N-channel Bi-FET process.

This technology provides the industry's only low "ON" resistance, high speed, monolithic N-channel junction FET analog switch. Unique circuit techniques are employed to achieve break-before-make switching action and constant "ON" resistance over the analog voltage range. The switch can block 20V peak-to-peak signals, and because of the driver design, an "OFF" isolation greater than 60 dB is achieved at 10 MHz.

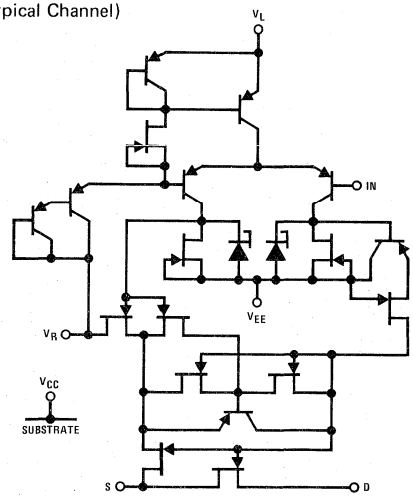
Features

- Interfaces with standard DTL, TTL and CMOS
- Constant "ON" resistance with signals to ±10V
- "ON" resistance match 2 Ω typ
- "OFF" isolation and crosstalk less than –60 dB at 10 MHz (typ)
- t_{ON}/t_{OFF} = 105 ns/95 ns typ
- Break-before-make action

Applications

- A-to-D/D-to-A converters
- Data acquisition
- Signal multiplexers
- Sample and hold
- Video switch

Schematic Diagram (Typical Channel)



Application Hints*

V_{CC} Positive Supply Voltage (V)	V_{EE} Negative Supply Voltage (V)	V_L Logic Supply Voltage (V)	V_R Reference Supply Voltage (V)	V_{IN} Logic Input Voltage V_{INH} Min/ V_{INL} Max– (V)	100 Series V_S Analog Voltage Range (V)	200 Series V_S Analog Signal Range (V)
+15**	–15	+5	Gnd	2.0/0.8	–7.5 to +15	–10 to +15
+10	–20	+5	Gnd	2.0/0.8	–12.5 to +10	–15 to +10
+12	–12	+5	Gnd	2.0/0.8	–4.5 to +12	–7 to +12

*Applications Hints are for design aid only, not guaranteed and not subject to production testing

**Electrical Parameter Chart based on V_{CC} + 15V, V_{EE} = –15V, V_L = 5V, V_R = Gnd

Absolute Maximum Ratings

$V_{CC} - V_{EE}$	36V
$V_{CC} - V_D$	33V
$V_D - V_{EE}$	33V
$V_D - V_S$	±22V
$V_L - V_{EE}$	36V
$V_L - V_{IN}$	8V
$V_L - V_R$	8V
$V_{IN} - V_R$	8V
$V_R - V_{EE}$	27V
$V_R - V_{IN}$	2V
Current (Any Terminal)	30 mA

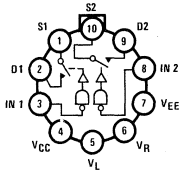
Storage Temperature	−65°C to +150°C
Operating Temperature	−55°C to +125°C
Power Dissipation*	
Metal Can**	450 mW
14-Pin DIP***	825 mW
16-Pin DIP****	900 mW

* All leads soldered to PC board
** Derate 6 mW/°C above 75°C
*** Derate 11 mW/°C above 75°C
**** Derate 12 mW/°C above 75°C

Connection Diagrams

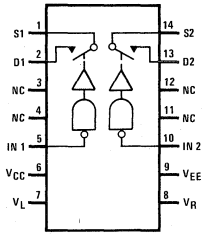
AM181/AM281, AM182/AM282▲

Metal Can Package
See Package 1
Order by Part Number
Followed by H Suffix



TOP VIEW

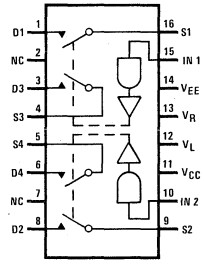
Switch states are for logical "1" input



TOP VIEW

Dual-In-Line Package
See Package 16
Order by Part Number
Followed by D Suffix

AM184/AM284, AM185/AM285▲



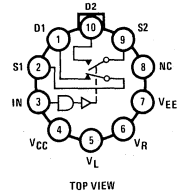
TOP VIEW

Dual-In-Line Package
See Package 17
Order by Part Number
Followed by D Suffix

Switch states are for logical "0" input

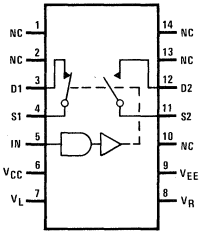
AM187/AM287, AM188/AM288▲

Metal Can Package
See Package 1
Order by Part Number
Followed by H Suffix



TOP VIEW

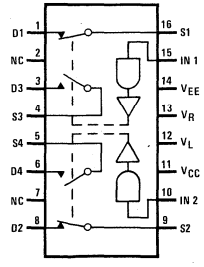
Switch states are for logical "1" input



TOP VIEW

Dual-In-Line Package
See Package 16
Order by Part Number
Followed by D Suffix

AM190/AM290, AM191/AM291▲



TOP VIEW

Dual-In-Line Package
See Package 17
Order by Part Number
Followed by D Suffix

Switch states are for logical "1" input

▲Consult local sales representative or factory for information concerning the 14-pin flat package

Electrical Characteristics AM181/AM281, AM182/AM282

dc parameters are 100% tested at 25°C; ac parameters, high and low temperatures, and t_{ON}, t_{OFF} are sampled to ensure conformance with specifications.

PARAMETER		TEST CONDITIONS, UNLESS NOTED: V_{CC} = 15V, V_{EE} = −15V, V_L = 5V, V_R = 0		MAX LIMITS AM181 −55°C	AM181 25°C	AM181 125°C	AM281 −20°C	AM281 25°C	AM281 85°C	UNITS
$r_{DS(ON)}$	Drain-Source "ON" Resistance	I_S = −10 mA, V_{IN} = 0.8V	V_D = −7.5V	30	30	60	50	50	75	Ω
$I_{S(OFF)}$	Source "OFF" Leakage Current	V_{IN} = 2V	V_S = 10V, V_D = −10V, V_{CC} = 10V, V_{EE} = −20V		1	100		5	100	nA
			V_S = 7.5V, V_D = −7.5V		1	100		5	100	
$I_{D(OFF)}$	Drain "OFF" Leakage Current		V_D = 10V, V_S = −10V, V_{CC} = 10V, V_{EE} = −20V		1	100		5	100	
			V_D = 7.5V, V_S = −7.5V		1	100		5	100	
$I_{D(ON)} + I_{S(ON)}$	Channel "ON" Leakage Current	V_{IN} = 0.8V	$V_D = V_S$ = −7.5V		−2	−200		−10	−200	
I_{INL}	Input Current, Input Voltage Low	V_{IN} = 0		−250	−250	−250	−250	−250	−250	μA
I_{INH}	Input Current, Input Voltage High	V_{IN} = 5V			10	20		10	20	
t_{ON}	Turn "ON" Time	See Switching Time Test Circuit			150			180		ns
t_{OFF}	Turn "OFF" Time				130			150		

PARAMETER		TEST CONDITIONS, UNLESS NOTED: V_{CC} = 15V, V_{EE} = −15V, V_L = 5V, V_R = 0		MAX LIMITS AM182 −55°C	AM182 25°C	AM182 125°C	AM282 −20°C	AM282 25°C	AM282 85°C	UNITS
$r_{DS(ON)}$	Drain-Source "ON" Resistance	I_S = −10 mA, V_{IN} = 0.8V	V_D = −10V	75	75	100	100	100	150	Ω
$I_{S(OFF)}$	Source "OFF" Leakage Current	V_{IN} = 2V	V_S = 10V, V_D = −10V, V_{CC} = 10V, V_{EE} = −20V		1	100		5	100	nA
			V_S = 10V, V_D = −10V		1	100		5	100	
$I_{D(OFF)}$	Drain "OFF" Leakage Current		V_D = 10V, V_S = −10V, V_{CC} = 10V, V_{EE} = −20V		1	100		5	100	
			V_D = 10V, V_S = −10V		1	100		5	100	
$I_{D(ON)} + I_{S(ON)}$	Channel "ON" Leakage Current	V_{IN} = 0.8V	$V_D = V_S$ = −10V		−2	−200		−10	−200	
I_{INL}	Input Current, Input Voltage Low	V_{IN} = 0		−250	−250	−250	−250	−250	−250	μA
I_{INH}	Input Current, Input Voltage High	V_{IN} = 5V			10	20		10	20	
t_{ON}	Turn "ON" Time	See Switching Time Test Circuit			250			300		ns
t_{OFF}	Turn "OFF" Time				130			150		

PARAMETER		TEST CONDITIONS, UNLESS NOTED: V_{CC} = 15V, V_{EE} = −15V, V_L = 5V, V_R = 0		MAX LIMITS AM181, AM182 −55°C	AM181, AM182 25°C	AM181, AM182 125°C	AM281, AM282 −20°C	AM281, AM282 25°C	AM281, AM282 85°C	UNITS
$C_{S(OFF)}$	Source "OFF" Capacitance	f = 1 MHz	V_S = −5V, I_D = 0	9 Typical, (Note 1)						pF
$C_{D(OFF)}$	Drain "OFF" Capacitance		V_D = −5V, I_S = 0	6 Typical, (Note 1)						
$C_{D(ON)} + C_{S(ON)}$	Channel "ON" Capacitance		$V_D = V_S$ = 0	14 Typical, (Note 1)						
	"OFF" Isolation	R_L = 75 Ω		> 60 dB at 10 MHz Typical, (Note 1)						
I_{CC}	Positive Supply Current	Both V_{IN} = 0, All Channels "ON"			0.1			0.1		mA
I_{EE}	Negative Supply Current				−5			−5		
I_L	Logic Supply Current				4.5			4.5		
I_R	Reference Supply Current				−2			−2		
I_{CC}	Positive Supply Current	Both V_{IN} = 5V, All Channels "OFF"			0.1			0.1		
I_{EE}	Negative Supply Current				−5			−5		
I_L	Logic Supply Current				4.5			4.5		
I_R	Reference Supply Current				−2			−2		

Note 1: Typical values are for Design Aid *only*, not guaranteed and not subject to production testing.

Electrical Characteristics AM184/AM284, AM185/AM285

dc parameters are 100% tested at 25°C; ac parameters, high and low temperatures, and t_{ON}, t_{OFF} are sampled to ensure conformance with specifications.

PARAMETER		TEST CONDITIONS, UNLESS NOTED: V_{CC} = 15V, V_{EE} = −15V, V_L = 5V, V_R = 0		MAX LIMITS AM184 −55°C	AM184 25°C	AM184 125°C	AM284 −20°C	AM284 25°C	AM284 85°C	UNITS
$r_{DS(ON)}$	Drain-Source ON Resistance	I_S=−10 mA, V_{IN} = 2V	V_D = −7.5V	30	30	60	50	50	75	Ω
$I_{S(OFF)}$	Source OFF Leakage Current	V_{IN} = 0.8V	V_S = 10V, V_D = −10V, V_{CC} = 10V, V_{EE} = −20V		1	100		5	100	nA
			V_S = 7.5V, V_D = −7.5V		1	100		5	100	
$I_{D(OFF)}$	Drain OFF Leakage Current		V_D = 10V, V_S = −10V, V_{CC} = 10V, V_{EE} = −20V		1	100		5	100	
			V_D = 7.5V, V_S = −7.5V		1	100		5	100	
$I_{D(ON)} + I_{S(ON)}$	Channel ON Leakage Current	V_{IN} = 2V	V_D = V_S = −7.5V		−2	−200		−10	−200	
I_{INL}	Input Current, Input Voltage Low	V_{IN} = 0		−250	−250	−250	−250	−250	−250	µA
I_{INH}	Input Current, Input Voltage High	V_{IN} = 5V			10	20		10	20	
t_{ON}	Turn ON Time	See Switching Time Test Circuit			150			180		ns
t_{OFF}	Turn OFF Time				130			150		

PARAMETER		TEST CONDITIONS, UNLESS NOTED: V_{CC} = 15V, V_{EE} = −15V, V_L = 5V, V_R = 0		MAX LIMITS AM185 −55°C	AM185 25°C	AM185 125°C	AM285 −20°C	AM285 25°C	AM285 85°C	UNITS
$r_{DS(ON)}$	Drain-Source ON Resistance	I_S = −10V, V_{IN} = 2V	V_D = −10V	75	75	150	100	100	150	Ω
$I_{S(OFF)}$	Source OFF Leakage Current	V_{IN} = 0.8V	V_S = 10V, V_D = −10V, V_{CC} = 10V, V_{EE} = −20V		1	100		5	100	nA
			V_S = 10V, V_D = −10V		1	100		5	100	
$I_{D(OFF)}$	Drain OFF Leakage Current		V_D = 10V, V_S = −10V, V_{CC} = 10V, V_{EE} = −20V		1	100		5	100	
			V_D = 10V, V_S = −10V		1	100		5	100	
$I_{D(ON)} + I_{S(ON)}$	Channel ON Leakage Current	V_{IN} = 2V	V_D = V_S = −10V		−2	−200		−10	−200	
I_{INL}	Input Current, Input Voltage Low	V_{IN} = 0		−250	−250	−250	−250	−250	−250	µA
I_{INH}	Input Current, Input Voltage High	V_{IN} = 5V			10	20		10	20	
t_{ON}	Turn ON Time	See Switching Time Test Circuit			250			300		ns
t_{OFF}	Turn OFF Time				130			150		

PARAMETER		TEST CONDITIONS, UNLESS NOTED: V_{CC} = 15V, V_{EE} = −15V, V_L = 5V, V_R = 0		MAX LIMITS AM184, AM185 −55°C	AM184, AM185 25°C	AM184, AM185 125°C	AM284, AM285 −20°C	AM284, AM285 25°C	AM284, AM285 85°C	UNITS
$C_{S(OFF)}$	Source OFF Capacitance	f = 1 MHz	V_S = −5V, I_D = 0	9 Typical, (Note 1)						pF
$C_{D(OFF)}$	Drain OFF Capacitance		V_D = −5V, I_S = 0	6 Typical, (Note 1)						
$C_{D(ON)} + C_{S(ON)}$	Channel ON Capacitance		V_D = V_S = 0	14 Typical, (Note 1)						
	"OFF" Isolation	R_L = 75 Ω		> 60 dB at 10 MHz Typical, (Note 1)						
I_{CC}	Positive Supply Current	Both V_{IN} = 5V, All Channels "ON"			0.1			0.1		mA
I_{EE}	Negative Supply Current				−4			−4		
I_L	Logic Supply Current				4.5			4.5		
I_R	Reference Supply Current				−2			−2		
I_{CC}	Positive Supply Current	Both V_{IN} = 0, All Channels "OFF"			0.1			0.1		
I_{EE}	Negative Supply Current				−5.5			−5.5		
I_L	Logic Supply Current				4.5			4.5		
I_R	Reference Supply Current				−2			−2		

Note 1: Typical values are for Design Aid *only*, not guaranteed and not subject to production testing.

Electrical Characteristics AM187/AM287, AM188/AM288

dc parameters are 100% tested at 25°C; ac parameters, high and low temperatures, and t_{ON}, t_{OFF} are sampled to ensure conformance with specifications.

PARAMETER		TEST CONDITIONS, UNLESS NOTED: V_{CC} = 15V, V_{EE} = −15V, V_L = 5V, V_R = 0		MAX LIMITS AM187 −55°C	AM187 25°C	AM187 125°C	AM287 −20°C	AM287 25°C	AM287 85°C	UNITS
$r_{DS(ON)}$	Drain-Source "ON" Resistance	I_S = −10 mA, V_{IN} = 2V, Ch. 1 "ON", V_{IN} = 0.8V, Ch. 2 "ON"	V_D = −7.5V	30	30	60	50	50	75	Ω
$I_{S(OFF)}$	Source "OFF" Leakage Current	V_{IN} = 2V, Ch. 2 "OFF" V_{IN} = 0.8V, Ch. 1 "OFF"	V_S = 10V, V_D = −10V, V_{CC} = 10V, V_{EE} = −20V		1	100		5	100	nA
			V_S = 7.5V, V_D = −7.5V		1	100		5	100	
$I_{D(OFF)}$	Drain "OFF" Leakage Current		V_D = 10V, V_S = −10V, V_{CC} = 10V, V_{EE} = −20V		1	100		5	100	
			V_D = 7.5V, V_S = −7.5V		1	100		5	100	
$I_{D(ON)} + I_{S(ON)}$	Channel "ON" Leakage Current	V_{IN} = 2V, Ch. 1 "ON" V_{IN} = 0.8V, Ch. 2 "ON"	$V_D = V_S$ = −7.5V		−2	−200		−10	−200	
I_{INL}	Input Current, Input Voltage Low	V_{IN} = 0		−250	−250	−250	−250	−250	−250	μA
I_{INH}	Input Current, Input Voltage High	V_{IN} = 5V			10	20		10	20	
t_{ON}	Turn "ON" Time	See Switching Time Test Circuit			150			180		ns
t_{OFF}	Turn "OFF" Time				130			150		

PARAMETER		TEST CONDITIONS, UNLESS NOTED: V_{CC} = 15V, V_{EE} = −15V, V_L = 5V, V_R = 0		MAX LIMITS AM188 −55°C	AM188 25°C	AM188 125°C	AM288 −20°C	AM288 25°C	AM288 85°C	UNITS
$r_{DS(ON)}$	Drain-Source "ON" Resistance	I_S = −10 mA, V_{IN} = 0.8V, Ch. 2 "ON", V_{IN} = 2V, Ch. 1 "ON"	V_D = −10V	75	75	150	100	100	150	Ω
$I_{S(OFF)}$	Source "OFF" Leakage Current	V_{IN} = 0.8V, Ch. 1 "OFF" V_{IN} = 2V, Ch. 2 "OFF"	V_S = 10V, V_D = −10V, V_{CC} = 10V, V_{EE} = −20V		1	100		5	100	nA
			V_S = 10V, V_D = −10V		1	100		5	100	
$I_{D(OFF)}$	Drain "OFF" Leakage Current		V_D = 10V, V_S = −10V, V_{CC} = 10V, V_{EE} = −20V		1	100		5	100	
			V_D = 10V, V_S = −10V		1	100		5	100	
$I_{D(ON)} + I_{S(ON)}$	Channel "ON" Leakage Current	V_{IN} = 2V, Ch. 1 "ON" V_{IN} = 0.8V, Ch. 2 "ON"	$V_D = V_S$ = −10V		−2	−200		−10	−200	
I_{INL}	Input Current, Input Voltage Low	V_{IN} = 0		−250	−250	−250	−250	−250	−250	μA
I_{INH}	Input Current, Input Voltage High	V_{IN} = 5V			10	20		10	20	
t_{ON}	Turn "ON" Time	See Switching Time Test Circuit			250			300		ns
t_{OFF}	Turn "OFF" Time				130			150		

PARAMETER		TEST CONDITIONS, UNLESS NOTED: V_{CC} = 15V, V_{EE} = −15V, V_L = 5V, V_R = 0		MAX LIMITS AM187, AM188 −55°C	AM187, AM188 25°C	AM187, AM188 125°C	AM287, AM288 −20°C	AM287, AM288 25°C	AM287, AM288 85°C	UNITS
$C_{S(OFF)}$	Source "OFF" Capacitance	f = 1 MHz	V_S = −5V, I_D = 0	9 Typical, (Note 1)						pF
$C_{D(OFF)}$	Drain "OFF" Capacitance		V_D = 5V, I_S = 0	6 Typical, (Note 1)						
$C_{D(ON)} + C_{S(ON)}$	Channel "ON" Capacitance		$V_D = V_S$ = 0	14 Typical, (Note 1)						
	"OFF" Isolation	R_L = 75Ω		> 60 dB at 10 MHz Typical, (Note 1)						
I_{CC}	Positive Supply Current	V_{IN} = 0, Ch. 2 "ON", Ch. 1 "OFF"			0.1			0.1		mA
I_{EE}	Negative Supply Current				−3			−3		
I_L	Logic Supply Current				3.2			3.2		
I_R	Reference Supply Current				−2			−2		
I_{CC}	Positive Supply Current	V_{IN} = 5V, Ch. 2 "OFF", Ch. 1 "ON"			0.1			0.1		
I_{EE}	Negative Supply Current				−3			−3		
I_L	Logic Supply Current				3.2			3.2		
I_R	Reference Supply Current				−2			−2		

Note 1: Typical values are for Design Aid *only*, not guaranteed and not subject to production testing.

Electrical Characteristics AM190/AM290, AM191/AM291

dc parameters are 100% tested at 25°C; ac parameters, high and low temperatures, and t_{ON}, t_{OFF} are sampled to ensure conformance with specifications.

PARAMETER		TEST CONDITIONS, UNLESS NOTED: V_{CC} = 15V, V_{EE} = −15V, V_L = 5V, V_R = 0		MAX LIMITS AM190 −55°C	AM190 25°C	AM190 125°C	AM290 −20°C	AM290 25°C	AM290 85°C	UNITS
$r_{DS(ON)}$	Drain-Source ON Resistance	I_S = −10 mA, V_{IN} = 2V, Ch. 1 and 2 "ON", V_{IN} = 0.8V, Ch. 3 and 4 "ON"	V_D = −7.5V	30	30	60	50	50	75	Ω
$I_{S(OFF)}$	Source OFF Leakage Current	V_{IN} = 2V, Ch. 3 and 4 "OFF" V_{IN} = 0.8V, Ch. 1 and 2 "OFF"	V_S = 10V, V_D = −10V, V_{CC} = 10V, V_{EE} = −20V		1	100		5	100	nA
			V_S = 7.5V, V_D = −7.5V		1	100		5	100	
$I_{D(OFF)}$	Drain OFF Leakage Current		V_D = 10V, V_S = −10V, V_{CC} = 10V, V_{EE} = −20V		1	100		5	100	
			V_D = 7.5V, V_S = −7.5V		1	100		5	100	
$I_{D(ON)} + I_{S(ON)}$	Channel ON Leakage Current	V_{IN} = 2V, Ch. 1 and 2 "ON" V_{IN} = 0.8V, Ch. 3 and 4 "ON"	$V_D = V_S$ = −7.5V		−2	−200		−10	−200	
I_{INL}	Input Current, Input Voltage Low	V_{IN} = 0		−250	−250	−250	−250	−250	−250	μA
I_{INH}	Input Current, Input Voltage High	V_{IN} = 5V			10	20		10	20	
t_{ON}	Turn ON Time	See Switching Time Test Circuit			150			180		ns
t_{OFF}	Turn OFF Time				130			150		

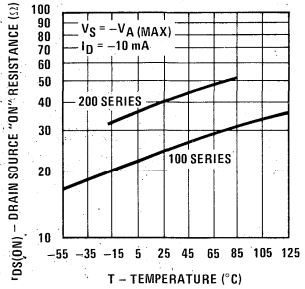
PARAMETER		TEST CONDITIONS, UNLESS NOTED: V_{CC} = 15V, V_{EE} = −15V, V_L = 5V, V_R = 0		MAX LIMITS AM191 −55°C	AM191 25°C	AM191 125°C	AM291 −20°C	AM291 25°C	AM291 85°C	UNITS
$r_{DS(ON)}$	Drain-Source ON Resistance	I_S = −10 mA, V_{IN} = 0.8V, Ch. 3 and 4 "ON", V_{IN} = 2V, Ch. 1 and 2 "ON"	V_D = −10V	75	75	150	100	100	150	Ω
$I_{S(OFF)}$	Source OFF Leakage Current	V_{IN} = −0.8V, Ch. 1 and 2 "OFF" V_{IN} = 2V, Ch 3 and 4 "OFF"	V_S = 10V, V_D = −10V, V_{CC} = 10V, V_{EE} = −20V		1	100		5	100	nA
			V_S = 10V, V_D = −10V		1	100		5	100	
$I_{D(OFF)}$	Drain OFF Leakage Current		V_D = 10V, V_S = −10V, V_{CC} = 10V, V_{EE} = −20V		1	100		5	100	
			V_D = 10V, V_S = −10V		1	100		5	100	
$I_{D(ON)} + I_{S(ON)}$	Channel ON Leakage Current	V_{IN} = 0.8V, Ch. 3 and 4 "ON" V_{IN} = 2V, Ch. 1 and 2 "ON"	$V_D = V_S$ = −10V		−2	−200		−10	−200	
I_{INL}	Input Current, Input Voltage Low	V_{IN} = 0		−250	−250	−250	−250	−250	−250	μA
I_{INH}	Input Current, Input Voltage High	V_{IN} = 5V			10	20		10	20	
t_{ON}	Turn ON Time	See Switching Time Test Circuit			250			300		ns
t_{OFF}	Turn OFF Time				130			150		

PARAMETER		TEST CONDITIONS, UNLESS NOTED: V_{CC} = 15V, V_{EE} = −15V, V_L = 5V, V_R = 0		MAX LIMITS AM190, AM191 −55°C	AM190, AM191 25°C	AM190, AM191 125°C	AM290, AM291 −20°C	AM290, AM291 25°C	AM290, AM291 85°C	UNITS
$C_{S(OFF)}$	Source OFF Capacitance	f = 1 MHz	V_S = −5V, I_D = 0	9 Typical, (Note 1)						pF
$C_{D(OFF)}$	Drain OFF Capacitance		V_D = 5V, I_S = 0	6 Typical, (Note 1)						
$C_{D(ON)} + C_{S(ON)}$	Channel ON Capacitance		$V_D = V_S$ = 0	14 Typical, (Note 1)						
	"OFF" Isolation	R_L = 75 Ω		> 60 dB at 10 MHz Typical, (Note 1)						
I_{CC}	Positive Supply Current	V_{IN} = 0, Ch. 3 and 4 "ON", Ch. 1 and 2 "OFF"			0.1			0.1		mA
I_{EE}	Negative Supply Current				−5			−5		
I_L	Logic Supply Current				4.5			4.5		
I_R	Reference Supply Current				−2			−2		
I_{CC}	Positive Supply Current	V_{IN} = 5V, Ch. 3 and 4 "OFF", Ch. 1 and 2 "ON"			0.1			0.1		
I_{EE}	Negative Supply Current				−5			−5		
I_L	Logic Supply Current				4.5			4.5		
I_R	Reference Supply Current				−2			−2		

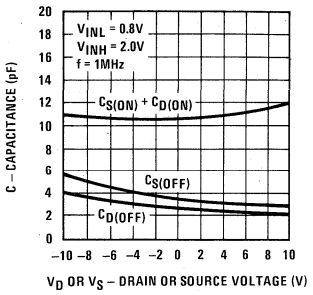
Note 1: Typical values are for Design Aid *only*, not guaranteed and not subject to production testing.

Typical Performance Characteristics V_{CC} = 15V, V_{EE} = −15V, V_L = 5V, V_R = 0 unless otherwise noted.

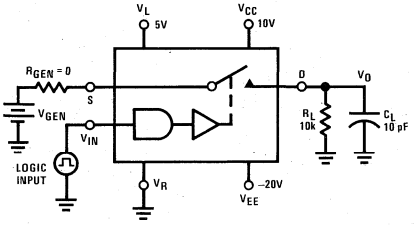
$r_{DS(ON)}$ vs V_D and Temperature



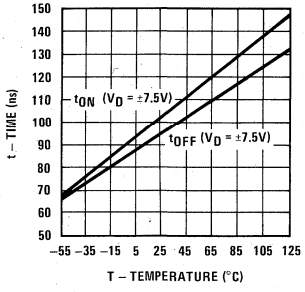
Capacitance vs V_D or V_S



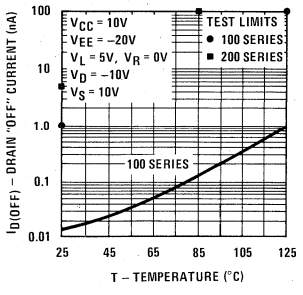
Typical delay, rise, fall, settling times, and switching transients in this circuit.



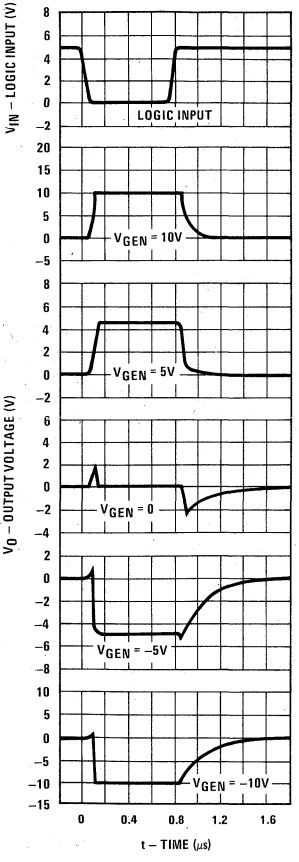
Switching Time vs V_D and Temperature



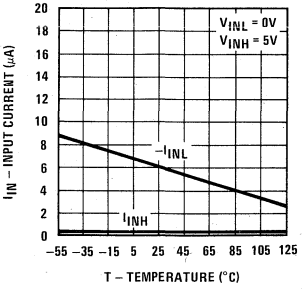
$I_{D(OFF)}$ vs Temperature



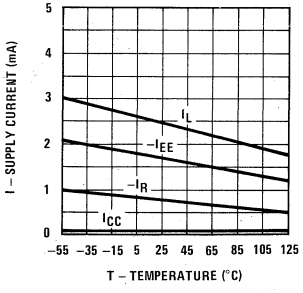
If R_{GEN}, R_L or C_L is increased there will be proportional increases in rise and/or fall RC times.



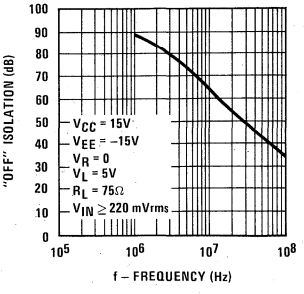
I_{IN} vs V_{IN} and Temperature



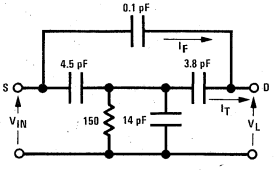
Supply Current vs Temperature



"OFF" Isolation vs Frequency

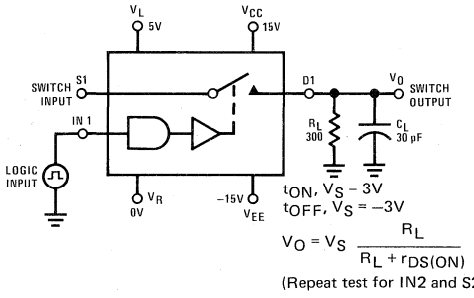


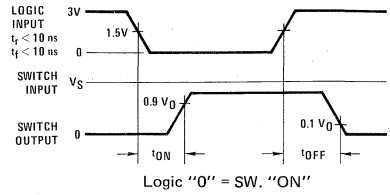
Equivalent "OFF" Circuit



Switching Time Test Circuit

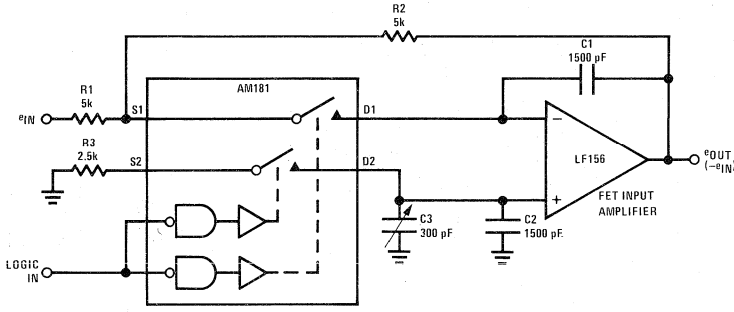
Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or − as per switching time test circuit. V_O is the steady state output with switch "ON". Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.





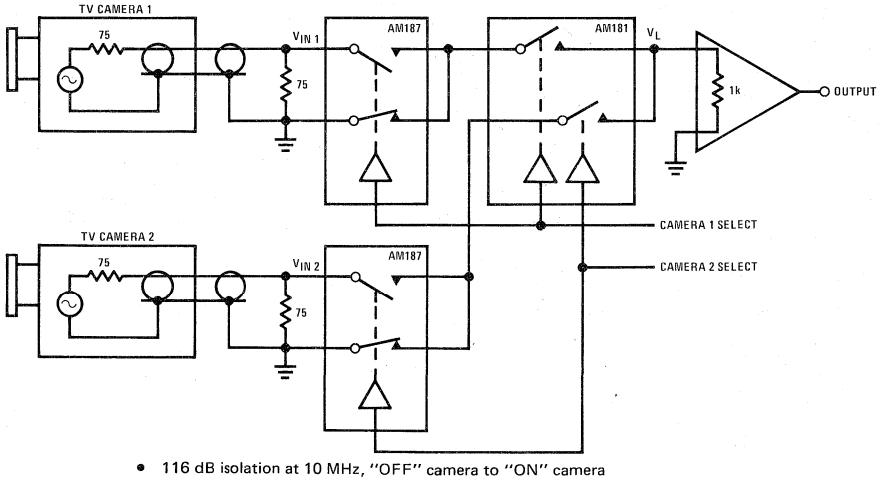
Typical Applications

Low Drift-Compensated Sample and Hold



- Input impedance 5 kΩ
- Slew rate limiting and 3 dB point: 20V swing: 3.2K C; 5V swing: 12K C; small signal: 21K C
- Droop rate @ 25°C 0.5 nV per μs
- Sample to hold offset adjustable to zero
- Acquisition time—98 μs
- Aperture time—80 ns
- Aperture uncertainty—2 ns

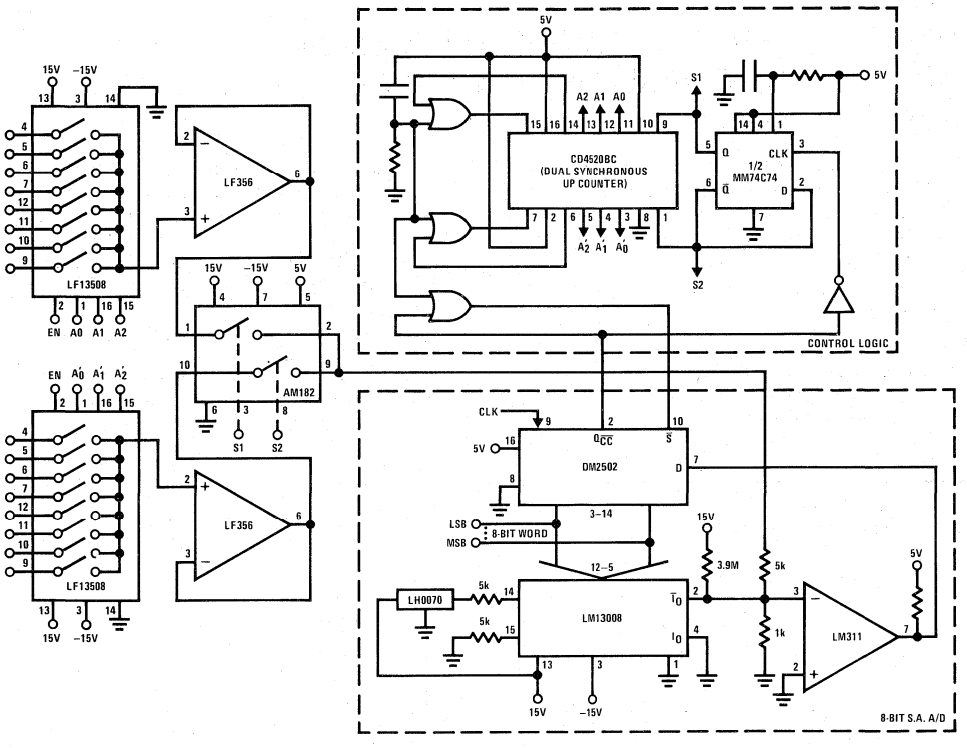
Video Switch with Very High "OFF" Isolation
(f = dc to 10 MHz)



- 116 dB isolation at 10 MHz, "OFF" camera to "ON" camera
- 98 dB isolation at 10 MHz, load from each camera when both cameras are "OFF"
- < 1 dB on insertion loss

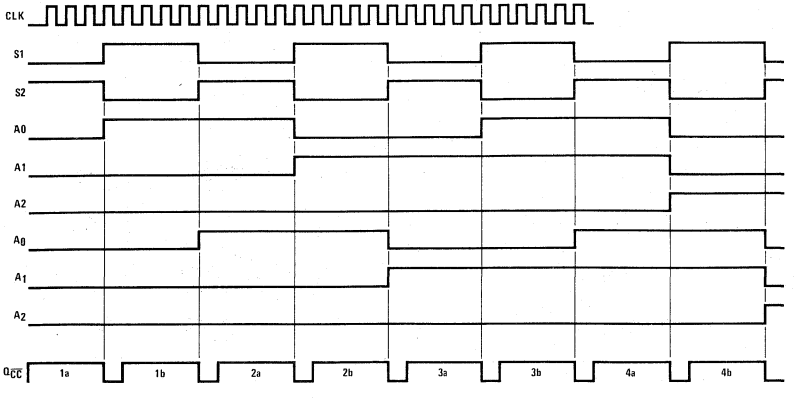
Typical Applications (Continued)

A 16-Channel Data Acquisition Unit with Second Level Multiplexing



- Maximum A/D clock frequency: 4.5 MHz
- Maximum throughput rate: 31.25k samples/sec
- Minimum switch "ON" time for the 2-channel MUX: $t_{ON(min)} \leq 1/4.5$ MHz
- Maximum input signal bandwidth 15.6 kHz
- Maximum input signal variation during conversion for 8-bit accuracy and 10V full scale: $\Delta V_{IN}/\Delta T = 19.5\ mV/\mu s$

Timing Diagram



AM2009/AM2009C, MM4504/MM5504
6-Channel MOS Multiplex Switches

General Description

The AM2009/AM2009C/MM4504/MM5504 are six channel multiplex switches constructed on a single silicon chip using low threshold P-channel MOS process. The gate of each MOS device is protected by a diode circuit.

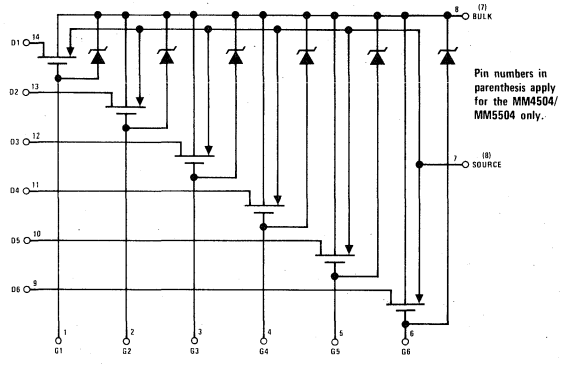
The AM2009/AM2009C/MM4504/MM5504 are designed for applications such as time division multiplexing of analog or digital signals. Switching speeds are primarily determined by conditions external to the device such as signal source impedance, capacitive loading and the total number of channels used in parallel.

The AM2009/MM4504 are specified for operation over the -55°C to +125°C military temperature range. The AM2009C/MM5504 are specified for operation over the -25°C to +85°C temperature range.

Features

- Typical low "on" resistance 150Ω
- Typical low "off" leakage 100 pA
- Typical large analog voltage range ±10V
- Zero inherent offset voltage
- Normally off with zero gate voltage

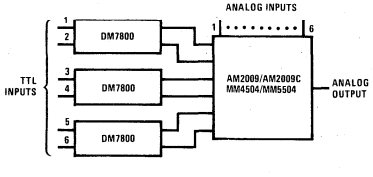
Schematic Diagrams



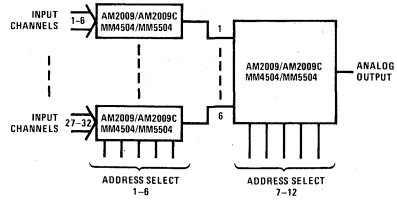
Order Number
AM2009F or AM2009CF
MM4504F or MM5540F
See Package 23

Order Number
AM2009D or AM2009CD
MM4504D or MM5504D
See Package 14

Typical Applications



TTL Compatible 6 Channel MUX



32 Channel MUX

Absolute Maximum Ratings (V_{BULK} = 0V)

Voltage on Any Source or Drain	−30V	Total Power Dissipation (at T_A = 25°C)	900 mW
Voltage on Any Gate	−35V	Power Dissipation — each gate circuit	150 mW
Positive Voltage on Any Pin	+0.3V	Operating Temperature Range AM2009	−55°C to +125°C
Source or Drain Current	50 mA	AM2009C	−25°C to +85°C
Gate Current (forward direction of zener clamp)	0.1 mA	Storage Temperature Range	−65°C to +150°C
		Lead Temperature (Soldering, 10 sec)	300°C

Electrical Characteristics (Note 1)

PARAMETER	CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Threshold Voltage	$V_{GS} = V_{DS}$, $I_{DS} = -1\ \mu A$	−1.0		−3.0	V
DC ON Resistance	$V_{GS} = -20V$, $I_{DS} = -100\ \mu A$, $T_A = 25°C$		150	250	Ω
DC ON Resistance	$V_{GS} = -10V$, $V_{SB} = -20V$, $I_{DS} = -100\ \mu A$, $T_A = 25°C$		500	1250	Ω
DC ON Resistance	$V_{GS} = -20V$, $I_{DS} = -100\ \mu A$			325	Ω
DC ON Resistance	$V_{GS} = -10V$, $V_{SB} = -20V$, $I_{DS} = -100\ \mu A$			1500	Ω
Gate Leakage	$V_{GS} = -20V$, Note 2 $V_{GS} = -20V$, Note 2, $T_A = 25°C$		 100	1.0	μA pA
Input Leakage	$V_{DS} = -20V$, Note 2 $V_{DS} = -20V$, Note 2, $T_A = 25°C$		 100	1.0	μA pA
Output Leakage	$V_{SD} = -20V$, Note 2 $V_{SD} = -20V$, Note 2, $T_A = 25°C$		 500	3.0	μA pA
Gate-Bulk Breakdown Voltage	$I_{GB} = -10\ \mu A$, Note 2	−35			V
Source-Drain Breakdown Voltage	$I_{SD} = -10\ \mu A$, $V_{GD} = 0$, Note 2	−30			V
Drain-Source Breakdown Voltage	$I_{DS} = -10\ \mu A$, $V_{GS} = 0$, Note 2	−30			V
Transconductance			4000		mhos
Gate Capacitance	Note 3, f = 1 MHz		4.7	8	pF
Input Capacitance	Note 3, f = 1 MHz		4.6	8	pF
Output Capacitance	Note 3, f = 1 MHz		16	20	pF

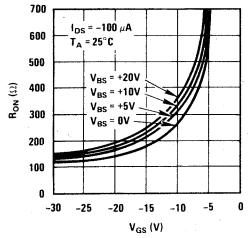
Note 1: Ratings apply over the specified temperature range and V_{BULK} = 0, unless otherwise specified.

Note 2: All other pins grounded.

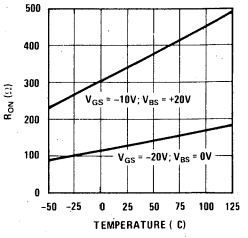
Note 3: Capacitance measured on dual-in-line package between pin under measurement to all other pins. Capacitances are guaranteed by design.

Typical Performance Characteristics

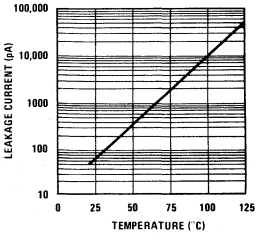
"ON" Resistance vs Gate-to-Source Voltage



"ON" Resistance vs T Temperature



Input Leakage Current vs Temperature



AM3705/AM3705C 8-Channel MOS Analog Multiplexer

General Description

The AM3705/AM3705C is an eight-channel MOS analog multiplex switch. TTL compatible logic inputs that require no level shifting or input pull-up resistors and operation over a wide range of supply voltages is obtained by constructing the device with low threshold P-channel enhancement MOS technology. To simplify external logic requirements, a one-of-eight decoder and an output enable are included in the device.

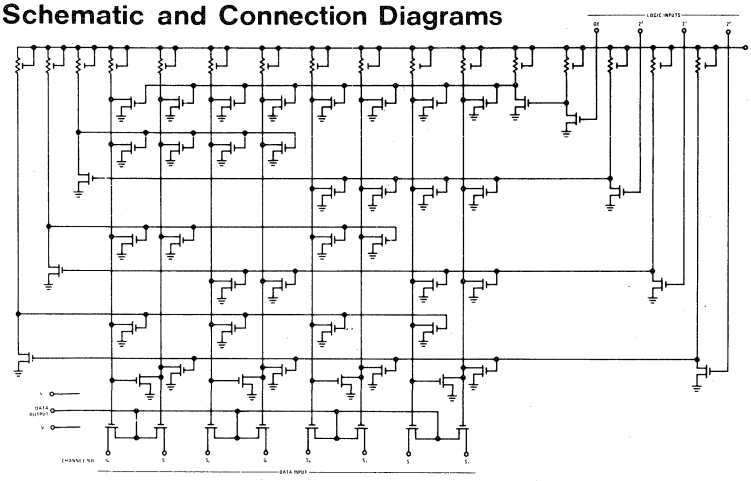
Important design features include:

- TTL/DTL compatible input logic levels
- Operation from standard +5V and −15V supplies
- Wide analog voltage range — ±5V
- One-of-eight decoder on chip
- Output enable control
- Low ON resistance — 150Ω
- Input gate protection
- Low leakage currents — 0.5 nA

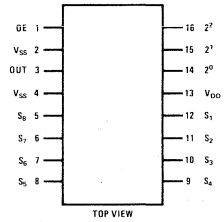
The AM3705/AM3705C is designed as a low cost analog multiplex switch to fulfill a wide variety of data acquisition and data distribution applications including cross-point switching, MUX front ends for A/D converters, process controllers, automatic test gear, programmable power supplies and other military or industrial instrumentation applications.

The AM3705 is specified for operation over the −55°C to +125°C military temperature range. The AM3705C is specified for operation over the −25°C to +85°C temperature range.

Schematic and Connection Diagrams

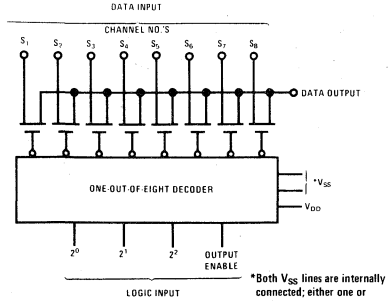


Dual-In-Line Package



Order Number
AM3705D or AM3705CD
See Package 15
AM3705F or AM3705CF
See Package 24

Block Diagram (MIL-STD-806B)



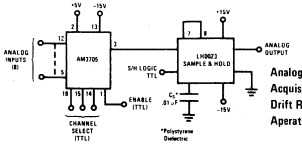
*Both V_{SS} lines are internally connected; either one or both may be used.

Truth Table

LOGIC INPUTS				CHANNEL
2^0	2^1	2^2	OE	ON
L	L	L	H	S_1
H	L	L	H	S_2
L	H	L	H	S_3
H	H	L	H	S_4
L	L	H	H	S_5
H	L	H	H	S_6
L	H	H	H	S_7
H	H	H	H	S_8
X	X	X	L	OFF

Typical Application

Buffered 8-Channel Multiplex, Sample and Hold



Analog Signal Range — 0.5V
Acquisition Time — 25 ns
Drift Rate — 0.5 mV/sec
Aperture Time — 250 ns

Absolute Maximum Ratings

Positive Voltage on Any Pin (Note 1)		+0.3V
Negative Voltage on Any Pin (Note 1)		−35V
Source to Drain Current		±30 mA
Logic Input Current		±0.1 mA
Power Dissipation (Note 2)		500 mW
Operating Temperature Range	AM3705	−55°C to +125°C
	AM3705C	−25°C to +85°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

Electrical Characteristics (Note 3)

PARAMETER	SYMBOL	CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
ON Resistance	R_{ON}	$V_{IN} = V_{SS}$; $I_{OUT} = 100\ \mu A$		80	250	Ω
ON Resistance	R_{ON}	$V_{IN} = -5V$; $I_{OUT} = -100\ \mu A$		160	400	Ω
ON Resistance	R_{ON}	$V_{IN} = -5V$; $I_{OUT} = -100\ \mu A$				
AM3705		$T_A = +125°C$			400	Ω
AM3705C		$T_A = +70°C$			400	Ω
ON Resistance	R_{ON}	$V_{IN} = +5V$; $V_{DD} = -15V$; $I_{OUT} = 100\ \mu A$		100		Ω
ON Resistance	R_{ON}	$V_{IN} = 0V$, $V_{DD} = -15V$, $I_{OUT} = -100\ \mu A$		150		Ω
ON Resistance	R_{ON}	$V_{IN} = -5V$; $V_{DD} = -15V$; $I_{OUT} = -100\ \mu A$		250		Ω
OFF Resistance	R_{OFF}			10^{10}		Ω
Output Leakage Current	I_{LO}	$V_{SS} - V_{OUT} = 15V$		0.5	10	nA
AM3705	I_{LO}	$V_{SS} - V_{OUT} = 15V$; $T_A = 125°C$		150	500	nA
AM3705C	I_{LO}	$V_{SS} - V_{OUT} = 15V$; $T_A = 70°C$		35	500	nA
Data Input Leakage Current	I_{LDI}	$V_{SS} - V_{IN} = 15V$		0.1	3.0	nA
AM3705	I_{LDI}	$V_{SS} - V_{IN} = 15V$; $T_A = 125°C$		25	500	nA
AM3705C	I_{LDI}	$V_{SS} - V_{IN} = 15V$; $T_A = 70°C$		0.5	500	nA
Logic Input Leakage Current	I_{LI}	$V_{SS} - V_{Logic\ In} = 15V$		.001	1	μA
AM3705	I_{LI}	$V_{SS} - V_{Logic\ In} = 15V$; $T_A = 125°C$		.05	10	μA
AM3705C	I_{LI}	$V_{SS} - V_{Logic\ In} = 15V$; $T_A = 70°C$		.05	10	μA
Logic Input LOW Level	V_{IL}	$V_{SS} = +5.0V$		0.5	1.0	V
Logic Input LOW Level	V_{IL}		V_{DD}		$V_{SS} - 4.0$	V
Logic Input HIGH Level	V_{IH}	$V_{SS} = +5.0V$	3.0	3.5		V
Logic Input HIGH Level	V_{IH}		$V_{SS} - 2.0$		$V_{SS} + 0.3$	V
Channel Switching Time-Positive	t^+	Switching Time		300		ns
Channel Switching Time-Negative	t^-	Test Circuit		600		ns
Channel Separation		f = 1 kHz		62		dB
Output Capacitance	C_{db}	$V_{SS} - V_{OUT} = 0$; f = 1 MHz		35		pF
Data Input Capacitance	C_{sb}	$V_{SS} - V_{DIP} = 0$; f = 1 MHz		6.0		pF
Logic Input Capacitance	C_{cg}	$V_{SS} - V_{Logic\ In} = 0$; f = 1 MHz		6.0		pF
Power Dissipation	P_D	$V_{DD} = -31V$, $V_{SS} = 0V$		125	175	mW

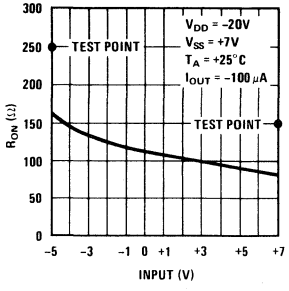
Note 1: All voltages referenced to V_{SS}.

Note 2: Ratings applies for ambient temperatures to +25°C, derate linearly at 3 mW/°C for ambient temperatures above +25°C.

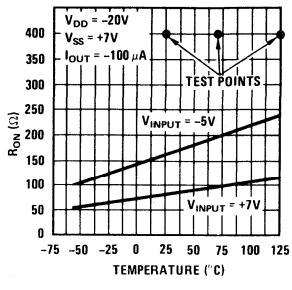
Note 3: Specifications apply for $T_A = 25°C$, $-24V \leq V_{DD} \leq -20V$, and $+5.0V \leq V_{SS} \leq +7.0V$; unless otherwise specified (all voltages are referenced to ground).

Typical Performance Characteristics

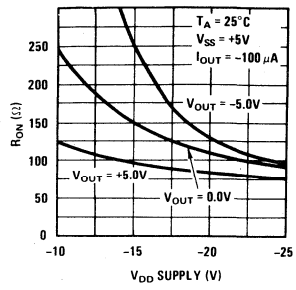
ON Resistance vs Analog Input Voltage



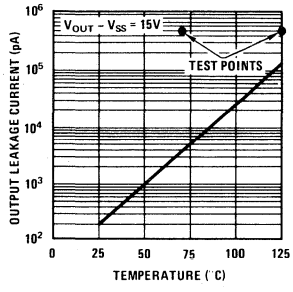
ON Resistance vs Ambient Temperature



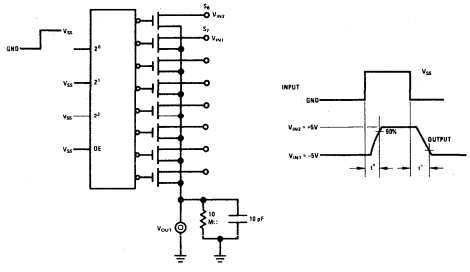
ON Resistance vs V_{DD} Supply Voltage



Output Leakage Current vs Ambient Temperature

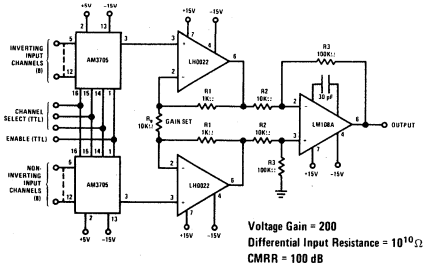


Switching Time Test Circuit



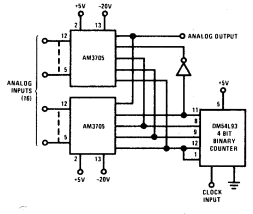
Typical Applications (Continued)

Differential Input MUX

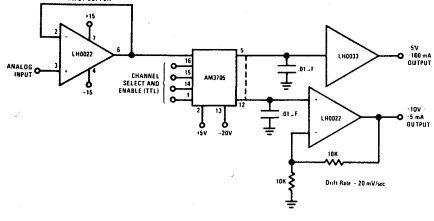


Voltage Gain = 200
Differential Input Resistance = $10^{10}\Omega$
CMRR = 100 dB
Input Current = 0.5 nA

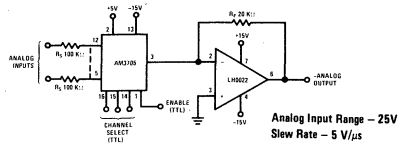
16-Channel Commutator



8-Channel Demultiplexer with Sample and Hold



Wide Input Range Analog Switch



Analog Input Range – 25V
Slew Rate – 5 V/μs

AM9709, AM97C09, AH5009 Series Monolithic Analog Current Switches

General Description

A versatile family of monolithic JFET analog switches designed to economically fulfill a wide variety of multiplexing and analog switching applications.

Even numbered switches may be driven directly from standard 5V logic, whereas the odd numbered switches are intended for applications utilizing 10V or 15V logic. The monolithic construction guarantees tight resistance match and track.

The AM97C09 series is specifically intended to be driven from CMOS providing the best performance at lowest cost.

Applications

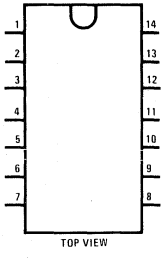
- AD/DA converters
- Micropower converters
- Industrial controllers
- Position controllers
- Data acquisition
- Active filters
- Signal multiplexers/demultiplexers
- Multiple channel AGC
- Quad compressors/expanders
- Choppers/demodulators
- Programmable gain amplifiers
- High impedance voltage buffer
- Sample and hold

Features

Interfaces with standard TTL and CMOS	
On-resistance match	2 ohms
Low "ON" resistance	100 ohms
Very low leakage	50 pA
Large analog signal range	±10V peak
High switching speed	150 ns
Excellent isolation between channels	80 dB at 1 kHz

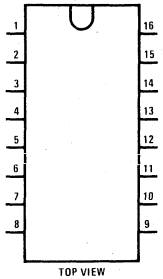
Connection Diagrams

Dual-In-Line Package



Order Number AM9709CN, AM9710CN, AM97C09CN, AM97C10CN, AH5009CN, AH5010CN, AH5013CN or AH5014CN
See Package 21

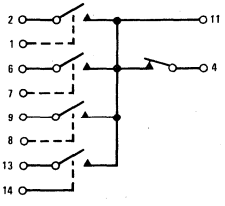
Dual-In-Line Package



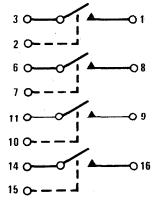
Order Number AM9711CN, AM9712CN, AM97C09CN, AM97C10CN, AH5011CN, AH5012CN, AH5015CN or AH5016CN
See Package 22

Functional and Schematic Diagrams (Additional type on other pages)

MUX Switches (4-Channel Version Shown)

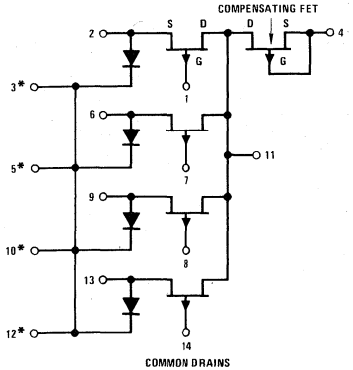


SPST Switches (Quad Version Shown)

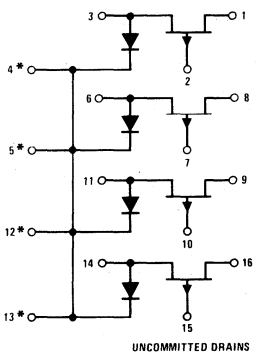


*Note: All diode cathodes are internally connected to the substrate.

MUX Switches (4-Channel Version Shown)



SPST Switches (Quad Version Shown)



Absolute Maximum Ratings

Input Voltage	
AM9709–12CN, AH5009–24CN	30V
AM97C09–12CN	25V
Positive Analog Signal Voltage	30V
Negative Analog Signal Voltage	−15V
Diode Current	10 mA
Drain Current	30 mA
Power Dissipation	500 mW
Operating Temperature Range	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

AM9709, AM97C09, AH5009 (Notes 1 and 2)

PARAMETER		CONDITIONS	5V TTL AM9710CN AM9712CN		5V TTL AH5010–16 (EVEN SERIES)		5V–10V CMOS AM97C10CN AM9712CN		UNITS
			TYP	MAX	TYP	MAX	TYP	MAX	
I_{GSX}	Input Current "OFF"	V_{GD} = 11V, V_{SD} = 0.7V	0.01	2	0.01	0.2			nA
		T_A = 85°C		100		10			nA
I_{GSX}	Input Current "OFF"	V_{GD} = 15V, V_{SD} = 0.7V					0.01	2	nA
		T_A = 85°C						100	nA
$I_{D(OFF)}$	Leakage Current "OFF"	V_{SD} = 0.7V, V_{GS} = 3.8V	0.01	0.2	0.01	0.2			nA
		T_A = 85°C		10		10			nA
$I_{D(OFF)}$	Leakage Current "OFF"	V_{SD} = 0.7V, V_{GS} = 4.3V					0.01	2	nA
		T_A = 85°C						100	nA
$I_{G(ON)}$	Leakage Current "ON"	V_{GD} = 0V, I_S = 1 mA	0.08	1	0.08	1	0.08	1	nA
		T_A = 85°C		200		200		200	nA
$I_{G(ON)}$	Leakage Current "ON"	V_{GD} = 0V, I_S = 2 mA	0.13	5		1000	0.13	5	nA
		T_A = 85°C		10		10		10	μA
$I_{G(ON)}$	Leakage Current "ON"	V_{GD} = 0V, I_S = −2 mA	0.1	10		100	0.10	10	nA
		T_A = 85°C		20		100		20	μA
$r_{DS(ON)}$	Drain-Source Resistance	V_{GS} = 0.35V, I_S = 2 mA	90	150	90	150			Ω
		T_A = +85°C		240		240			Ω
$r_{DS(ON)}$	Drain-Source Resistance	V_{GS} = 0V, I_S = 2 mA					90	150	Ω
		T_A = 85°C						240	Ω
V_{DIODE}	Forward Diode Drop	I_D = 0.5 mA		0.8				0.8	V
$r_{DS(ON)}$	Match	V_{GS} = 0, I_D = 1 mA	4	20		50	4	20	Ω
T_{ON}	Turn "ON" Time	See ac Test Circuit	150	500	150	500	150	500	ns
T_{OFF}	Turn "OFF" Time	See ac Test Circuit	300	500	300	500	300	500	ns
CT	Cross Talk	See ac Test Circuit	120		120		120		dB

Note 1: Test conditions 25°C unless otherwise noted.
Note 2: "OFF" and "ON" notation refers to the conduction state of the FET switch.

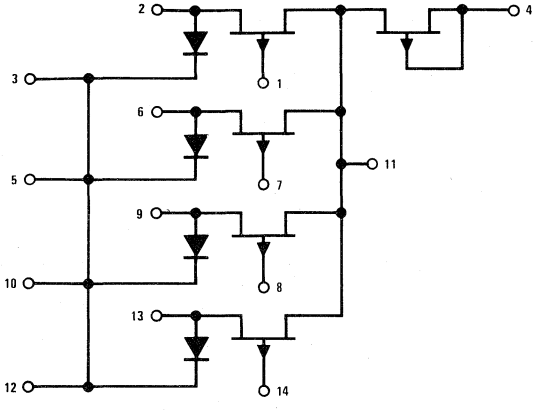
Electrical Characteristics (Continued)

	PARAMETER	CONDITIONS	15V TTL AM9709CN AM9711CN		15V TTL AH5009–15 (ODD SERIES)		10–15V CMOS AM97C09CN AM97C11CN		UNITS
			TYP	MAX	TYP	MAX	TYP	MAX	
I_{GSX}	Input Current "OFF"	V_{GD} = 11V, V_{SD} = 0.7V	0.01	2	0.01	0.2			nA
		T_A = 85°C		100		10			nA
I_{GSX}	Input Current "OFF"	V_{GD} = 15V, V_{SD} = 0.7V					0.01	2	nA
		T_A = 85°C						100	nA
$I_{D(OFF)}$	Leakage Current "OFF"	V_{SD} = 0.7V, V_{GS} = 9.3V					0.01	2	nA
		T_A = 85°C						100	nA
$I_{D(OFF)}$	Leakage Current "OFF"	V_{SD} = 0.7V, V_{GS} = 10.3V	0.01	2	0.01	0.2			nA
		T_A = 85°C		10		10			nA
$I_{G(ON)}$	Leakage Current "ON"	V_{GD} = 0V, I_S = 1 mA	0.04	0.5	0.04	0.5	0.04	0.5	nA
		T_A = 85°C		100		100		100	nA
$I_{G(ON)}$	Leakage Current "ON"	V_{GD} = 0V, I_S = 2 mA	0.07	2		2	0.07	2	nA
		T_A = 85°C		1		2		1	μA
$I_{G(ON)}$	Leakage Current "ON"	V_{GD} = 0V, I_S = −2 mA	0.05	5		100	0.05	5	nA
		T_A = 85°C		2		20		2	μA
$r_{DS(ON)}$	Drain-Source Resistance	V_{GS} = 0V, I_S = 2 mA					60	100	Ω
		T_A = 85°C						160	Ω
$r_{DS(ON)}$	Drain-Source Resistance	V_{GS} = 1.5V, I_S = 2 mA	60	100	60	100			Ω
		T_A = 85°C		160		160			Ω
V_{DIODE}	Forward Diode Drop	I_D = 0.5 mA		0.8				0.8	V
$r_{DS(ON)}$	Match	V_{GS} = 0, I_D = 1 mA	2	10		50	2	10	Ω
T_{ON}	Turn "ON" Time	See ac Test Circuit	150	500	150	500	150	500	ns
T_{OFF}	Turn "OFF" Time	See ac Test Circuit	300	500	300	500	300	500	ns
CT	Cross Talk	See ac Test Circuit	120		120		120		dB

Schematic Diagrams and Pin Connections

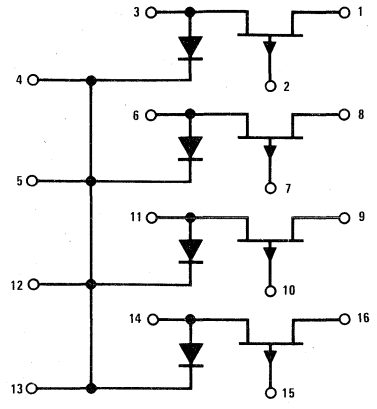
Four Channel

AM97C09CN ($R_{DS(ON)} \leq 100\Omega$, 10–15V CMOS)
AM97C10CN ($R_{DS(ON)} \leq 150\Omega$, 5–10V CMOS)
AM9709CN, AH5009CN ($R_{DS(ON)} \leq 100\Omega$, 15V TTL)
AM9710CN, AH5010CN ($R_{DS(ON)} \leq 150\Omega$, 5V TTL)



14-Pin DIP

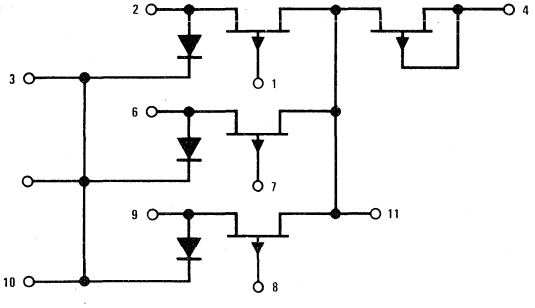
AM97C11CN ($R_{DS(ON)} \leq 100\Omega$, 10–15V CMOS)
AM97C12CN ($R_{DS(ON)} \leq 150\Omega$, 5–10V CMOS)
AM9711CN, AH5011CN ($R_{DS(ON)} \leq 100\Omega$, 15V TTL)
AM9712CN, AH5012CN ($R_{DS(ON)} \leq 150\Omega$, 5V TTL)



16-Pin DIP

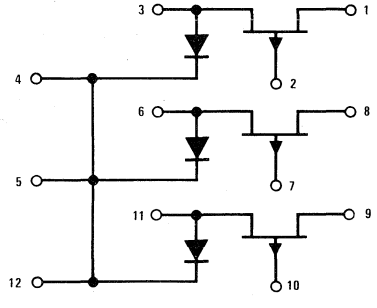
Three-Channel

AH5013CN ($R_{DS(ON)} \leq 100\Omega$, 15V TTL)
AH5014CN ($R_{DS(ON)} \leq 150\Omega$, 5V TTL)



14-Pin DIP

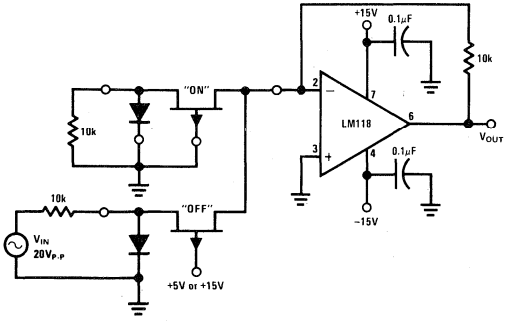
AH5015CN ($R_{DS(ON)} \leq 100\Omega$, 15V TTL)
AH5016CN ($R_{DS(ON)} \leq 150\Omega$, 5V TTL)



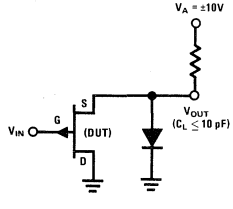
16-Pin DIP

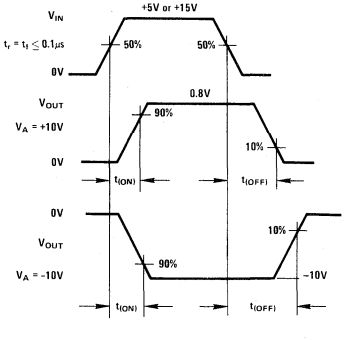
Test Circuits and Switching Time Waveforms

Cross Talk Test Circuit



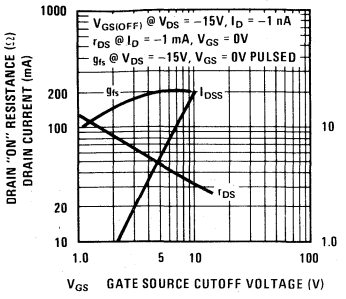
ac Test Circuit



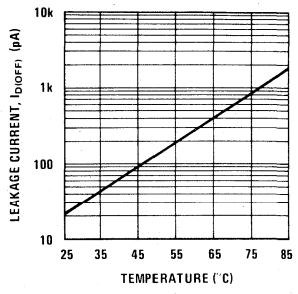


Typical Performance Characteristics

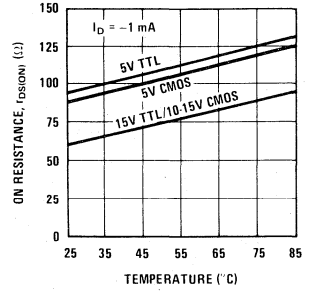
Parameter Interaction



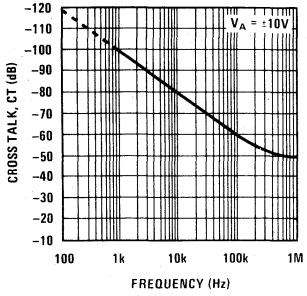
Leakage Current, $I_{D(OFF)}$ vs Temperature



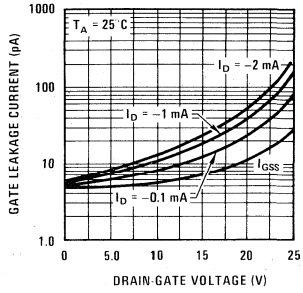
On Resistance, $r_{DS(ON)}$ vs Temperature



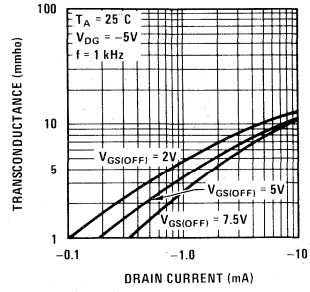
Cross Talk, CT vs Frequency



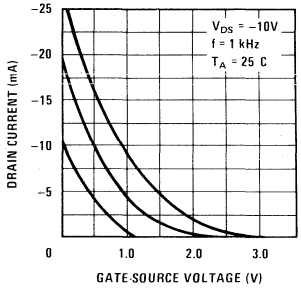
Leakage Current vs Drain-Gate Voltage



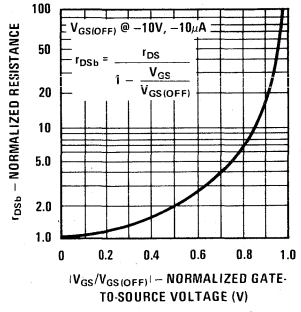
Transconductance vs Drain Current



Drain Current vs Bias Voltage



Normalized Drain Resistance vs Bias Voltage



Applications Information

Theory of Operation

The AM/AH series of analog switches are primarily intended for operation in current mode switch applications; i.e., the drains of the FET switch are held at or near ground by operating into the summing junction of an operational amplifier. Limiting the drain voltage to under a few hundred millivolts eliminates the need for a special gate driver, allowing the switches to be driven directly by standard TTL (AM9710), 5V–10V CMOS (AM97C10), open collector 15V TTL (AM9709), and 10–15V CMOS (AM97C09).

Two basic switch configurations are available: multiple independent switches (N by SPST) and multiple pole switches used for multiplexing (NPST-MUX). The MUX versions such as the AM9709 offer common drains and include a series FET operated at V_{GS} = 0V. The additional FET is placed in feedback path in order to compensate for the "ON" resistance of the switch FET as shown in *Figure 1*.

5

Applications Information (Continued)

The closed-loop gain of *Figure 1* is:

$$A_{VCL} = \frac{R2 + r_{DS(ON)Q2}}{R1 + r_{DS(ON)Q1}}$$

For R1 = R2, gain accuracy is determined by the $r_{DS(ON)}$ match between Q1 and Q2. Typical match between Q1 and Q2 is 4 ohms resulting in a gain accuracy of 0.05% (for R1 = R2 = 10 kΩ).

Noise Immunity

The switches with the source diodes grounded exhibit improved noise immunity for positive analog signals in the "OFF" state. With V_{IN} = 15V and the V_A = 10V, the source of Q1 is clamped to about 0.7V by the diode (V_{GS} = 14.3V) ensuring that ac signals imposed on the 10V will not gate the FET "ON."

Selection of Gain Setting Resistors

Since the AM/AH series of analog switches are operated current mode, it is generally advisable to make the signal current as large as possible. However, current through the FET switch tends to forward bias the source to gate junction and the signal shunting diode resulting in leakage through these junctions. As shown in *Figure 2,* $I_{G(ON)}$ represents a finite error in the current reaching the summing junction of the op amp.

Secondly, the $r_{DS(ON)}$ of the FET begins to "round" as I_S approaches I_{DSS}. A practical rule of thumb is to maintain I_S at less than 1/10 of I_{DSS}.

Combining the criteria from the above discussion yields:

$$R1_{(MIN)} \geq \frac{V_{A(MAX)}\, A_D}{I_{G(ON)}} \qquad (2a)$$

or:

$$\geq \frac{V_{A(MAX)}}{I_{DSS}/10} \qquad (2b)$$

whichever is worse.

Where: $V_{A(MAX)}$ = Peak amplitude of the analog input signal

A_D = Desired accuracy

$I_{G(ON)}$ = Leakage at a given I_S

I_{DSS} = Saturation current of the FET switch

≅ 20 mA

In a typical application, V_A might = ±10V, A_D = 0.1%, 0°C ≤ T_A ≤ 85°C. The criterion of equation (2b) predicts:

$$R1_{(MIN)} \geq \frac{10V}{\frac{20\ mA}{10}} = 5\ k\Omega$$

For R1 = 5k, $I_S \cong$ 10V/5k or 2 mA. The electrical characteristics guarantee an $I_{G(ON)} \leq 1\mu A$ at 85°C for the AM9710. Per the criterion of equation (2a):

$$R1_{(MIN)} \geq \frac{(10V)(10^{-3})}{1 \times 10^{-6}} \geq 10\ k\Omega$$

Since equation (2a) predicts a higher value, the 10k resistor should be used.

The "OFF" condition of the FET also affects gain accuracy. As shown in *Figure 3,* the leakage across Q2, $I_{D(OFF)}$ represents a finite error in the current arriving at the summing junction of the op amp.

Accordingly:

$$R1_{(MAX)} \leq \frac{V_{A(MIN)}\, A_D}{(N)\, I_{D(OFF)}}$$

Where: $V_{A(MIN)}$ = Minimum value for the analog input signal

A_D = Desired accuracy

N = Number of channels

$I_{D(OFF)}$ = "OFF" leakage of a given FET switch

As an example, if N = 10, A_D = 0.1%, and $I_{D(OFF)} \leq$ 10 nA at 85°C for the AM9709, $R1_{(MAX)}$ is:

$$R1_{(MAX)} \leq \frac{(1V)(10^{-3})}{(10)(10 \times 10^{-9})} = 10k$$

Selection of R2, of course, depends on the gain desired and for unity gain R1 = R2.

Lastly, the foregoing discussion has ignored resistor tolerances, input bias current and offset voltage of the op amp—all of which should be considered in setting the overall gain accuracy of the circuit.

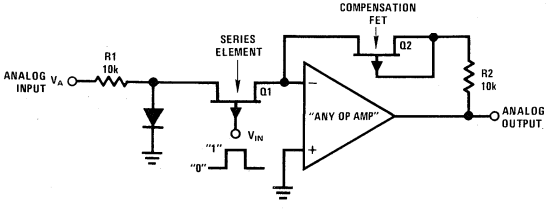


FIGURE 1. Use of Compensation FET

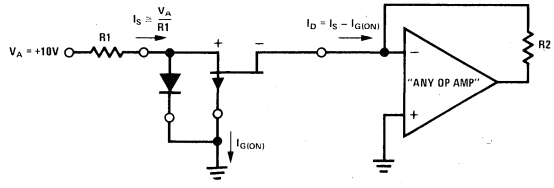


FIGURE 2. On Leakage Current, $I_{G(ON)}$

Applications Information (Continued)

TTL Compatibility

Two input logic drive versions of AM/AH series are available: the even numbered part types are specified to be driven from standard 5V-TTL logic and the odd numbered types from 15V open collector TTL.

Standard TTL gates pull-up to about 3.5V (no load). In order to ensure turn-off of the even numbered switches such as AM9710, a pull-up resistor, R_{EXT}, of at least 10 kΩ should be placed between the 5V V_{CC} and the gate output as shown in *Figure 4.*

Likewise, the open-collector, high voltage TTL outputs should use a pull-up resistor as shown in *Figure 5.* In both cases, $t_{(OFF)}$ is improved for lower values of R_{EXT} and the expense of power dissipation in the low state.

CMOS Compatibility

The cost effective AM97C09 series of switches is optimized for CMOS drive without resistor pull-up. The AM97C10's and AM97C12's are specified for 5V–10V operation while the AM97C09's and AM97C11's are specified for 10V–15V operation.

Definition of Terms

The terms referred to in the electrical characteristics tables are as defined in *Figure 6.*

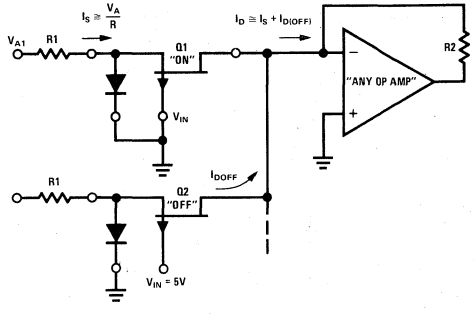


FIGURE 3.

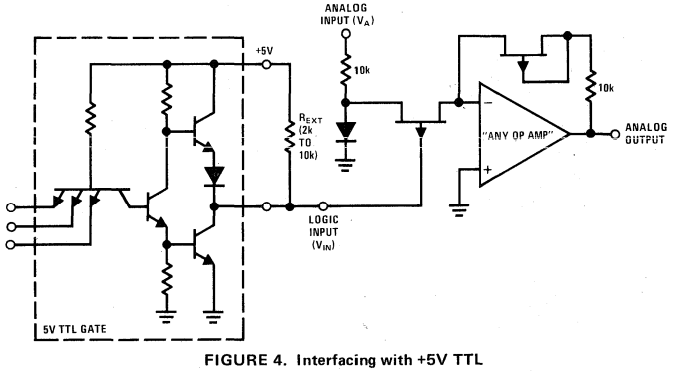


FIGURE 4. Interfacing with +5V TTL

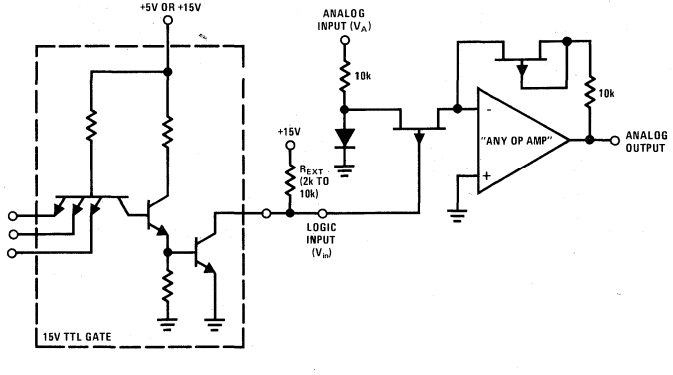


FIGURE 5. Interfacing with +15V Open Collector TTL

Applications Information (Continued)

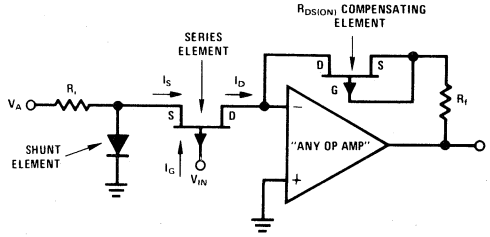
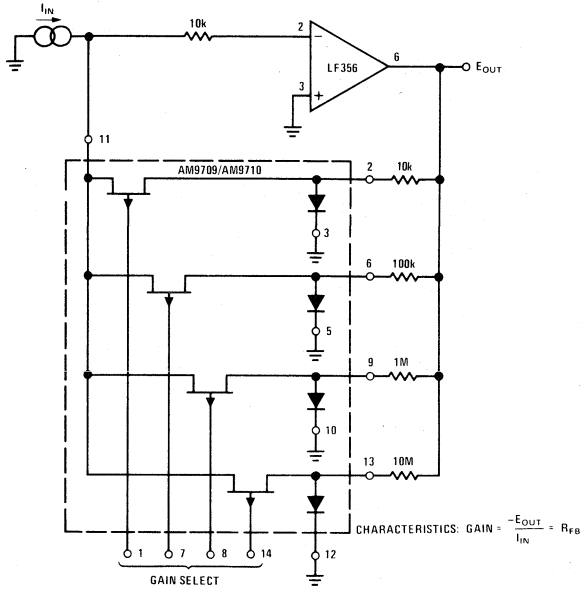


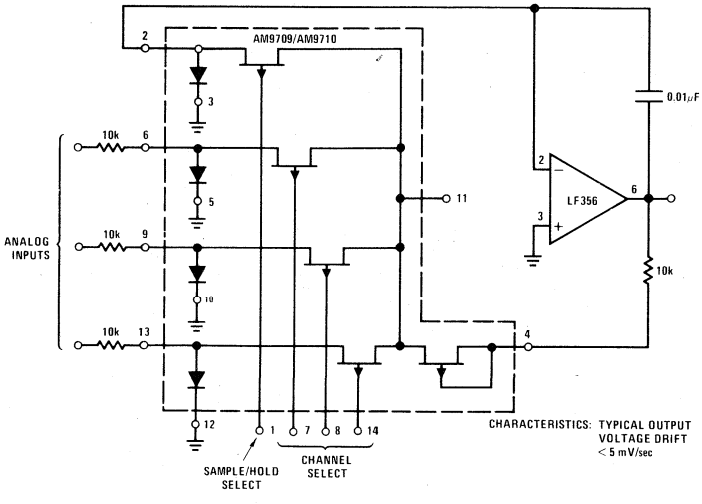
FIGURE 6. Definition of Terms

Typical Applications

Gain Programmable Amplifier

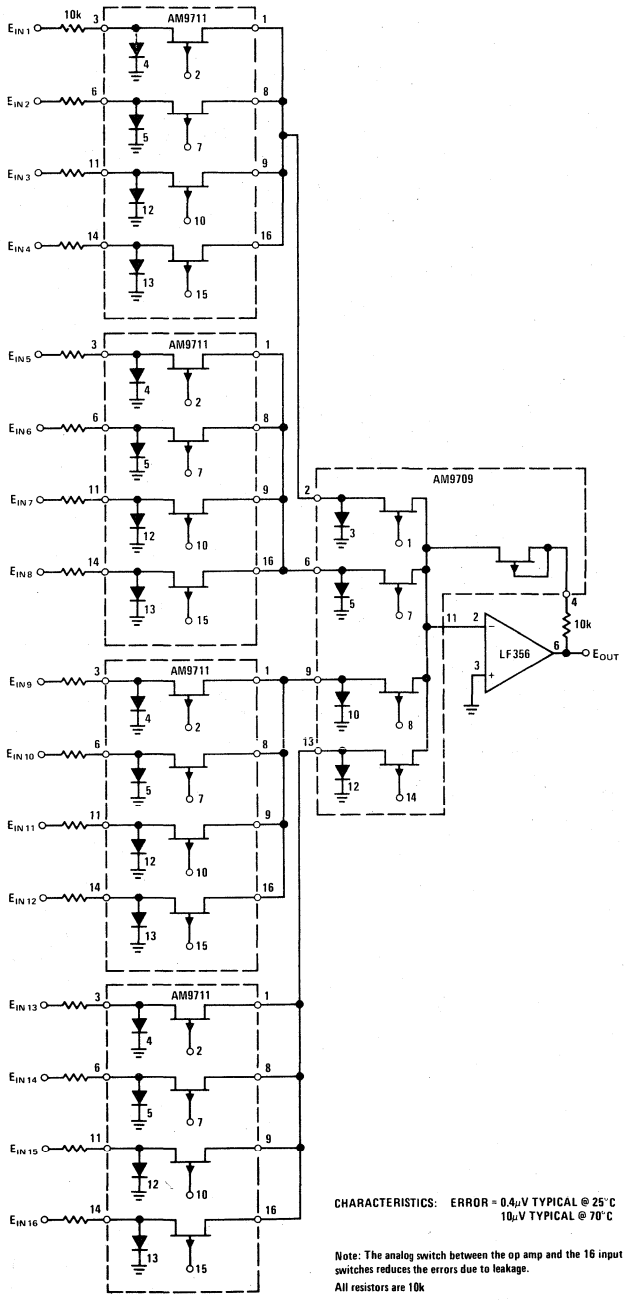


3-Channel Multiplexer with Sample and Hold



Typical Applications (Continued)

16-Channel Multiplexer



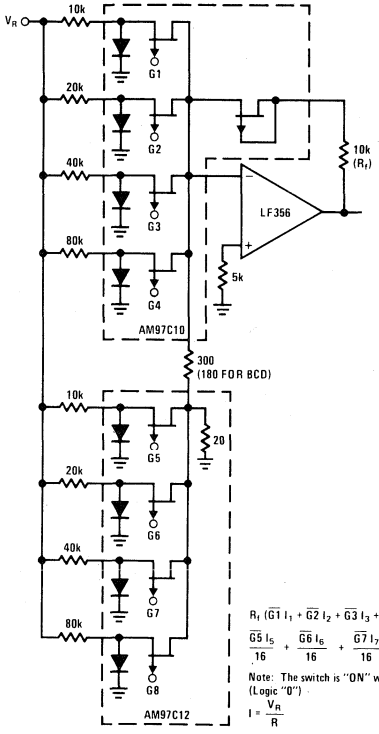
CHARACTERISTICS: ERROR = 0.4μV TYPICAL @ 25°C
10μV TYPICAL @ 70°C

Note: The analog switch between the op amp and the 16 input switches reduces the errors due to leakage.

All resistors are 10k

Typical Applications (Continued)

8-Bit Binary (BCD) Multiplying D/A Converter



$$R_f\left(\overline{G1}\,I_1 + \overline{G2}\,I_2 + \overline{G3}\,I_3 + \overline{G4}\,I_4 + \frac{\overline{G5}\,I_5}{16} + \frac{\overline{G6}\,I_6}{16} + \frac{\overline{G7}\,I_7}{16} + \frac{\overline{G8}\,I_8}{16}\right)$$

Note: The switch is "ON" when G is at 0V (Logic "0")

$$I = \frac{V_R}{R}$$

CD4007M/CD4007C
Dual Complementary Pair Plus Inverter

General Description

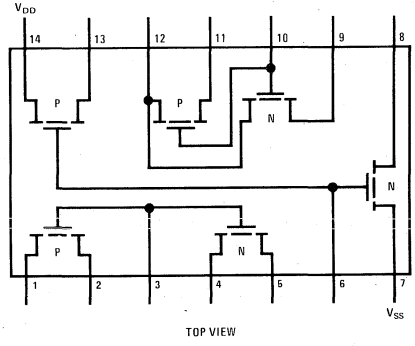
The CD4007M/CD4007C consists of three complementary pairs of N-channel and P-channel enhancement mode MOS transistors suitable for series/shunt applications. All inputs are protected from static discharge by diode clamps to V_{DD} and V_{SS}.

For proper operation the voltages at all pins must be constrained to be between V_{SS} − 0.3V and V_{DD} + 0.3V at all times.

- Wide supply voltage range — 3.0V to 15V
- High noise immunity — 0.45 V_{CC} typ

Connection Diagram

Dual-In-Line and Flat Package



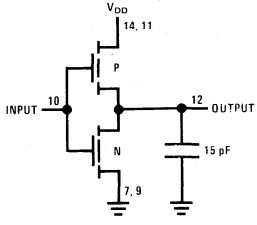
TOP VIEW

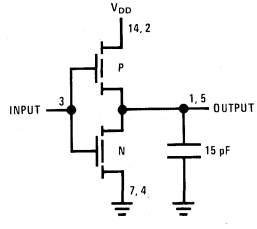
Note: All P-channel substrates are connected to V_{DD}, and all N-channel substrates are connected to V_{SS}.

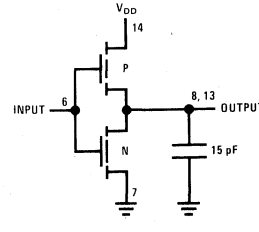
Order Number CD4007MD
See Package 14
Order Number CD4007MF
See Package 23

Order Number CD4007CJ
or CD4007MJ
See Package 18
Order Number CD4007CN
See Package 21

AC Test Circuits







Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	V_{SS} − 0.3V to V_{DD} + 0.3V
Operating Temperature Range	
CD4007M	−55°C to +125°C
CD4007C	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{DD} Range	V_{SS} + 3.0V to V_{SS} + 15V
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics CD4007M

PARAMETER	CONDITIONS	LIMITS									UNITS
		−55°C			25°C			125°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5V			0.05		0.001	0.05			3	μA
	V_{DD} = 10V			0.1		0.001	0.1			6	μA
Quiescent Device Dissipation/Package (P_D)	V_{DD} = 5V			0.25		0.005	0.25			15	μW
	V_{DD} = 10V			1		0.01	1			60	μW
Output Voltage Low Level (V_{OL})	V_{DD} = 5V			0.01		0	0.01			0.05	V
	V_{DD} = 10V			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	V_{DD} = 5V	4.99			4.99	5		4.95			V
	V_{DD} = 10V	9.99			9.99	10		9.95			V
Noise Immunity (V_{NL}) (All Inputs)	V_{DD} = 5V, V_O = 3.6V	1.5			1.5	2.25		1.4			V
	V_{DD} = 10V, V_O = 7.2V	3			3	4.5		2.9			V
Noise Immunity (V_{NH}) (All Inputs)	V_{DD} = 5V, V_O = 0.95V	1.4			1.5	2.25		1.5			V
	V_{DD} = 10V, V_O = 2.9V	2.9			3	4.5		3			V
Output Drive Current N-Channel (I_DN)	V_{DD} = 5V, V_O = 0.4V, V_I = V_{DD}	0.75			0.6	1		0.4			mA
	V_{DD} = 10V, V_O = 0.5V, V_I = V_{DD}	1.6			1.3	2.5		0.95			mA
Output Drive Current P-Channel (I_DP)	V_{DD} = 5V, V_O = 2.5V, V_I = V_{SS}	−1.75			−1.4	−4		−1			mA
	V_{DD} = 10V, V_O = 9.5V, V_I = V_{SS}	−1.35			−1.1	−2.5		−0.75			mA
Input Current (I_I)						10					pA

DC Electrical Characteristics CD4007C

PARAMETER	CONDITIONS	LIMITS									UNITS
		−40°C			25°C			85°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5V			0.5		0.005	0.5			15	μA
	V_{DD} = 10V			1		0.005	1			30	μA
Quiescent Device Dissipation/Package (P_D)	V_{DD} = 5V			2.5		0.025	2.5			75	μW
	V_{DD} = 10V			10		0.05	10			300	μW
Output Voltage Low Level (V_{OL})	V_{DD} = 5V			0.01		0	0.01			0.05	V
	V_{DD} = 10V			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	V_{DD} = 5V	4.99			4.99	5		4.95			V
	V_{DD} = 10V	9.99			9.99	10		9.95			V
Noise Immunity (V_{NL}) (All Inputs)	V_{DD} = 5V, V_O = 3.6V	1.5			1.5	2.25		1.4			V
	V_{DD} = 10V, V_O = 7.2V	3			3	4.5		2.9			V
Noise Immunity (V_{NH}) (All Inputs)	V_{DD} = 5V, V_O = 0.95V	1.4			1.5	2.25		1.5			V
	V_{DD} = 10V, V_O = 2.9V	2.9			3	4.5		3			V
Output Drive Current N-Channel (I_DN)	V_{DD} = 5V, V_O = 0.4V, V_I = V_{DD}	0.35			0.3	1		0.24			mA
	V_{DD} = 10V, V_O = 0.5V, V_I = V_{DD}	1.2			1	2.5		0.8			mA
Output Drive Current P-Channel (I_DP)	V_{DD} = 5V, V_O = 2.5V, V_I = V_{SS}	−1.3			−1.1	−4		−0.9			mA
	V_{DD} = 10V, V_O = 9.5V, V_I = V_{SS}	−0.65			−0.55	−2.5		−0.45			mA
Input Current (I_I)						10					pA

Note 1: This device should not be connected to circuits with the power on because high transient voltages may cause permanent damage.

AC Electrical Characteristics CD4007M

T_A = 25°C and C_L = 15 pF and input rise and fall times = 20 ns. Typical temperature coefficient for all values of V_{DD} = 0.3%/°C.

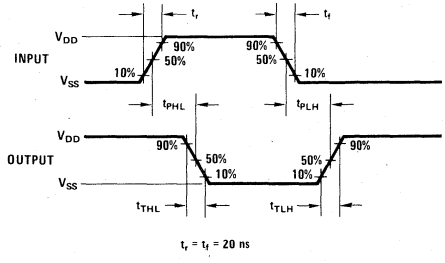
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time ($t_{PLH} = t_{PHL}$)	V_{DD} = 5V		35	60	ns
	V_{DD} = 10V		20	40	ns
Transition Time ($t_{TLH} = t_{THL}$)	V_{DD} = 5V		50	75	ns
	V_{DD} = 10V		30	40	ns
Input Capacitance (C_I)	Any Input		5		pF

AC Electrical Characteristics CD4007C

T_A = 25°C and C_L = 15 pF and input rise and fall times = 20 ns. Typical temperature coefficient for all values of V_{DD} = 0.3%/°C.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time ($t_{PLH} = t_{PHL}$)	V_{DD} = 5V		35	75	ns
	V_{DD} = 10V		20	50	ns
Transition Time ($t_{TLH} = t_{THL}$)	V_{DD} = 5V		50	100	ns
	V_{DD} = 10V		30	50	ns
Input Capacitance (C_I)	Any Input		5		pF

Switching Time Waveforms



$t_r = t_f$ = 20 ns

CD4016M/CD4016C Quad Bilateral Switch

General Description

The CD4016M/CD4016C is a quad bilateral switch which utilizes P-channel and N-channel complementary MOS (CMOS) circuits to provide an extremely high "OFF" resistance and low "ON" resistance switch. The switch will pass signals in either direction and is extremely useful in digital switching.

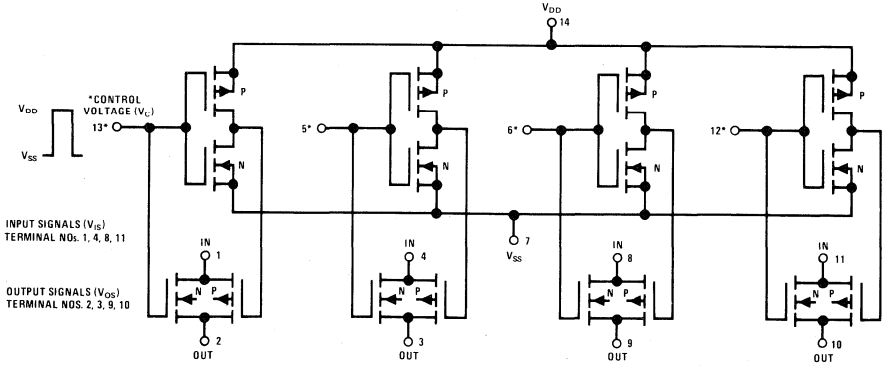
Features

■ Wide supply voltage range	3V to 15V
■ High noise immunity	0.45 V_{CC} typ.
■ Wide range of digital and analog levels	±7.5 V_{PEAK}
■ Low "ON" resistance	300Ω typ. $V_{DD} - V_{SS} = 15V$
■ Matched switch characteristics	$\Delta R_{ON} = 40\Omega$ typ.
■ High "ON/OFF" output voltage ratio	65 dB typ. @ $f_{is} = 10$ kHz $R_L = 10k$
■ High degree of linearity	.5% distortion typ. @ $f_{is} = 1$ kHz
■ Extremely low leakage	$V_{is} = 5\ V_{p-p}$ $V_{DD} - V_{SS} = 10V$ $R_L = 10\ k\Omega$
■ Transmits frequencies up to 10 MHz	

Applications

- Analog signal switching/multiplexing
  - Signal gating
  - Squelch control
  - Chopper
  - Modulator
  - Demodulator
  - Commutating switch
- Digital signal switching/multiplexing
- CMOS logic implementation
- Analog to digital/digital to analog conversion
- Digital control of frequency, impedance, phase, and analog-signal gain

Schematic and Connection Diagrams

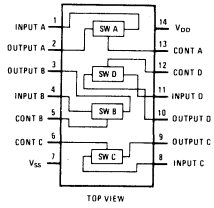


Note 1: All switch P-channel substrates are internally connected to terminal No. 14.
Note 2: All switch N-channel substrates are internally connected to terminal No. 7.

Signal-level range: $V_{SS} < V_{is} > V_{DD}$

Normal operation: Control-line biasing, switch ON V_C "1" = V_{DD}, switch OFF V_C "0" = V_{SS}

Dual-In-Line and Flat Package



Order Number CD4016MD
See Package 14
Order Number CD4016MF
See Package 23
Order Number CD4016CJ or CD4016MJ
See Package 18
Order Number CD4016CN
See Package 21

Absolute Maximum Ratings

Voltage at Any Pin (Note 1) V_{SS} −0.3V to V_{SS} +15.5V
Operating Temperature Range CD4016M −55°C to +125°C
CD4016C −40°C to +85°C
Storage Temperature Range −65°C to +150°C
Package Dissipation 500 mW
Lead Temperature (Soldering, 10 sec) 300°C
Operating V_{DD} Range V_{SS} +3V to V_{SS} +15V

Electrical Characteristics CD4016M

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS −55°C MIN	−55°C TYP	−55°C MAX	25°C MIN	25°C TYP	25°C MAX	125°C MIN	125°C TYP	125°C MAX	UNITS
Quiescent Dissipation per Package		TERMINALS: V_{DD} 14 (+10); V_{SS} 7 (GND); V_C 5, 6, 12, 13 (GND); V_{is} 1, 4, 8, 11 (≤ +10); V_{os} 2, 3, 9, 10 (≤ +10)										
All Switches "OFF"	P_T				5		0.1	5			300	μW
All Switches "ON"	P_T	TERMINALS: V_{DD} 14 (+10); V_{SS} 7 (GND); V_C 5, 6, 12, 13 (+10); $V_{is} = V_{OS}$ 1-4, 8-11 (≤ +10)			5		0.1	5			300	μW
Threshold Voltage N-Channel	$V_{TH}N$	I_{DS} = 10 μA, V_{DD} = 5V, 10V, or 15V		1.7			1.5			1.3		V
P-Channel	$V_{TH}P$	I_{DS} = −10 μA, V_{DD} = 5V, 10V, or 15V		−1.7			−1.5			−1.3		V
SIGNAL INPUTS (V_{is}) AND OUTPUTS (V_{os})												
"ON" Resistance	R_{ON}	R_L = 10kΩ; $V_C = V_{DD}$, V_{SS}, V_{is}: +7.5V, −7.5V, −7.5V		120	360		200	400		300	600	Ω
		+7.5V, −7.5V, ±0.25V		130	775		280	850		470	1230	
		+7.5V, −7.5V, +5V		130	600		250	660		400	960	
		+5V, −5V, −5V		130	600		250	660		400	960	Ω
		+5V, −5V, ±0.25V		325	1870		580	2000		900	2600	
		+15V, 0V, +15V		120	360		200	400		300	600	
		+15V, 0V, +0.25V		120	360		200	400		300	600	Ω
		+15V, 0V, 9.3V		150	775		300	850		490	1230	
		+10V, 0V, +10V		130	600		250	660		400	960	
		+10V, 0V, +0.25V		130	600		250	660		400	960	Ω
		+10V, 0V, 5.6V		300	1870		560	2000		880	2600	
Δ "ON" Resistance Between Any 2 of 4 Switches	ΔR_{ON}	+7.5V, −7.5V, ±7.5V					10					Ω
		+5V, −5V, ±5V					15					
Sine Wave Response (Distortion)		R_L = 10 kΩ, f_{is} = 1 kHz; +5V, −5V, 5V(p-p) (Note 3)					0.4					%
Input or Output Leakage—Switch "OFF"		V_{DD} +7.5V, $V_C = V_{SS}$ −7.5V, V_{is} +7.5V / −7.5V					±100 / ±100					pA
(Effective "OFF" Resistance)		V_{DD} +5V, V_C −5V, V_{is} +5V / −5V					(Note 2) 125 / (Note 2) 125					nA
Frequency Response—Switch "ON" (Sine Wave Input)		$V_C = V_{DD}$ = +5V, V_{SS} = −5V; R_L = 1 kΩ, V_{is} = 5V(p-p); $20 \log_{10} \frac{V_{os}}{V_{is}}$ = −3 dB					40					MHz
Feedthrough Switch "OFF"		V_{DD} = +5V, $V_C = V_{SS}$ = −5V; $20 \log_{10} \frac{V_{os}}{V_{is}}$ = −50 dB					1.25					MHz
Crosstalk Between any 2 of the 4 switches (Frequency at −50 dB)		$V_C(A) = V_{DD}$ = +5V, $V_C(B) = V_{SS}$ = −5V; R_L = 1 kΩ, $V_{is}(A)$ = 5V(p-p); $20 \log_{10} \frac{V_{os}(B)}{V_{is}(A)}$ = −50 dB					0.9					MHz
Capacitance Input	C_{IS}	V_{DD} = +5V, $V_C = V_{SS}$ = −5V					4					pF
Output	C_{OS}						4					
Feedthrough	C_{IOS}						0.2					
Propagation Delay Signal Input to Signal Output	t_{pd}	$V_C = V_{DD}$ = +10V, V_{SS} = GND, C_L = 15 pF; V_{is} = 10V (square wave); $t_r = t_f$ = 20 ns (input signal)					10					ns
CONTROL (V_C)												
Switch Threshold Voltage	$V_{TH}C$	$V_{is} \leq V_{DD}$; $V_{DD} - V_{SS}$ = 15V, 10V, 5V; I_{IS} = 10 μA	0.7		2.9	0.5	1.5	2.7	0.2		2.4	V
Input Current	I_C	$V_{DD} - V_{SS}$ = 10V; $V_C \leq V_{DD} - V_{SS}$					±10					pA
Average Input Capacitance	C_C						5					pF
Crosstalk — Control Input to Signal Output		$V_{DD} - V_{SS}$ = 10V, V_C = 10V (square wave); R_L = 10 kΩ					50					mV
Turn "ON" Propagation Delay	$t_{pd}C$	$t_{rc} = t_{fc}$ = 20 ns; $V_{is} \leq$ 10V, C_L = 15 pF					20					ns
Maximum Allowable Control Input Repetition Rate		V_{DD} = 10V, V_{SS} = GND, R_L = 1 kΩ, C_L = 15 pF, V_C = 10V (square wave), $t_r = t_f$ = 20 ns					10					MHz

Note 1: The device should not be connected to circuits with the power on.
Note 2: ±10 x 10^{-3}.
Note 3: Symmetrical about 0V.

Electrical Characteristics CD4016C

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS –40°C MIN	–40°C TYP	–40°C MAX	25°C MIN	25°C TYP	25°C MAX	85°C MIN	85°C TYP	85°C MAX	UNITS
Quiescent Dissipation per Package		VOLTS APPLIED: V_{DD} = 14 = +10; V_{SS} = 7 = GND; V_C = 5, 6, 12, 13 = GND; V_{is} = 1, 4, 8, 11 = ≤ +10; V_{os} = 2, 3, 9, 10 = ≤ +10										
All Switches "OFF"	P_T				5		0.1	5			80	μW
		VOLTS APPLIED: V_{DD} = 14 = +10; V_{SS} = 7 = GND; V_C = 5, 6, 12, 13 = +10; $V_{is} = V_{OS}$ = 1-4, 8-11 = ≤ +10										
All Switches "ON"					5		0.1	5			80	μW
Threshold Voltage N-Channel	$V_{TH}N$	I_{DS} = 10 μA, V_{DD} = 5V, 10V, or 15V		1.7			1.5			1.3		V
P-Channel	$V_{TH}P$	I_{DS} = 10 μA, V_{DD} = 5V, 10V, or 15V		–1.7			–1.5			–1.3		V
SIGNAL INPUTS (V_{is}) AND OUTPUTS (V_{os})												
"ON" Resistance	R_{ON}	R_L = 10kΩ; $V_C = V_{DD}$, V_{SS}, V_{is}: +7.5V		130	370		200	400		260	520	
		+7.5V, –7.5V, –7.5V		130	370		200	400		260	520	Ω
		±0.25V		160	790		280	850		400	1080	
		+5V		150	610		250	660		340	840	
		+5V, –5V, –5V		150	610		250	660		340	840	Ω
		±0.25V		370	1900		580	2000		770	2380	
		+15V		130	370		200	400		260	520	
		+15V, 0V, +0.25V		130	370		200	400		260	520	Ω
		9.3V		180	790		300	850		400	1080	
		+10V		150	610		250	660		340	840	
		+10V, 0V, +0.25V		150	610		250	660		340	840	Ω
		5.6V		350	1900		560	2000		750	2380	
Δ "ON" Resistance Between Any 2 of 4 Switches	ΔR_{ON}	+7.5V, –7.5V, ±7.5V					10					Ω
		+5V, –5V, ±5V					15					
Sine Wave Response (Distortion)		R_L = 10 kΩ, f_{is} = 1 kHz; +5V, –5V, 5V(p-p) (Note 3)					0.4					%
Input or Output Leakage–Switch "OFF" (Effective "OFF" Resistance)		V_{DD} = +7.5V, $V_C = V_{SS}$ = –7.5V, V_{is} = +7.5V, –7.5V					±100					pA
		V_{DD} = +5V, $V_C = V_{SS}$ = –5V, V_{is} = +5V, –5V					±100 (Note 2)	125				nA
							(Note 2)	125				
Frequency Response–Switch "ON" (Sine Wave Input)		$V_C = V_{DD}$ = +5V, V_{SS} = –5V; R_L = 1 kΩ, V_{is} = 5V(p-p); $20 \log_{10} \frac{V_{os}}{V_{is}} = -3$ dB					40					MHz
Feedthrough Switch "OFF"		V_{DD} = +5V, $V_C = V_{SS}$ = –5V; $20 \log_{10} \frac{V_{os}}{V_{is}} = -50$ dB					1.25					MHz
Crosstalk Between any 2 of the 4 switches (Frequency at –50 dB)		R_L = 1 kΩ, $V_{is}(A)$ = 5V(p-p); $V_C(A) = V_{DD}$ = +5V, $V_C(B) = V_{SS}$ = –5V; $20 \log_{10} \frac{V_{os}(B)}{V_{is}(A)} = -50$ dB					0.9					MHz
Capacitance Input	C_{IS}	V_{DD} = +5V, $V_C = V_{SS}$ = –5V					4					
Output	C_{OS}						4					pF
Feedthrough	C_{IOS}						0.2					
Propagation Delay Signal Input to Signal Output	t_{pd}	$V_C = V_{DD}$ = +10V, V_{SS} = GND, C_L = 15 pF, V_{is} = 10V (square wave), $t_r = t_f$ = 20 ns (input signal)					10					ns
CONTROL (V_C)												
Switch Threshold Voltage	$V_{TH}C$	$V_{is} \leq V_{DD}$; $V_{DD} - V_{SS}$ = 15V, 10V, 5V; I_{IS} = 10 μA				0.5	1.5	2.7				V
Input Current	I_C	$V_{DD} - V_{SS}$ = 10V, $V_C \leq V_{DD} - V_{SS}$					±10					pA
Average Input Capacitance	C_C						5					pF
Crosstalk – Control Input to Signal Output		$V_{DD} - V_{SS}$ = 10V, V_C = 10V (square wave), R_L = 10 kΩ					50					mV
Turn "ON" Propagation Delay	$t_{pd}C$	$t_{rc} = t_{fc}$ = 20 ns, $V_{is} \leq$ 10V, C_L = 15 pF					20					ns
Maximum Allowable Control Input Repetition Rate		V_{DD} = 10V, V_{SS} = GND, R_L = 1 kΩ, C_L = 15 pF, V_C = 10V (square wave), $t_r = t_f$ = 20 ns					10					MHz

Note 1: The device should not be connected to circuits with the power on.

Note 2: $\pm 10 \times 10^{-3}$.

Note 3: Symmetrical about 0V.

Typical ON Resistance Characteristics

CHARACTERISTIC*	SUPPLY CONDITIONS		LOAD CONDITIONS					
			R_L = 1 kΩ		R_L = 10 kΩ		R_L = 100 kΩ	
	V_{DD} (V)	V_{SS} (V)	VALUE (Ω)	V_{is} (V)	VALUE (Ω)	V_{is} (V)	VALUE (Ω)	V_{is} (V)
R_{ON}	+15	0	200	+15	200	+15	180	+15
			200	0	200	0	200	0
R_{ON} (max.)	+15	0	300	+11	300	+9.3	320	+9.2
R_{ON}	+10	0	290	+10	250	+10	240	+10
			290	0	250	0	300	0
R_{ON} (max.)	+10	0	500	+7.4	560	+5.6	610	+5.5
R_{ON}	+5	0	860	+5	470	+5	450	+5
			600	0	580	0	800	0
R_{ON} (max.)	+5	0	1.7k	+4.2	7k	+2.9	33k	+2.7
R_{ON}	+7.5	−7.5	200	+7.5	200	+7.5	180	+7.5
			200	−7.5	200	−7.5	180	−7.5
R_{ON} (max.)	+7.5	−7.5	290	±0.25	280	±25	400	±0.25
R_{ON}	+5	−5	260	+5	250	+5	240	+5
			310	−5	250	−5	240	−5
R_{ON} (max.)	+5	−5	600	±0.25	580	±0.25	760	±0.25
R_{ON}	+2.5	−2.5	590	+2.5	450	+2.5	490	+2.5
			720	−2.5	520	−2.5	520	−2.5
R_{ON} (max.)	+2.5	−2.5	232k	±0.25	300k	±0.25	870k	±0.25

*Variation from a perfect switch: R_{ON} = 0Ω.

CD4051M/CD4051C
Single 8-Channel Analog Multiplexer/Demultiplexer
CD4052M/CD4052C
Dual 4-Channel Analog Multiplexer/Demultiplexer
CD4053M/CD4053C
Triple 2-Channel Analog Multiplexer/Demultiplexer

General Description

These analog multiplexers/demultiplexers are digitally controlled analog switches having low "ON" impedance and very low "OFF" leakage currents. Control of analog signals up to 15 Vp-p can be achieved by digital signal amplitudes of 3–15V. For example, if V_{DD} = 5V, V_{SS} = 0V and V_{EE} = −5V, analog signals from −5V–+5V can be controlled by digital inputs of 0–5V. The multiplexer circuits dissipate, extremely low quiescent power over the full $V_{DD} - V_{SS}$ and $V_{DD} - V_{EE}$ supply-voltage ranges, independent of the logic state of the control signals. When a logical "1" is present at the inhibit input terminal all channels are "OFF."

CD4051M/CD4051C is a single 8-channel multiplexer having three binary control inputs, A, B and C, and an inhibit input. The three binary signals select 1 of 8 channels to be turned "ON" and connect the input to the output.

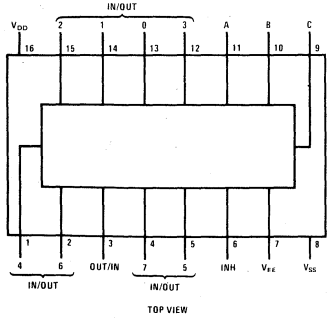
CD4052M/CD4052C is a differential 4-channel multiplexer having two binary control inputs, A and B, and an inhibit input. The two binary input signals select 1 of 4 pairs of channels to be turned on and connect the differential analog inputs to the differential outputs.

CD4053M/CD4053C is a triple 2-channel multiplexer having three separate digital control inputs, A, B and C and an inhibit input. Each control input selects one of a pair of channels which are connected in a single-pole double-throw configuration.

Features

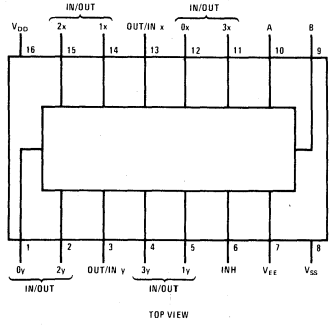
- Wide range of digital and analog signal levels: digital 3–15V, analog to 15 Vp-p
- Low "ON" resistance: 80Ω (typ) over entire 15 Vp-p signal-input range for $V_{DD} - V_{EE}$ = 15V
- High "OFF" resistance: input leakage ±10 pA (typ) at $V_{DD} - V_{EE}$ = 10V
- Logic level conversion for digital addressing signals of 3–15V ($V_{DD} - V_{SS}$ = 3–15V) to switch analog signals to 15 Vp-p ($V_{DD} - V_{EE}$ = 15V)
- Matched switch characteristics: ΔR_{ON} = 5Ω (typ) for $V_{DD} - V_{EE}$ = 15V
- Very low quiescent power dissipation under all digital-control input and supply conditions: 1μW typ at $V_{DD} - V_{SS} = V_{DD} - V_{EE}$ = 10V
- Binary address decoding on chip

Connection Diagrams (Dual-In-Line and Flat Packages)



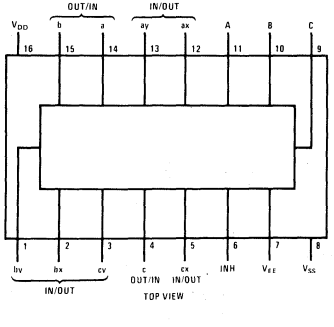
TOP VIEW

Order Number CD4051MD
See Package 15
Order Number CD4051MF
See Package 24
Order Number CD4051CJ or CD4051MJ
See Package 19
Order Number CD4051CN
See Package 22



TOP VIEW

Order Number CD4052MD
See Package 15
Order Number CD4052MF
See Package 24
Order Number CD4052CJ or CD4052MJ
See Package 19
Order Number CD4052CN
See Package 22



TOP VIEW

Order Number CD4053MD
See Package 15
Order Number CD4053MF
See Package 24
Order Number CD4053CJ or CE4053MJ
See Package 19
Order Number CD4053CN
See Package 22

Absolute Maximum Ratings

Voltage at Any Control Input	V_{SS} − 0.3V to V_{DD} + 0.3V
Voltage at Any Switch Input or Output	V_{EE} − 0.3V to V_{DD} + 0.3V
Operating Temperature Range	
CD40XXM	−55°C to +125°C
CD40XXC	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{DD} Range	V_{EE} + 3V to V_{EE} + 15V
	V_{SS} + 3V to V_{SS} + 15V

Electrical Characteristics CD4051M, CD4052M, CD4053M

	PARAMETER	CONDITIONS			−55°C MIN	−55°C TYP	−55°C MAX	25°C MIN	25°C TYP	25°C MAX	125°C MIN	125°C TYP	125°C MAX	UNITS
P_D	Quiescent Dissipation Per Package	V_{DD} = 10V, V_{EE} = V_{SS} = 0V					100		1	100			6000	μW
R_{ON}	"ON" Resistance (Peak for $V_{SS} \leq V_{IS} \leq V_{DD}$)	R_L = 10 kΩ, V_{SS} = 0, (Any Channel Selected)	V_{DD} = 7.5V, V_{EE} = −7.5V, or V_{DD} = 15V, V_{EE} = 0V			60	220		80	280		145	320	Ω
			V_{DD} = 5V, V_{EE} = −5V, or V_{DD} = 10V, V_{EE} = 0V			85	400		120	400		190	550	Ω
			V_{DD} = 2.5V, V_{EE} = −2.5V, or V_{DD} = 5V, V_{EE} = 0V			210	3000		270	2500		360	5500	Ω
ΔR_{ON}	Δ"ON" Resistance Between Any Two Channels	R_L = 10 kΩ, V_{SS} = 0, (Any Channel Selected)	V_{DD} = 7.5V, V_{EE} = −7.5V, or V_{DD} = 15V, V_{EE} = 0V						5					Ω
			V_{DD} = 5V, V_{EE} = −5V, or V_{DD} = 10V, V_{EE} = 0V						10					Ω
	Sine Wave Response (Distortion)	R_L = 10 kΩ, V_{SS} = 0, f_{IS} = 1 kHz	V_{DD} = 7.5V, V_{EE} = −7.5V						0.1					%
			V_{DD} = 5V, V_{EE} = −5V						0.2					%
			V_{DD} = 2.5V, V_{EE} = −2.5V						1					%
	"OFF" Channel Leakage Current Any Channel "OFF"	V_{SS} = 0V; OUT/IN = ±7.5V, IN/OUT = 0V	V_{DD} = 7.5V, V_{EE} = −7.5V				±50		±0.01	±50			±500	nA
	All Channels "OFF" (Common OUT/IN)	Inhibit = 5V, V_{SS} = 0V, OUT/IN = 0V, IN/OUT = ±7.5V	V_{DD} = 7.5V, V_{EE} = −7.5V	CD4051M			±400		±0.08	±400			±4000	nA
				CD4052M			±200		±0.04	±200			±2000	nA
				CD4053M			±100		±0.02	±100			±1000	nA
	Frequency Response Channel "ON" (Sine Wave Input)	R_L = 1 kΩ, V_{IS} = 5V (p-p), V_{SS} = 0V	V_{DD} = 5V, V_{EE} = −5V, 20 $\log_{10} V_{OS}/V_{IS}$ = −3 dB						40					MHz
	Feedthrough Channel "OFF"	R_L = 1 kΩ, V_{IS} = 5V (p-p), V_{SS} = 0V	V_{DD} = 5V, V_{EE} = −5V, 20 $\log_{10} V_{OS}/V_{IS}$ = −40 dB						1					MHz
	Crosstalk Between Any Two Channels (Frequency at 40 dB)	R_L = 1 kΩ, $V_{IS}(A)$ = 5V (p-p), V_{SS} = 0V	V_{DD} = 5V, V_{EE} = −5V, 20 $\log_{10} V_{OS}(B)/V_{IS}(A)$ = −40 dB (Note 1)						1					MHz
C_{IS}	Capacitance Input (IN/OUT)	V_{DD} = V_{EE} = V_{SS} = 0V							10					pF
C_{OS}	Output (Common OUT/IN)			CD4051M					60					pF
				CD4052M					30					pF
				CD4053M					20					pF
C_{IOS}	Feedthrough								0.2					pF
t_{PLH}, t_{PHL}	Propagation Delay Signal Input to Signal Output	V_{DD} = 10V, V_{SS} = V_{EE} = Inhibit = 0V, C_L = 15 pF, V_{IS} = 10V (Square Wave), t_r, t_f = 20 ns (Input Signal)							10					ns

Electrical Characteristics (Continued) CD4051M, CD4052M, CD4053M

PARAMETER		CONDITIONS		−55°C			25°C			125°C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
CONTROL INPUTS A, B, C AND INHIBIT													
	Noise Immunity (Any Control Input)												
V_{NL}		$V_{IS} = V_{DD}$ through 1 kΩ, $V_{EE} = V_{SS}$ $I_{IS} = 10\mu A$ $R_L = 1k\Omega$ to V_{EE}	$V_{DD} - V_{SS} = 10V$	3.0			3.0	4.5		2.9			V
			$V_{DD} - V_{SS} = 5V$	1.5			1.5	2.25		1.4			V
V_{NH}			$V_{DD} - V_{SS} = 10V$	2.9			3.0	4.5		3.0			V
			$V_{DD} - V_{SS} = 5V$	1.4			1.5	2.25		1.5			V
C_I	Average Input Capacitance							5					pF
t_{PHL}, t_{PLH}	Turn "ON" Propagation Delay Control Input-to-Signal Output	$C_L = 15$ pF, $R_L = 10$ kΩ, $V_{IS} \leq V_{DD}$, $t_r, t_f = 20$ ns, V_{SS} = Inhibit = 0V, (Note 2)	$V_{DD} = 10V$, $V_{EE} = 0V$					150	300				ns
			$V_{DD} = 5V$, $V_{EE} = 0V$					400	800				ns
			$V_{DD} = 5V$, $V_{EE} = -5V$					200	400				ns
	Inhibit Input-to-Signal Output	$C_L = 15$ pF, $R_L = 10$ kΩ, $V_{IS} = V_{DD}$ $t_r, t_f = 20$ ns	$V_{DD} = 10V$, $V_{EE} = 0V$					200	400				ns
			$V_{DD} = 5V$ $V_{EE} = 0V$					550	1100				ns
	Inhibit Recovery Time	$V_{DD} = 10V$						200	400				ns

Electrical Characteristics CD4051C, CD4052C, CD4053C

PARAMETER		CONDITIONS			−40°C			25°C			85°C			UNITS
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
P_D	Quiescent Dissipation Per Package	$V_{DD} = 10V$, $V_{EE} = V_{SS} = 0V$					1000		1	1000			6000	μW
R_{ON}	"ON" Resistance (Peak for $V_{SS} \leq V_{IS} \leq V_{DD}$)	$R_L = 10$ kΩ, $V_{SS} = 0$, (Any Channel Selected)	$V_{DD} = 7.5V$, $V_{EE} = -7.5V$, or $V_{DD} = 15V$, $V_{EE} = 0V$			80	250		80	280		130	300	Ω
			$V_{DD} = 5V$, $V_{EE} = -5V$, or $V_{DD} = 10V$, $V_{EE} = 0V$			100	450		120	400		170	520	Ω
			$V_{DD} = 2.5V$, $V_{EE} = -2.5V$, or $V_{DD} = 5V$, $V_{EE} = 0V$			230	3500		270	2500		330	5200	Ω
ΔR_{ON}	Δ"ON" Resistance Between Any Two Channels	$R_L = 10$ kΩ, $V_{SS} = 0$, (Any Channel Selected)	$V_{DD} = 7.5V$, $V_{EE} = -7.5V$, or $V_{DD} = 15V$, $V_{EE} = 0V$						5					Ω
			$V_{DD} = 5V$, $V_{EE} = -5V$, or $V_{DD} = 10V$, $V_{EE} = 0V$						10					Ω
	Sine Wave Response (Distortion)	$R_L = 10$ kΩ, $V_{SS} = 0$, $f_{IS} = 1$ kHz	$V_{DD} = 7.5V$, $V_{EE} = -7.5V$						0.1					%
			$V_{DD} = 5V$, $V_{EE} = -5V$						0.2					%
			$V_{DD} = 2.5V$, $V_{EE} = -2.5V$						1					%
	"OFF" Channel Leakage Current Any Channel "OFF"	$V_{SS} = 0V$ OUT/IN = ±7.5V, IN/OUT = 0V	$V_{DD} = 7.5V$ $V_{EE} = -7.5V$				±50		±0.01	±50			±200	nA
	All Channels "OFF" (Common OUT/IN)	Inhibit = 5V, $V_{SS} = 0V$	$V_{DD} = 7.5V$, $V_{EE} = -7.5V$	CD4051C			±1600		±0.08	±400			±1600	nA
		OUT/IN = 0V, IN/OUT = ±7.5V		CD4052C			±800		±0.04	±200			±800	nA
				CD4053C			±400		±0.02	±100			±400	nA
	Frequency Response Channel "ON" (Sine Wave Input)	$R_L = 1$ kΩ, $V_{IS} = 5V$ (p-p), $V_{SS} = 0V$	$V_{DD} = 5V$, $V_{EE} = -5V$, $20 \log_{10} V_{OS}/V_{IS} = -3$ dB						40					MHz

Electrical Characteristics (Continued) CD4051C, CD4052C, CD4053C

PARAMETER		CONDITIONS		−40°C			25°C			85°C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
	Feedthrough Channel "OFF"	R_L = 1 kΩ, V_{IS} = 5V (p-p), V_{SS} = 0V	V_{DD} = 5V, V_{EE} = −5V, 20 Log_{10} V_{OS}/V_{IS} = −40 dB					1					MHz
	Crosstalk Between Any Two Channels (Frequency at 40 dB)	R_L = 1 kΩ, V_{IS}(A) = 5V (p-p), V_{SS} = 0V	V_{DD} = 5V, V_{EE} = −5V, 20 Log_{10} V_{OS}(B)/V_{IS}(A) = −40 dB (Note 1)					1					MHz
C_{IS}	Capacitance Input (IN/OUT)	V_{DD} = V_{EE} = V_{SS} = 0V						10					pF
C_{OS}	Output (Common OUT/IN)		CD4051C					60					pF
			CD4052C					30					pF
			CD4053C					20					pF
C_{IOS}	Feedthrough							0.2					pF
t_{PLH}, t_{PHL}	Propagation Delay Signal Input to Signal Output	V_{DD} = 10V, V_{SS} = V_{EE} = Inhibit = 0V, C_L = 15 pF, V_{IS} = 10V (Square Wave), t_r, t_f = 20 ns (Input Signal)						10					ns
CONTROL INPUTS A, B, C AND INHIBIT													
	Noise Immunity (Any Control Input)												
V_{NL}		V_{IS} = V_{DD} through 1 kΩ, V_{EE} = V_{SS} I_{IS} = 10μA R_L = 1kΩ to V_{EE}	V_{DD} − V_{SS} = 10V	3.0			3.0	4.5		2.9			V
			V_{DD} − V_{SS} = 5V	1.5			1.5	2.25		1.4			V
V_{NH}			V_{DD} − V_{SS} = 10V	2.9			3.0	4.5		3.0			V
			V_{DD} − V_{SS} = 5V	1.4			1.5	2.25		1.5			V
C_I	Average Input Capacitance							5					pF
t_{PHL}, t_{PLH}	Turn "ON" Propagation Delay Control Input-to-Signal Output	C_L = 15 pF, R_L = 10 kΩ, $V_{IS} \leq V_{DD}$, t_r, t_f = 20 ns, V_{SS} = Inhibit = 0V, (Note 2)	V_{DD} = 10V, V_{EE} = 0V					150	300				ns
			V_{DD} = 5V, V_{EE} = 0V					400	800				ns
			V_{DD} = 5V, V_{EE} = −5V					200	400				ns
	Inhibit Input-to-Signal Output	C_L = 15 pF, R_L = 10 kΩ, V_{IS} = V_{DD} t_r, t_f = 20 ns	V_{DD} = 10V, V_{EE} = 0V					200	400				ns
			V_{DD} = 5V V_{EE} = 0V					550	1100				ns
	Inhibit Recovery Time	V_{DD} = 10V						200	400				ns

Note 1: A,B are two arbitrary channels with A turned "ON" and B "OFF."

Note 2: Channel Overlap = Turn "ON" delay, where channel overlap is defined as the duration after control signal change during which two channels may be "ON" together.

Note 3: V_{IS} = input signal voltage, V_{OS} = output signal voltage, f_{IS} = input signal frequency.

Special Considerations

In certain applications the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into "In/Out" pin, the voltage drop across the bidirectional switch must not exceed 0.6V at $T_A \leq 25°C$, or 0.4V at $T_A > 25°C$ (calculated from R_{ON} values shown). No V_{DD} current will flow through R_L if the switch current flows into "Out/In" pin.

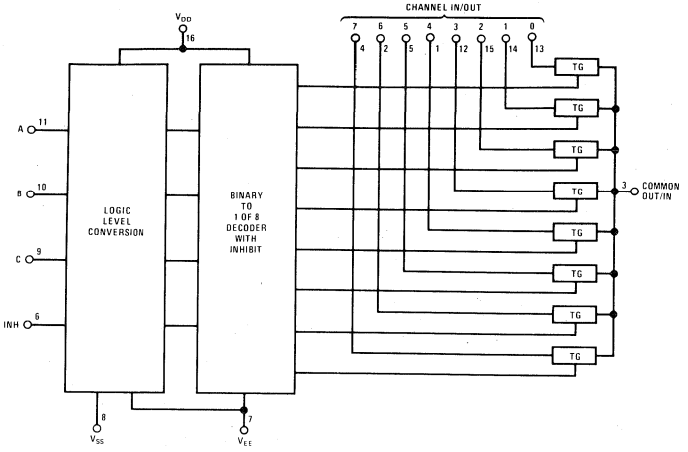
Truth Table

INPUT STATES				"ON" CHANNELS		
INHIBIT	C	B	A	CD4051A	CD4052A	CD4053A
0	0	0	0	0	0X, 0Y	cx, bx, ax
0	0	0	1	1	1X, 1Y	cx, bx, ay
0	0	1	0	2	2X, 2Y	cx, by, ax
0	0	1	1	3	3X, 3Y	cx, by, ay
0	1	0	0	4		cy, bx, ax
0	1	0	1	5		cy, bx, ay
0	1	1	0	6		cy, by, ax
0	1	1	1	7		cy, by, ay
1	*	*	*	NONE	NONE	NONE

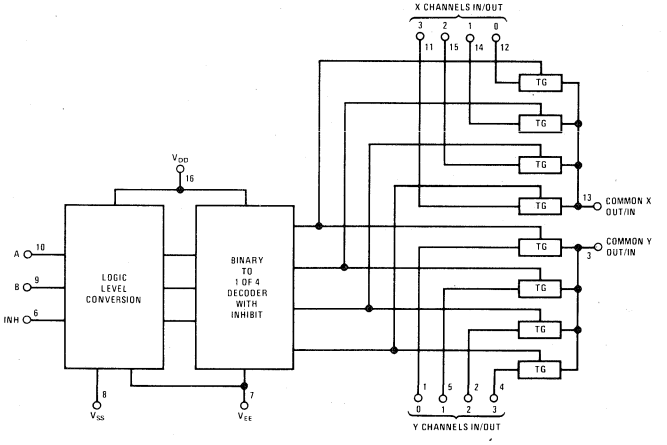
*Don't Care condition

Schematic Diagrams

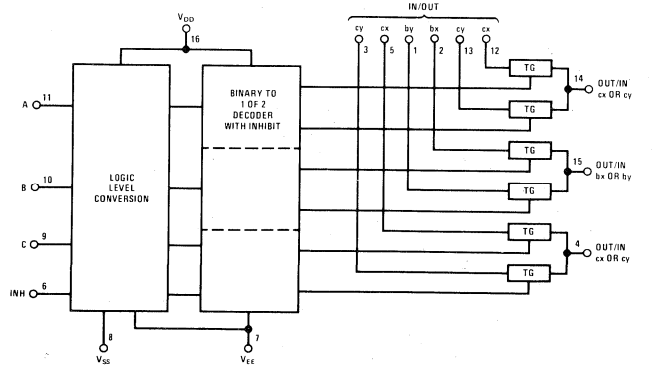
CD4051M/CD4051C



CD4052M/CD4052C

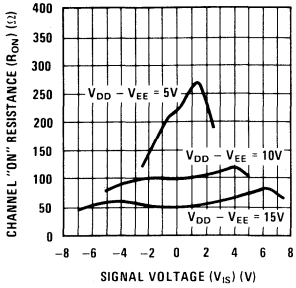


CD4053M/CD4053C

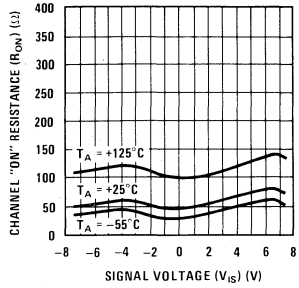


Typical Performance Characteristics

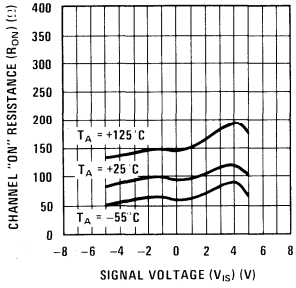
"ON" Resistance vs Signal Voltage for $T_A = 25°C$



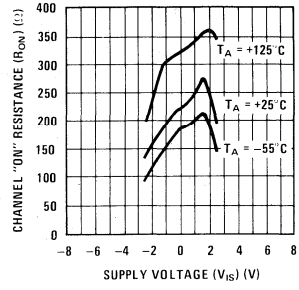
"ON" Resistance as a Function of Temperature for $V_{DD} - V_{EE} = 15V$



"ON" Resistance as a Function of Temperature for $V_{DD} - V_{EE} = 10V$



"ON" Resistance as a Function of Temperature for $V_{DD} - V_{EE} = 5V$



CD4066BM/CD4066BC Quad Bilateral Switch

General Description

The CD4066BM/CD4066BC is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals. It is pin-for-pin compatible with CD4016BM/CD4016BC, but has a much lower "ON" resistance, and "ON" resistance is relatively constant over the input-signal range.

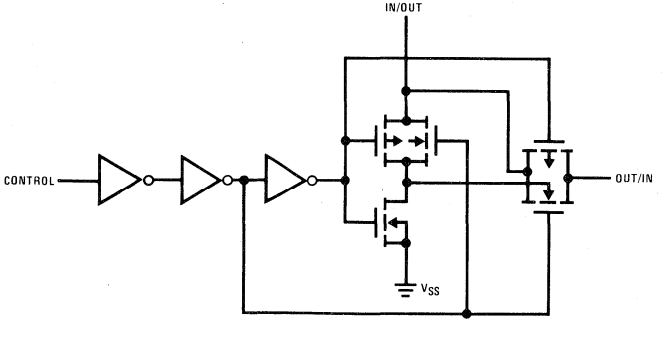
Features

- Wide supply voltage range — 3V to 15V
- High noise immunity — 0.45 V_{DD} typ
- Wide range of digital and analog switching — ±7.5 V_{PEAK}
- "ON" resistance for 15V operation — 80Ω typ
- Matched "ON" resistance over 15V signal input — ΔR_{ON} = 5Ω typ
- "ON" resistance flat over peak-to-peak signal range
- High "ON"/"OFF" output voltage ratio — 65 dB typ @ f_{is} = 10 kHz, R_L = 10 kΩ
- High degree of linearity — < 0.4% distortion typ @ f_{is} = 1 kHz, V_{is} = 5 Vp-p, $V_{DD} - V_{SS}$ = 10V, R_L = 10 kΩ
- Extremely low "OFF" switch leakage — 0.1 nA typ @ $V_{DD} - V_{SS}$ = 10V, T_A = 25°C
- Extremely high control input impedance — 10^{12}Ω typ
- Low crosstalk between switches — −50 dB typ @ f_{is} = 0.9 MHz, R_L = 1 kΩ
- Frequency response, switch "ON" — 40 MHz typ

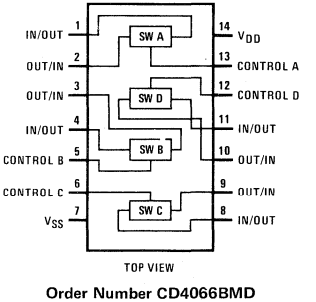
Applications

- Analog signal switching/multiplexing
  - Signal gating
  - Squelch control
  - Chopper
  - Modulator/Demodulator
  - Commutating switch
- Digital signal switching/multiplexing
- CMOS logic implementation
- Analog-to-digital/digital-to-analog conversion
- Digital control of frequency, impedance, phase, and analog-signal gain

Schematic and Connection Diagrams



Dual-In-Line and Flat Package



TOP VIEW

Order Number CD4066BMD
See Package 14
Order Number CD4066BMF
See Package 23
Order Number CD4066BCJ or CD4066BMJ
See Package 18
Order Number CD4066BCN
See Package 21

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} Supply Voltage	−0.5V to +18V
V_{IN} Input Voltage	−0.5V to V_{DD} + 0.5V
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

(Note 2)

V_{DD} Supply Voltage	3V to 15V
V_{IN} Input Voltage	0V to V_{DD}
T_A Operating Temperature Range	
CD4066BM	−55°C to +125°C
CD4066BC	−40°C to +85°C

DC Electrical Characteristics CD4066BM (Note 2)

	PARAMETER	CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		0.25		0.01	0.25		7.5	μA
		V_{DD} = 10V		0.5		0.01	0.5		15	μA
		V_{DD} = 15V		1.0		0.01	1.0		30	μA
SIGNAL INPUTS AND OUTPUTS										
R_{ON}	"ON" Resistance	R_L = 10 kΩ								
		V_C = V_{DD} V_{SS} V_{is}								
		7.5V −7.5V −7.5V to +7.5V		220		80	280		320	Ω
		15V 0V 0V to 15V								
		5V −5V −5V to +5V		400		120	500		550	Ω
		10V 0V 0V to 10V								
		2.5V −2.5V −2.5V to +2.5V		3000		270	5000		5500	Ω
		5V 0V 0V to 5V								
ΔR_{ON}	Δ"ON" Resistance	R_L = 10 kΩ								
	Between Any 2 of 4	V_C = V_{DD} V_{SS} V_{is}								
	Switches	7.5V −7.5V −7.5V to +7.5V				5				Ω
		15V 0V 0V to 15V								
		5V −5V −5V to +5V				10				Ω
		10V 0V 0V to 10V								
I_{OFF}	Input or Output Leakage	V_{DD} V_C = V_{SS} V_{is} V_{os}								
	Switch "OFF"	7.5V −7.5V ±7.5V 0V		±50		±0.1	±50		±500	nA
		5V −5V ±5V 0V		±50		±0.1	±50		±500	nA
CONTROL INPUTS										
V_{IL}	Low Level Input Voltage	V_{is} = V_{DD}, V_{os} = V_{SS}, $I_{is} \leq 10\,\mu A$								
		V_{DD} = 5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V		3.5		2.75	3.5		3.5	V
		V_{DD} = 10V		7.0		5.5	7.0		7.0	V
		V_{DD} = 15V		11.0		8.25	11.0		11.0	V
I_{IN}	Input Current	$V_{DD} - V_{SS}$ = 15V		±0.1		$\pm 10^{-5}$	±0.1		±1.0	μA
		$V_{DD} \geq V_{is} \geq V_{SS}$								
		$V_{DD} \geq V_C \geq V_{SS}$								

DC Electrical Characteristics CD4066BC (Note 2)

	PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		1.0		0.01	1.0		7.5	μA
		V_{DD} = 10V		2.0		0.01	2.0		15	μA
		V_{DD} = 15V		4.0		0.01	4.0		30	μA

DC Electrical Characteristics (Continued) CD4066BC (Note 2)

PARAMETER		CONDITIONS	−40°C MIN	−40°C MAX	25°C MIN	25°C TYP	25°C MAX	85°C MIN	85°C MAX	UNITS
SIGNAL INPUTS AND OUTPUTS										
R_{ON}	"ON" Resistance	R_L = 10 kΩ								
		$V_C = V_{DD}$ V_{SS} V_{is}								
		7.5V −7.5V −7.5V to +7.5V		250		80	280		300	Ω
		15V 0V 0V to 15V								
		5V −5V −5V to +5V		450		120	500		520	Ω
		10V 0V 0V to 10V								
		2.5V −2.5V −2.5V to +2.5V		3500		270	5000		5200	Ω
		5V 0V 0V to 5V								
ΔR_{ON}	Δ"ON" Resistance Between Any 2 of 4 Switches	R_L = 10 kΩ								
		$V_C = V_{DD}$ V_{SS} V_{is}								
		7.5V −7.5V −7.5V to +7.5V				5				Ω
		15V 0V 0V to 15V								
		5V −5V −5V to +5V				10				Ω
		10V 0V 0V to 10V								
I_{OFF}	Input or Output Leakage Switch "OFF"	V_{DD} $V_C = V_{SS}$ V_{is} V_{os}								
		7.5V −7.5V ±7.5V 0V		±50		±0.1	±50		±200	nA
		5V −5V ±5V 0V		±50		±0.1	±50		±200	nA
CONTROL INPUTS										
V_{IL}	Low Level Input Voltage	$V_{is} = V_{DD}$, $V_{os} = V_{SS}$, $I_{is} \leq 10\ \mu A$								
		V_{DD} = 5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V	3.5			2.75	3.5		3.5	V
		V_{DD} = 10V	7.0			5.5	7.0		7.0	V
		V_{DD} = 15V	11.0			8.25	11.0		11.0	V
I_{IN}	Input Current	$V_{DD} - V_{SS}$ = 15V		±0.3		$\pm 10^{-5}$	±0.3		±1.0	μA
		$V_{DD} \geq V_{is} \geq V_{SS}$								
		$V_{DD} \geq V_C \geq V_{SS}$								

AC Electrical Characteristics T_A = 25°C, $t_r = t_f$ = 20 ns and V_{SS} = 0V unless otherwise specified

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL}, t_{PLH}	Propagation Delay Time Signal Input to Signal Output	$V_{is} = V_{DD}$, C_L = 50 pF, *(Figure 1)*				
		V_{DD} = 5V		25	55	ns
		V_{DD} = 10V		15	35	ns
		V_{DD} = 15V		10	25	ns
t_{PZH}, t_{PZL}	Propagation Delay Time Control Input to Signal Output High Impedance to Logical Level	R_L = 10 kΩ, C_L = 50 pF, *(Figures 2 and 3)*				
		V_{DD} = 5V		90	180	ns
		V_{DD} = 10V		40	80	ns
		V_{DD} = 15V		30	60	ns
t_{PHZ}, t_{PLZ}	Propagation Delay Time Control Input to Signal Output Logical Level to High Impedance	R_L = 10 kΩ, C_L = 5 pF, *(Figures 2 and 3)*				
		V_{DD} = 5V		90	180	ns
		V_{DD} = 10V		60	120	ns
		V_{DD} = 15V		55	110	ns
	Sine Wave Distortion	$V_C = V_{DD}$ = 5V, V_{SS} = −5V, R_L = 10 kΩ, V_{is} = 5 Vp-p, f = 1 kHz, *(Figure 4)*		0.4		%
	Frequency Response—Switch "ON" (Frequency at −3 dB)	$V_C = V_{DD}$ = 5V, V_{SS} = −5V, R_L = 1 kΩ, V_{is} = 5 Vp-p, 20 Log_{10} V_{os}/V_{is} = −3 dB, *(Figure 4)*		40		MHz

AC Electrical Characteristics (Continued)

$T_A = 25^\circ C$, $t_r = t_f = 20$ ns and $V_{SS} = 0V$ unless otherwise specified

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	Feedthrough – Switch "OFF" (Frequency at –50 dB)	$V_{DD} = 5V$, $V_C = V_{SS} = -5V$, $R_L = 1\ k\Omega$, $V_{is} = 5$ Vp-p, 20 Log_{10}, $V_{os}/V_{is} = -50$ dB, *(Figure 4)*		1.25		MHz
	Crosstalk Between Any Two Switch (Frequency at –50 dB)	$V_{DD} = V_{C(1)} = 5V$; $V_{SS} = V_{C(2)} = -5V$, $R_L = 1\ k\Omega$, $V_{is(A)} = 5$ Vp-p, 20 Log_{10}, $V_{os(2)}/V_{is(1)} = -50$ dB, *(Figure 5)*		0.9		MHz
	Crosstalk: Control Input to Signal Output	$V_{DD} = 10V$, $R_L = 10\ k\Omega$, $R_{IN} = 1\ k\Omega$, $V_{CC} = 10V$ Square Wave, *(Figure 6)*		400		mVp-p
	Maximum Control Input Frequency (f at V_{os} = 1/2 $V_{DDp\text{-}p}$)	$R_L = 1\ k\Omega$, $C_L = 50$ pF, *(Figure 7)*				
		$V_{DD} = 5V$		6.0		MHz
		$V_{DD} = 10V$		8.0		MHz
		$V_{DD} = 15V$		8.5		MHz
C_{is}	Signal Input Capacitance			8		pF
C_{OS}	Signal Output Capacitance			8		pF
C_{ios}	Feedthrough Capacitance			0.5		pF
C_{IN}	Control Input Capacitance			5	7.5	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: These devices should not be connected to circuits with the power "ON".

Note 4: In all cases, there is approximately 5 pF of probe and jig capacitance on the output; however, this capacitance is included in C_L wherever it is specified.

AC Test Circuits and Switching Time Waveforms

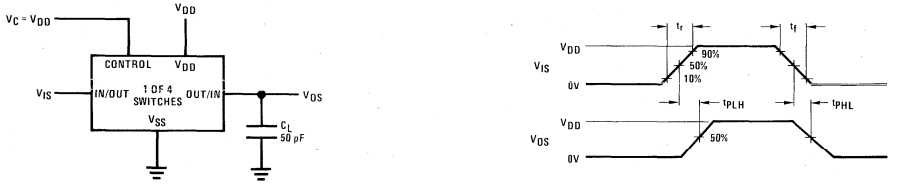


FIGURE 1. t_{PHL}, t_{PLH} Propagation Delay Time Signal Input to Signal Output

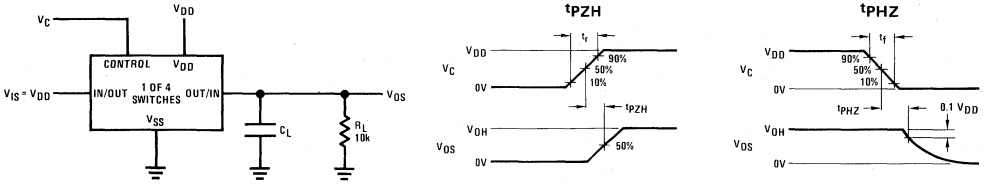


FIGURE 2. t_{PZH}, t_{PHZ} Propagation Delay Time Control to Signal Output

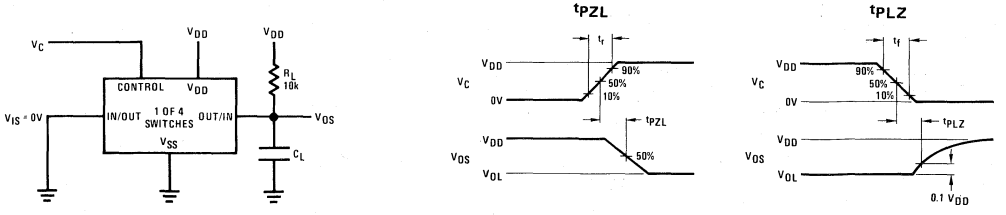
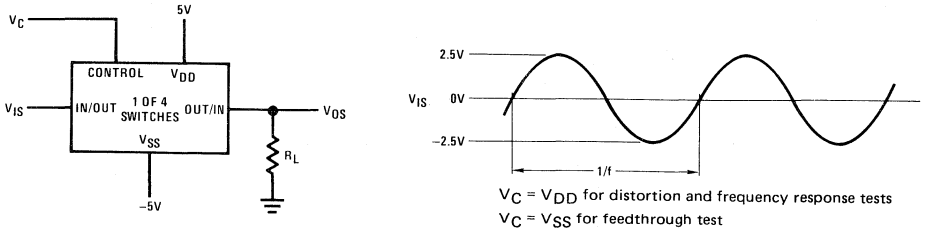


FIGURE 3. t_{PZL}, t_{PLZ} Propagation Delay Time Control to Signal Output

AC Test Circuits and Switching Time Waveforms (Continued)



$V_C = V_{DD}$ for distortion and frequency response tests
$V_C = V_{SS}$ for feedthrough test

FIGURE 4. Sine Wave Distortion, Frequency Response and Feedthrough

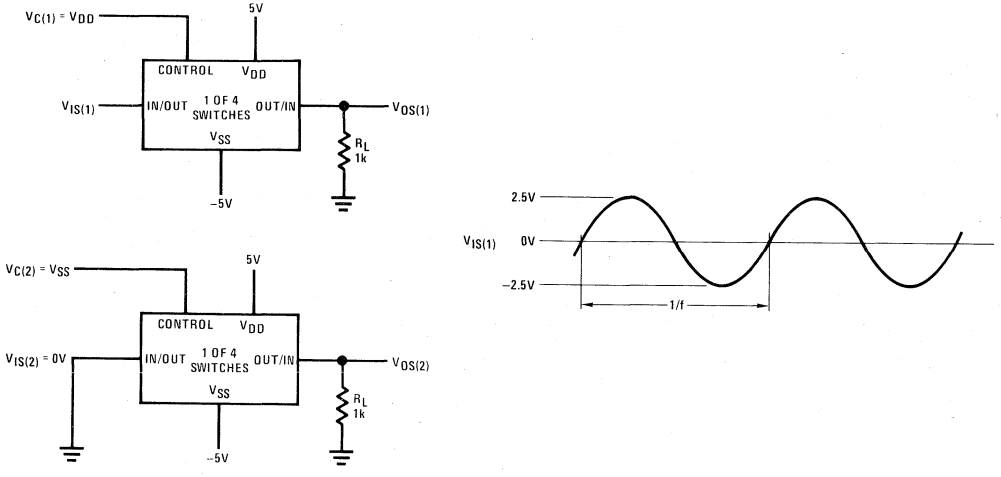


FIGURE 5. Crosstalk Between Any Two Switches

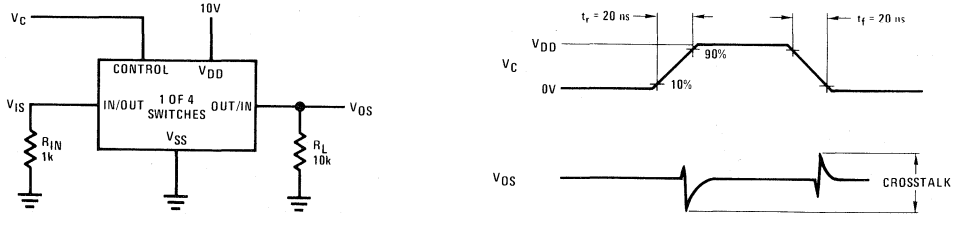


FIGURE 6. Crosstalk: Control Input to Signal Output

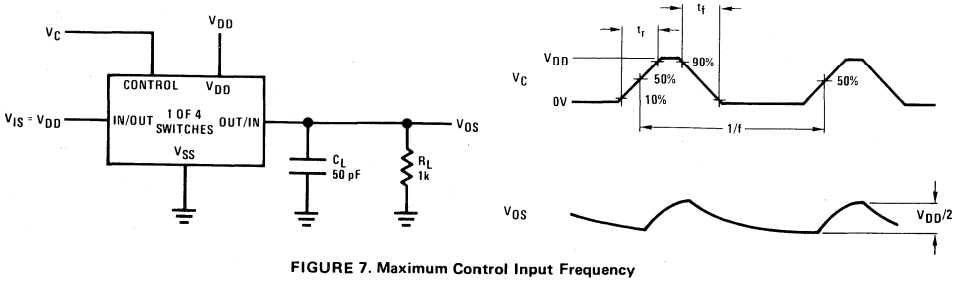
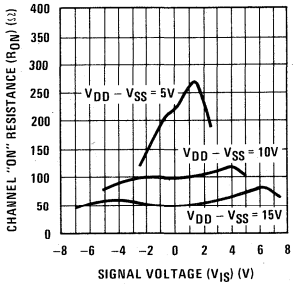


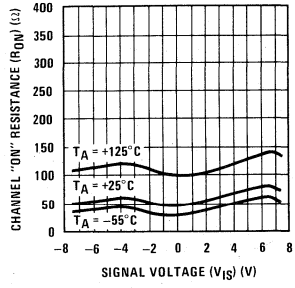
FIGURE 7. Maximum Control Input Frequency

Typical Performance Characteristics

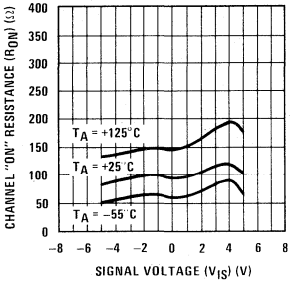
"ON" Resistance vs Signal Voltage for $T_A = 25°C$



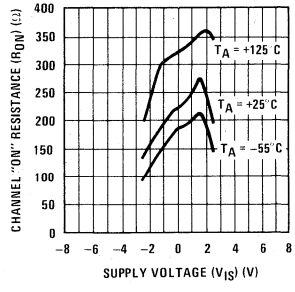
"ON" Resistance as a Function of Temperature for $V_{DD} - V_{SS} = 15V$



"ON" Resistance as a Function of Temperature for $V_{DD} - V_{SS} = 10V$



"ON" Resistance as a Function of Temperature for $V_{DD} - V_{SS} = 5V$

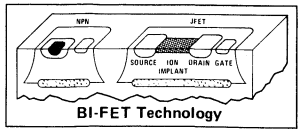


Special Considerations

In applications where separate power sources are used to drive V_{DD} and the signal input, the V_{DD} current capability should exceed V_{DD}/R_L (R_L = effective external load of the 4 CD4066BM/CD4066BC bilateral switches). This provision avoids any permanent current flow or clamp action on the V_{DD} supply when power is applied or removed from CD4066BM/CD4066BC.

In certain applications, the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into terminals 1, 4, 8 or 11, the voltage drop across the bidirectional switch must not exceed 0.6V at $T_A \leq 25°C$, or 0.4V at $T_A > 25°C$ (calculated from R_{ON} values shown).

No V_{DD} current will flow through R_L if the switch current flows into terminals 2, 3, 9 or 10.



BI-FET Technology

Quad SPST JFET Analog Switches

LF11331/LF12331/LF13331	4 normally open switches with disable
LF11332/LF12332/LF13332	4 normally closed switches with disable
LF11333/LF12333/LF13333	2 normally closed switches and 2 normally open switches with disable
LF11201/LF12201/LF13201	4 normally closed switches
LF11202/LF12202/LF13202	4 normally open switches

General Description

These devices are a monolithic combination of bipolar and JFET technology producing the industry's first one chip quad JFET switch. A unique circuit technique is employed to maintain a constant resistance over the analog voltage range of ±10V. The input is designed to operate from minimum TTL levels, and switch operation also ensures a break-before-make action.

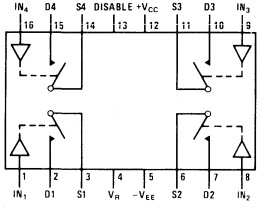
Features

- Analog signals are not loaded
- Constant "ON" resistance for signals up to ±10V and 100 kHz
- Pin compatible with CMOS switches with the advantage of blow out free handling
- Small signal analog signals to 50 MHz
- Break-before-make action $t_{OFF} < t_{ON}$
- High open switch isolation at 1.0 MHz −50 dB
- Low leakage in "OFF" state <1.0 nA
- TTL, DTL, RTL compatibility
- Single disable pin opens all switches in package on LF11331, LF11332, LF11333
- LF11201 is pin compatible with DG201

These devices operate from ±15V supplies and swing a ±10V analog signal. The JFET switches are designed for applications where a dc to medium frequency analog signal needs to be controlled.

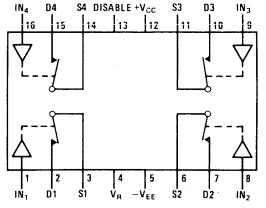
Connection Diagrams (Dual-In-Line Packages) (All Switches Shown are For Logical "0")

LF11331/LF12331/LF13331



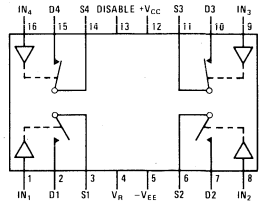
TOP VIEW

LF11332/LF12332/LF13332



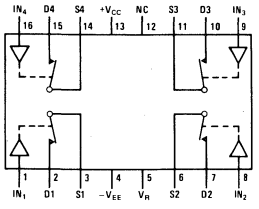
TOP VIEW

LF11333/LF12333/LF13333



TOP VIEW

LF11201/LF12201/LF13201

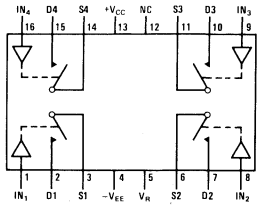


TOP VIEW

Order Number LF11201D, LF12201D, LF13201D, LF11202D, LF12202D, LF13202D, LF11331D, LF12331D, LF13331D, LF11332D, LF12332D, LF13332D, LF11333D, LF12333D or LF13333D
See Package 15

Order Number LF12201N, LF13201N, LF12202N, LF13202N, LF12331N, LF13331N, LF12332N, LF13332N, LF12333N or LF13333N
See Package 22

LF11202/LF12202/LF13202



TOP VIEW

Test Circuit and Schematic Diagram

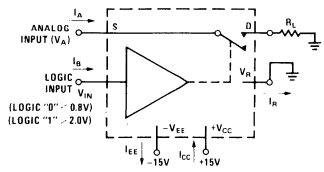


FIGURE 1. Typical Circuit for One Switch

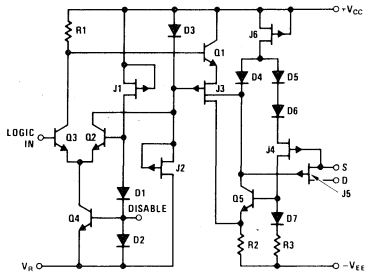


FIGURE 2. Schematic Diagram (Normally Open)

Absolute Maximum Ratings

Positive Supply – Negative Supply (V_{CC}–V_{EE})	36V
Reference Voltage	$V_{EE} \leq V_R \leq V_{CC}$
Logic Input Voltage	V_R –4.0V $\leq V_{IN} \leq V_R$ +6.0V
Analog Voltage	$V_{EE} \leq V_A \leq V_{CC}$ +6V; $V_A \leq V_{EE}$ +36V
Analog Current	$\lvert I_A \rvert < 20$ mA
Power Dissipation (Note 1)	
Molded DIP (N Suffix)	500 mW
Cavity DIP (D Suffix)	900 mW
Operating Temperature Range	
LF11201, 2 and LF11331, 2, 3	–55°C to +125°C
LF12201, 2 and LF12331, 2, 3	–25°C to +85°C
LF13201, 2 and LF13331, 2, 3	0°C to +70°C
Storage Temperature	–65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (Notes 2, 7)

SYMBOL	PARAMETER	CONDITIONS		LF11331/2/3 LF11201/2			LF12331/2/3 LF12201/2 LF13331/2/3 LF13201/2			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
R_{ON}	"ON" Resistance	V_A = 0, I_D = 1 mA	T_A = 25°C		150	200		150	250	Ω
					200	300		200	350	Ω
R_{ON} Match	"ON" Resistance Matching		T_A = 25°C		5	20		10	50	Ω
V_A	Analog Range			±10	±11		±10	±11		V
$I_{S(ON)}$ + $I_{D(ON)}$	Leakage Current in "ON" Condition	Switch "ON," V_S = V_D = ±10V	T_A = 25°C		0.3	5		0.3	10	nA
					3	100		3	30	nA
$I_{S(OFF)}$	Source Current in "OFF" Condition	Switch "OFF," V_S = +10V, V_D = –10V	T_A = 25°C		0.4	5		0.4	10	nA
					3	100		3	30	nA
$I_{D(OFF)}$	Drain Current in "OFF" Condition	Switch "OFF," V_S = +10V, V_D = –10V	T_A = 25°C		0.1	5		0.1	10	nA
					3	100		3	30	nA
V_{INH}	Logical "1" Input Voltage			2.0			2.0			V
V_{INL}	Logical "0" Input Voltage					0.8			0.8	V
I_{INH}	Logical "1" Input Current	V_{IN} = 5V	T_A = 25°C		3.6	10		3.6	40	μA
						25			100	μA
I_{INL}	Logical "0" Input Current	V_{IN} = 0.8	T_A = 25°C			0.1			0.1	μA
						1			1	μA
t_{ON}	Delay Time "ON"	V_S = ±10V, *(Figure 3)*	T_A = 25°C		500			500		ns
t_{OFF}	Delay Time "OFF"	V_S = ±10V, *(Figure 3)*	T_A = 25°C		90			90		ns
$t_{ON} - t_{OFF}$	Break-Before-Make	V_S = ±10V, *(Figure 3)*	T_A = 25°C		80			30		ns
$C_{S(OFF)}$	Source Capacitance	Switch "OFF," V_S = ±10V	T_A = 25°C		4.0			4.0		pF
$C_{D(OFF)}$	Drain Capacitance	Switch "OFF," V_D = ±10V	T_A = 25°C		3.0			3.0		pF
$C_{S(ON)}$ + $C_{D(ON)}$	Active Source and Drain Capacitance	Switch "ON," V_S = V_D = 0V	T_A = 25°C		5.0			5.0		pF
$I_{SO(OFF)}$	"OFF" Isolation	*(Figure 4)*, (Note 3)	T_A = 25°C		–50			–50		dB
CT	Crosstalk	*(Figure 4)*, (Note 3)	T_A = 25°C		–65			–65		dB
SR	Analog Slew Rate	(Note 4)	T_A = 25°C		50			50		V/μs
I_{DIS}	Disable Current	*(Figure 5)*, (Note 5)	T_A = 25°C		0.4	1.0		0.6	1.5	mA
					0.6	1.5		0.9	2.3	mA
I_{EE}	Negative Supply Current	All Switches "OFF," V_S = ±10V	T_A = 25°C		3.0	5.0		4.3	7.0	mA
					4.2	7.5		6.0	10.5	mA
I_R	Reference Supply Current	All Switches "OFF," V_S = ±10V	T_A = 25°C		2.0	4.0		2.7	5.0	mA
					2.8	6.0		3.8	7.5	mA
I_{CC}	Positive Supply Current	All Switches "OFF," V_S = ±10V	T_A = 25°C		4.5	6.0		7.0	9.0	mA
					6.3	9.0		9.8	13.5	mA

Note 1: For operating at high temperature the molded DIP products must be derated based on a +100°C maximum junction temperature and a thermal resistance of +150°C/W, devices in the cavity DIP are based on a +150°C maximum junction temperature and are derated at +100°C/W.

Note 2: Unless otherwise specified, V_{CC} = +15V, V_{EE} = –15V, V_R = 0V, and limits apply for –55°C $\leq T_A \leq$ +125°C for the LF11331,2,3 and the LF11201,2, –25°C $\leq T_A \leq$ +85°C for the LF12331,2,3 and the LF12201,2, and 0°C $\leq T_A \leq$ +70°C for the LF13331,2,3 and the LF13201,2.

Note 3: These parameters are limited by the pin to pin capacitance of the package.

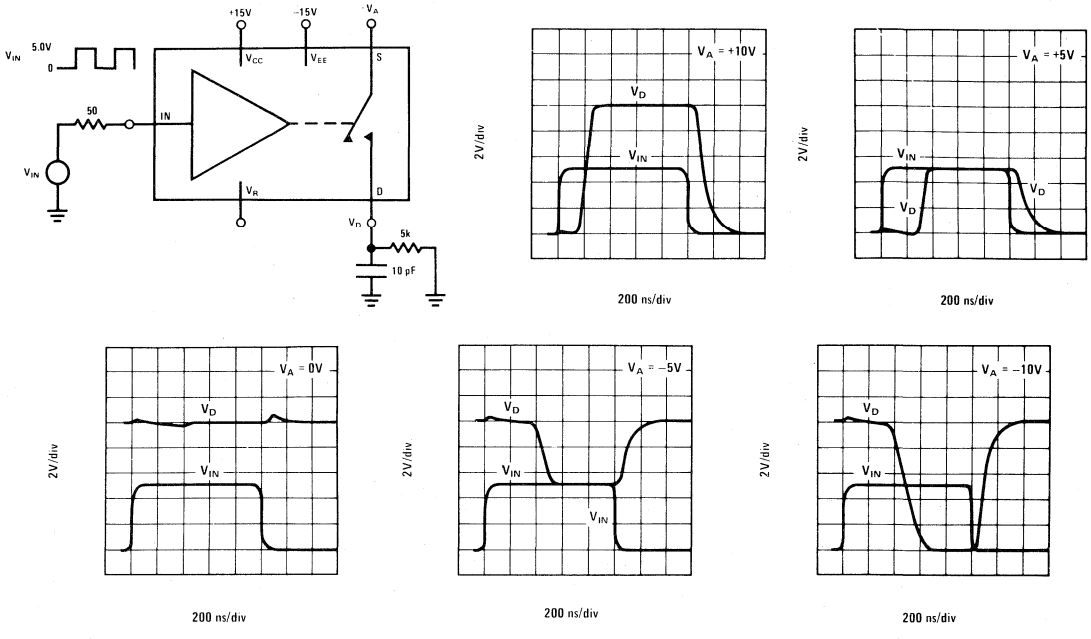
Note 4: This is the analog signal slew rate above which the signal is distorted as a result of finite internal slew rates.

Note 5: All switches in the device are turned "OFF" by saturating a transistor at the disable node as shown in *Figure 5*. The delay times will be approximately equal to the t_{ON} or t_{OFF} plus the delay introduced by the external transistor.

Note 6: This graph indicates the analog current at which 1% of the analog current is lost when the drain is positive with respect to the source.

Test Circuit and Typical Performance Curves

Delay Time, Rise Time, Settling Time, and Switching Transients



Additional Test Circuits

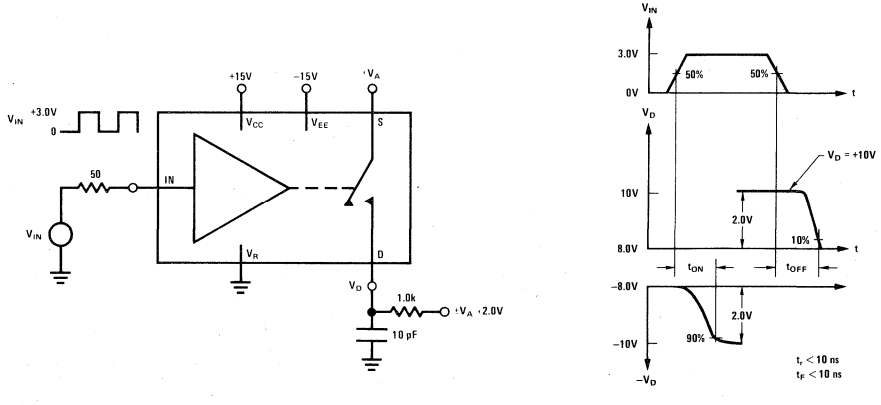


FIGURE 3. t_{ON}, t_{OFF} Test Circuit and Waveforms for a Normally Open Switch

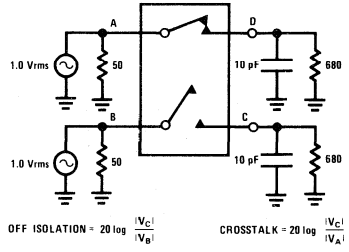
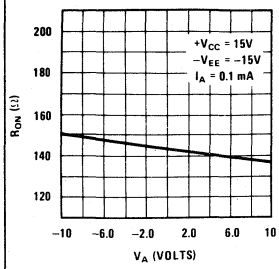


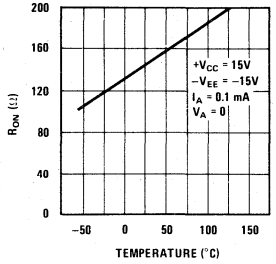
FIGURE 4. "OFF" Isolation, Crosstalk, Small Signal Response

Typical Performance Characteristics

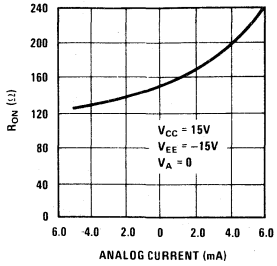
"ON" Resistance



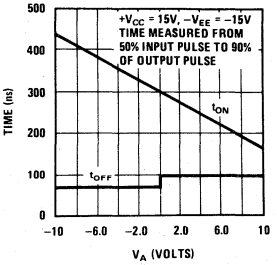
"ON" Resistance



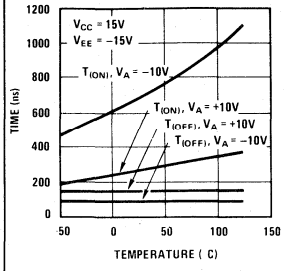
"ON" Resistance



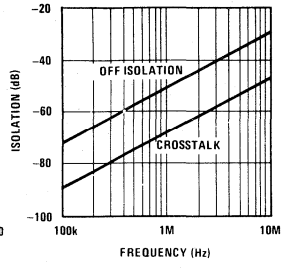
Break-Before-Make Action



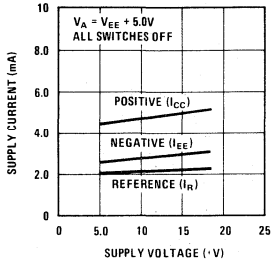
Switching Times



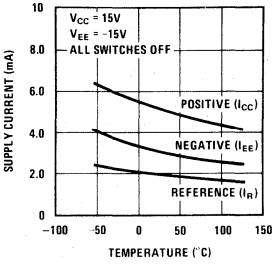
Crosstalk and "OFF" Isolation vs Frequency Using Test Circuit of *Figure 5*



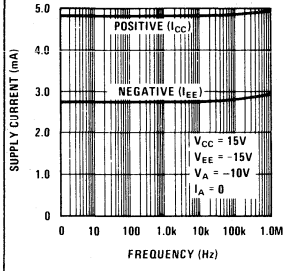
Supply Current



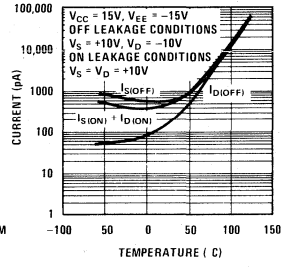
Supply Current



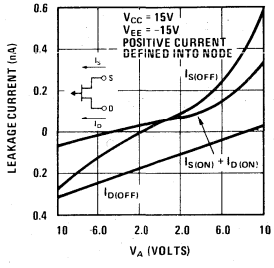
Supply Current



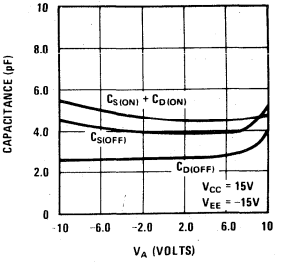
Switch Leakage Currents



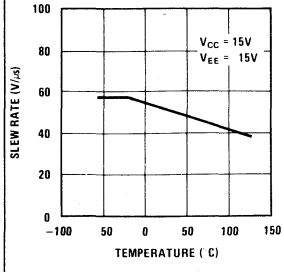
Switch Leakage Current



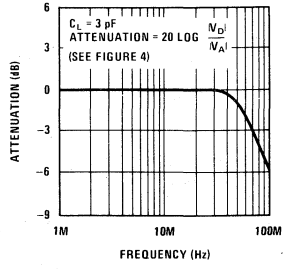
Switch Capacitances



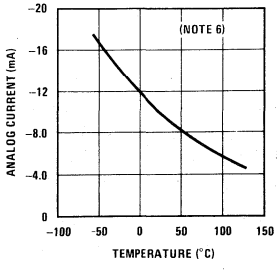
Slew Rate of Analog Voltage Above Which Signal Loading Occurs



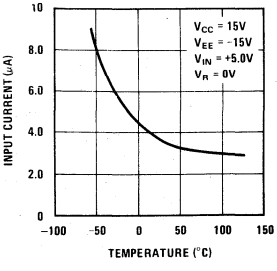
Small Signal Response



Maximum Accurate Analog Current vs Temperature



Logical "1" Input Bias Current



5

Application Hints

GENERAL INFORMATION

These devices are monolithic quad JFET analog switches with "ON" resistances which are essentially independent of analog voltage or analog current. The leakage currents are typically less than 1 nA at 25°C in both the "OFF" and "ON" switch states and introduce negligible errors in most applications. Each switch is controlled by minimum TTL logic levels at its input and is designed to turn "OFF" faster than it will turn "ON." This prevents two analog sources from being transiently connected together during switching. The switches were designed for applications which require break-before-make action, no analog current loss, medium speed switching times and moderate analog currents.

Because these analog switches are JFET rather than CMOS, they do not require special handling.

LOGIC INPUTS

The logic input (IN), of each switch, is referenced to two forward diode drops (1.4V at 25°C) from the reference supply (V_R) which makes it compatible with DTL, RTL, and TTL logic families. For normal operation, the logic "0" voltage can range from 0.8V to −4.0V with respect to V_R and the logic "1" voltage can range from 2.0V to 6.0V with respect to V_R, provided V_{IN} is not greater than (V_{CC} − 2.5V). If the input voltage is greater than (V_{CC} − 2.5V), the input current will increase. If the input voltage exceeds 6.0V or −4.0V with respect to V_R, a resistor in series with the input should be used to limit the input current to less than 100μA.

ANALOG VOLTAGE AND CURRENT

Analog Voltage

Each switch has a constant "ON" resistance (R_{ON}) for analog voltages from (V_{EE} + 5V) to (V_{CC} − 5V). For analog voltages greater than (V_{CC} − 5V), the switch will remain ON independent of the logic input voltage. For analog voltages less than (V_{EE} + 5V), the ON resistance of the switch will increase. Although the switch will not operate normally when the analog voltage is out of the previously mentioned range, the source voltage can go to either (V_{EE} + 36V) or (V_{CC} + 6V), whichever is more positive, and can go as negative as V_{EE} without destruction. The drain (D) voltage can also go to either (V_{EE} + 36V) or (V_{CC} + 6V), whichever is more positive, and can go as negative as (V_{CC} − 36V) without destruction.

Analog Current

With the source (S) positive with respect to the drain (D), the R_{ON} is constant for low analog currents, but will increase at higher currents (>5 mA) when the FET enters the saturation region. However, if the drain is positive with respect to the source and a small analog current loss at high analog currents (Note 6) is tolerable, a low R_{ON} can be maintained for analog currents greater than 5 mA at 25°C.

LEAKAGE CURRENTS

The drain and source leakage currents, in both the ON and the OFF states of each switch, are typically less than 1 nA at 25°C and less than 100 nA at 125°C. As shown in the typical curves, these leakage currents are dependent on power supply voltages, analog voltage, analog current and the source to drain voltage.

DELAY TIMES

The delay time OFF (t_{OFF}) is essentially independent of both the analog voltage and temperature. The delay time ON (t_{ON}) will decrease as either ($V_{CC} - V_A$) decreases or the temperature decreases.

POWER SUPPLIES

The voltage between the positive supply (V_{CC}) and either the negative supply (V_{EE}) or the reference supply (V_R) can be as much as 36V. To accommodate variations in input logic reference voltages, V_R can range from V_{EE} to (V_{CC} − 4.5V). Care should be taken to ensure that the power supply leads for the device never become reversed in polarity or that the device is never inadvertantly installed backwards in a test socket. If one of these conditions occurs, the supplies would zener an interal diode to an unlimited current; and result in a destroyed device.

SWITCHING TRANSIENTS

When a switch is turned OFF or ON, transients will appear at the load due to the internal transient voltage at the gate of the switch JFET being coupled to the drain and source by the junction capacitances of the JFET. The magnitude of these transients is dependent on the load. A lower value R_L produces a lower transient voltage. A negative transient occurs during the delay time ON, while a positive transient occurs during the delay time OFF. These transients are relatively small when compared to faster switch families.

DISABLE NODE

This node can be used, as shown in *Figure 5,* to turn all the switches in the unit off independent of logic inputs. Normally, the node floats freely at an internal diode drop (≈ 0.7V) above V_R. When the external transistor in *Figure 5* is saturated, the node is pulled very close to V_R and the unit is disabled. Typically, the current from the node will be less than 1 mA. This feature is not available on the LF11201 or LF11202 series.

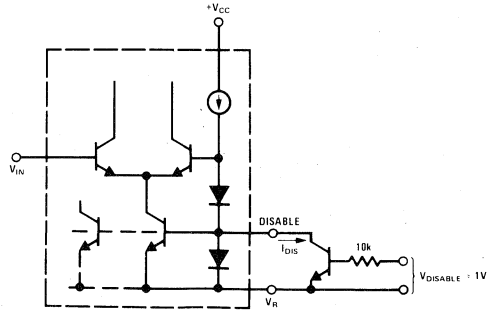
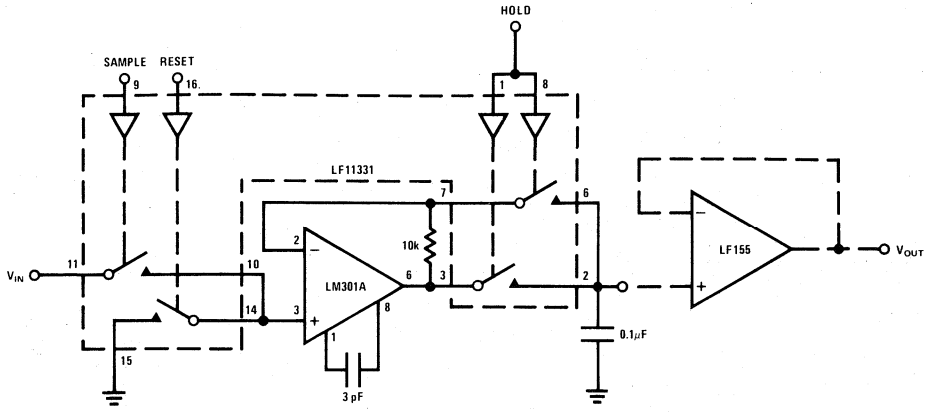


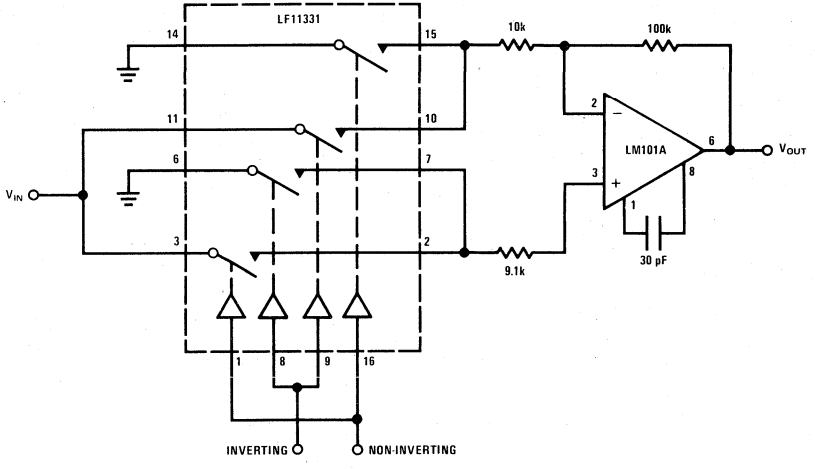
FIGURE 5. Disable Function

Typical Applications

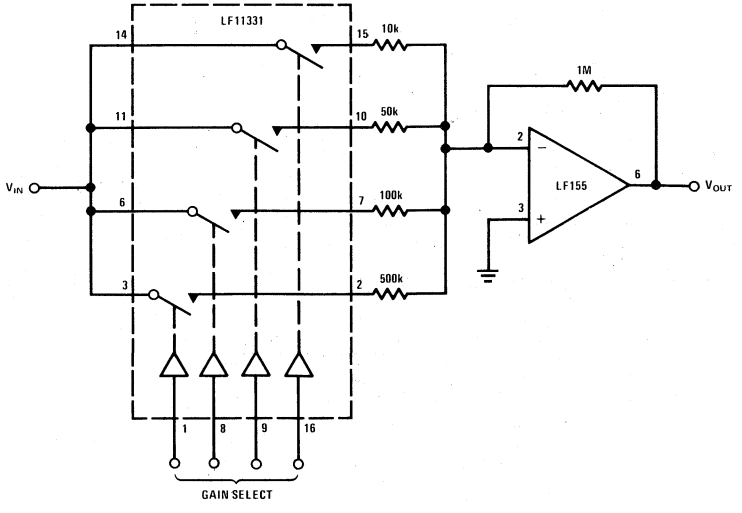
Sample and Hold with Reset



Programmable Inverting Non-Inverting Operational Amplifier

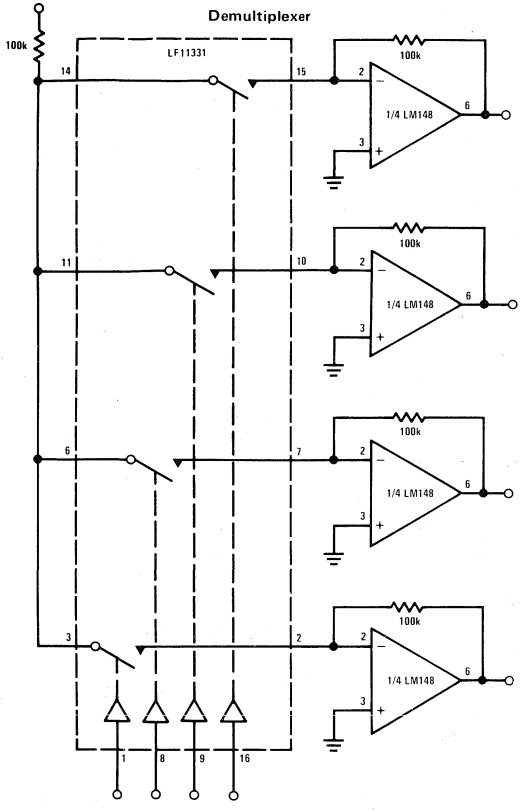


Programmable Gain Operational Amplifier

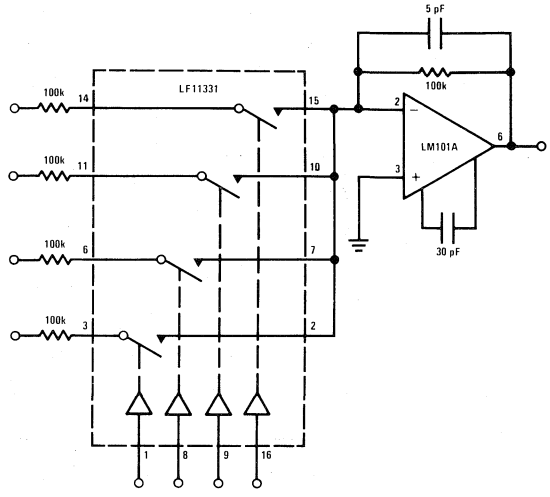


Typical Applications (Continued)

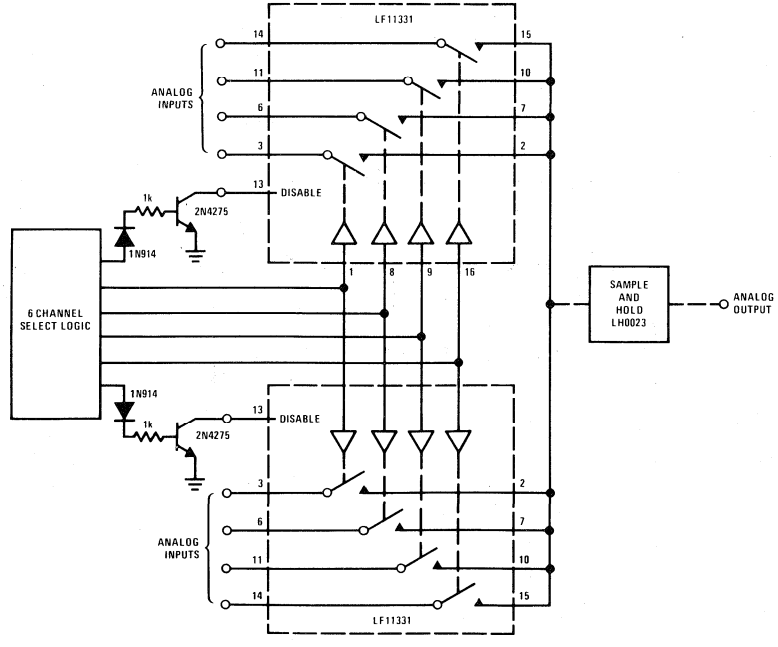
Demultiplexer



Multiplexer/Mixer

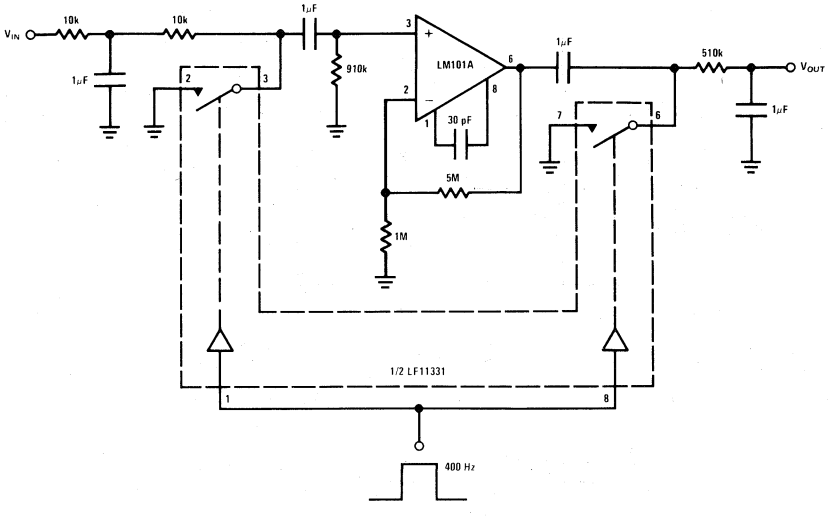


8-Channel Analog Commutator with 6-Channel Select Logic

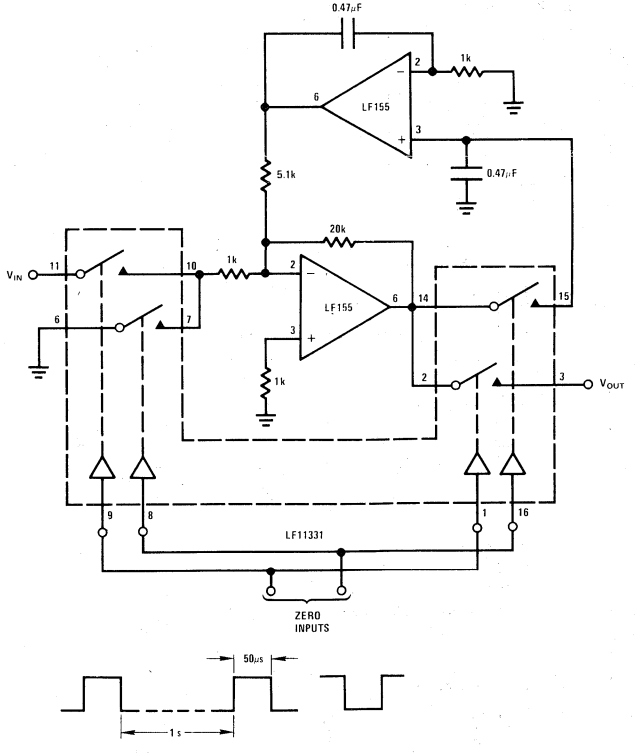


Typical Applications (Continued)

Chopper Channel Amplifier

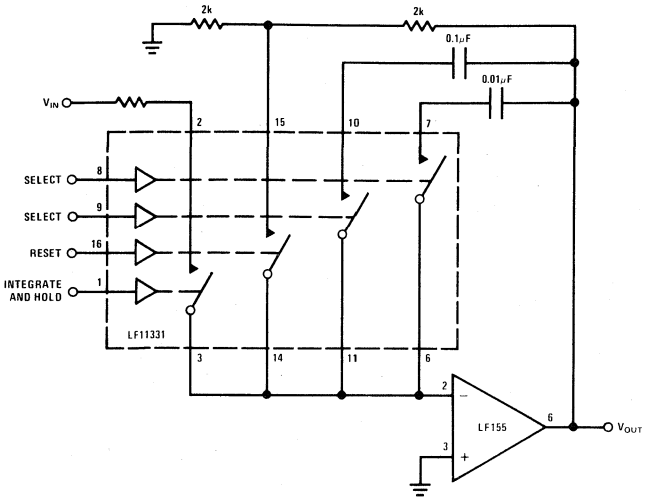


Self-Zeroing Operational Amplifier

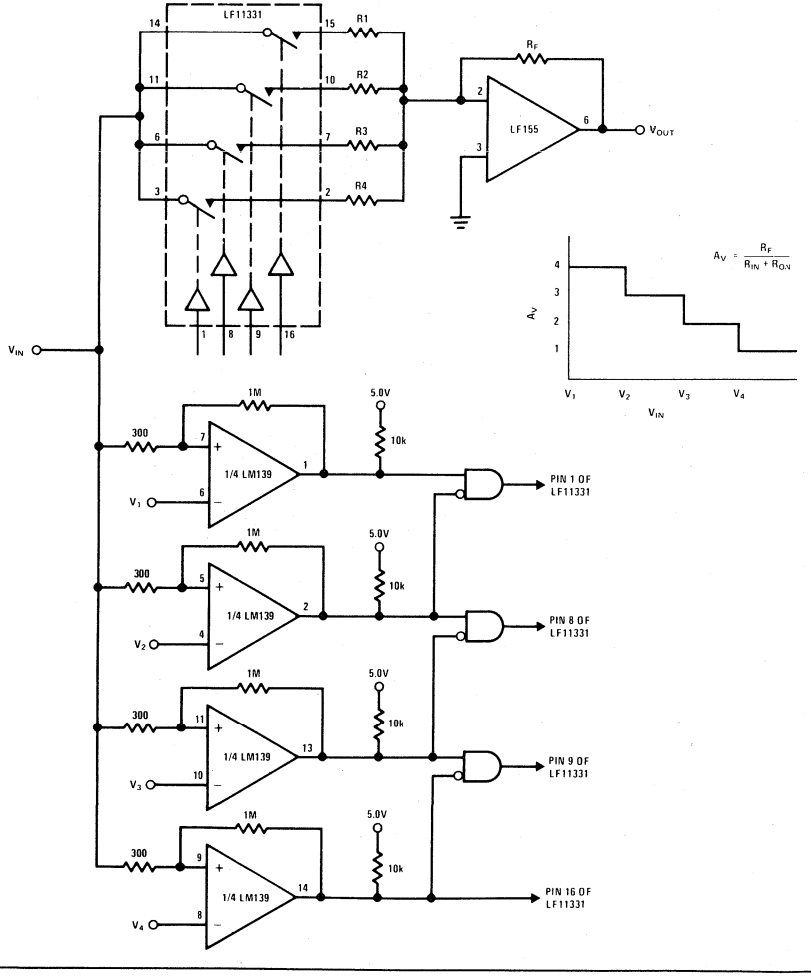


Typical Applications (Continued)

Programmable Integrator with Reset and Hold

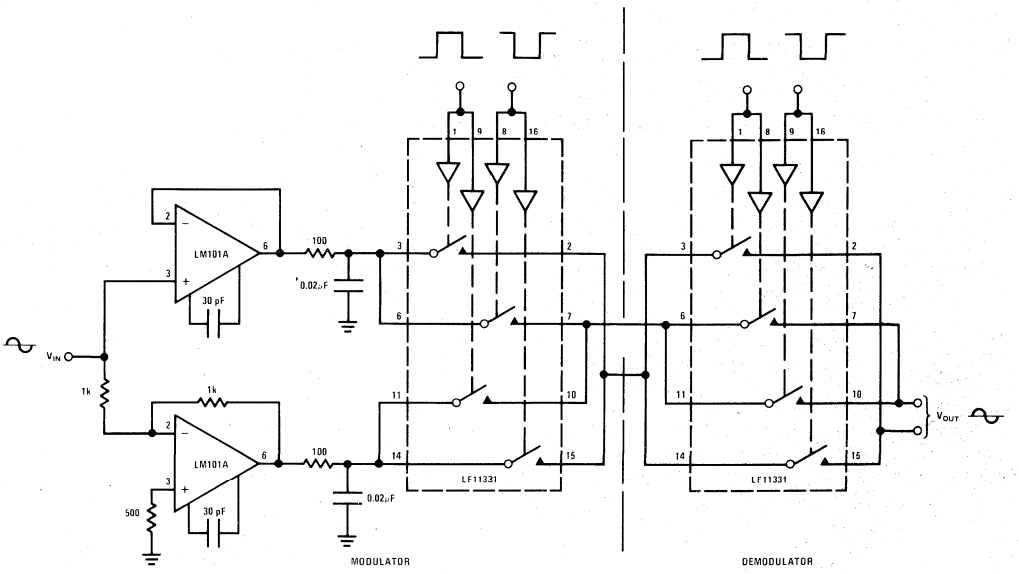


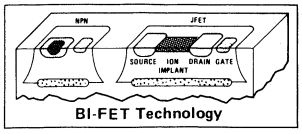
Staircase Transfer Function Operational Amplifier



Typical Applications (Continued)

DSB Modulator-Demodulator





LF11508/LF12508/LF13508 8-Channel Analog Multiplexer LF11509/LF12509/LF13509 4-Channel Differential Analog Multiplexer

General Description

The LF11508/LF12508/LF13508 is an 8-channel analog multiplexer which connects the output to 1 of the 8 analog inputs depending on the state of a 3-bit binary address. An enable control allows disconnecting the output, thereby providing a package select function.

This device is fabricated with National's BI-FET technology which provides ion-implanted JFETs for the analog switch on the same chip as the bipolar decode and switch drive circuitry. This technology makes possible low constant "ON" resistance with analog input voltage variations. This device does not suffer from latch-up problems or static charge blow-out problems associated with similar CMOS parts. The digital inputs are designed to operate from both TTL and CMOS levels while always providing a definite break-before-make action.

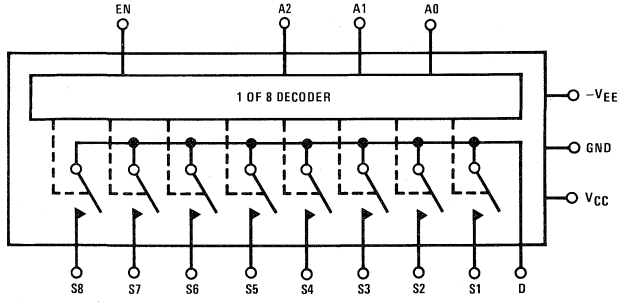
The LF11509/LF12509/LF13509 is a 4-channel differential analog multiplexer. A 2-bit binary address will connect a pair of independent analog inputs to one of any 4 pairs of independent analog outputs. The device has all the features of the LF11508 series and should be used whenever differential analog inputs are required.

Features

- JFET switches rather than CMOS
- No static discharge blow-out problem
- No SCR latch-up problems
- Analog signal range 11V, −15V
- Constant "ON" resistance for analog signals between −11V and 11V
- "ON" resistance 380 Ω typ
- Digital inputs compatible with TTL and CMOS
- Output enable control
- Break-before-make action: t_{OFF} = 0.2 μs; t_{ON} = 2 μs typ

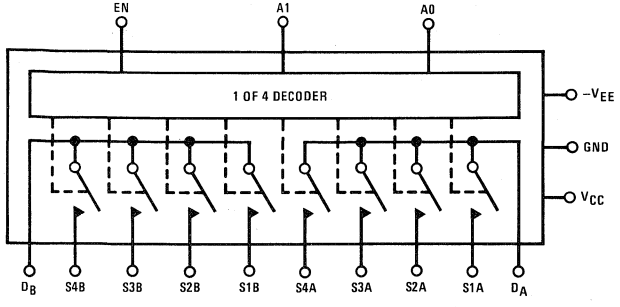
Functional Diagrams and Truth Tables

LF11508/LF12508/LF13508



EN	A2	A1	A0	SWITCH ON
H	L	L	L	S1
H	L	L	H	S2
H	L	H	L	S3
H	L	H	H	S4
H	H	L	L	S5
H	H	L	H	S6
H	H	H	L	S7
H	H	H	H	S8
L	X	X	X	NONE

LF11509/LF12509/LF13509



EN	A1	A0	SWITCH PAIR ON
L	X	X	None
H	L	L	S1
H	L	H	S2
H	H	L	S3
H	H	H	S4

Absolute Maximum Ratings

	LF11508, LF11509	LF12508, LF12509	LF13508, LF13509
Positive Supply − Negative Supply ($V_{CC} - V_{EE}$)	36V	36V	36V
Positive Analog Input Voltage (Note 1)	V_{CC}	V_{CC}	V_{CC}
Negative Analog Input Voltage (Note 1)	$-V_{EE}$	$-V_{EE}$	$-V_{EE}$
Positive Digital Input Voltage	V_{CC}	V_{CC}	V_{CC}
Negative Digital Input Voltage	−5V	−5V	−5V
Analog Switch Current	$\|I_S\| < 10$ mA	$\|I_S\| < 10$ mA	$\|I_S\| < 10$ mA
Power Dissipation (P_D at 25°C) and Thermal Resistance (θ_{jA}), (Note 2)			
Molded DIP (N) P_D	−	−	500 mW
θ_{jA}	−	−	150°C/W
Cavity DIP (D) P_D	900 mW	900 mW	900 mW
θ_{jA}	100°C/W	100°C/W	100°C/W
Maximum Junction Temperature (T_{jMAX})	150°C	110°C	100°C
Operating Temperature Range	$-55°C \leq T_A \leq +125°C$	$-25°C \leq T_A \leq +85°C$	$0°C \leq T_A \leq +70°C$
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 60 seconds)	300°C	300°C	300°C

Electrical Characteristics (Note 3)

SYMBOL	PARAMETER	CONDITIONS		LF11508, LF11509			LF12508, LF12509, LF13508, LF13509			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
R_{ON}	"ON" Resistance	V_{OUT} = 0V, I_S = 100 μA	T_A = 25°C		380	500		380	650	Ω
					600	750		500	850	Ω
ΔR_{ON}	ΔR_{ON} with Analog Voltage Swing	$-10V \leq V_{OUT} \leq +10V$, I_S = 100 μA	T_A = 25°C		0.01	1		0.01	1	%
R_{ON} Match	R_{ON} Match Between Switches	V_{OUT} = 0V, I_S = 100 μA	T_A = 25°C		20	100		20	150	Ω
$I_{S(OFF)}$	Source Current in "OFF" Condition	Switch "OFF", V_S = 11, V_D = −11, (Note 4)	T_A = 25°C			1			5	nA
					10	50		0.09	50	nA
$I_{D(OFF)}$	Drain Current in "OFF" Condition	Switch "OFF", V_S = 11, V_D = −11, (Note 4)	T_A = 25°C			10			20	nA
					25	500		0.6	500	nA
$I_{D(ON)}$	Leakage Current in "ON" Condition	Switch "ON" V_D = 11V, (Note 4)	T_A = 25°C			10			20	nA
					35	500		1	500	nA
V_{INH}	Digital "1" Input Voltage			2.0			2.0			V
V_{INL}	Digital "0" Input Voltage					0.7			0.7	V
I_{INL}	Digital "0" Input Current	V_{IN} = 0.7V	T_A = 25°C		1.5	20		1.5	30	μA
						40			40	μA
$I_{INL(EN)}$	Digital "0" Enable Current	V_{EN} = 0.7V	T_A = 25°C		1.2	20		1.2	30	μA
						40			40	μA
t_{TRAN}	Switching Time of Multiplexer	*(Figure 1)*, (Note 5)	T_A = 25°C		2.0	3		1.8		μs
t_{OPEN}	Break-Before-Make	*(Figure 3)*	T_A = 25°C		1.6			1.6		μs
$t_{ON(EN)}$	Enable Delay "ON"	*(Figure 2)*	T_A = 25°C		1.6			1.6		μs
$t_{OFF(EN)}$	Enable Delay "OFF"	*(Figure 2)*	T_A = 25°C		0.2			0.2		μs
$I_{SO(OFF)}$	"OFF" Isolation	(Note 6)	T_A = 25°C		−66			−66		dB
CT	Crosstalk	LF11509 Series, (Note 6)	T_A = 25°C		−66			−66		dB
$C_{S(OFF)}$	Source Capacitance ("OFF")	Switch "OFF", V_{OUT} = 0V, V_S = 0V	T_A = 25°C		2.2			2.2		pF
$C_{D(OFF)}$	Drain Capacitance ("OFF")	Switch "OFF", V_{OUT} = 0V, V_S = 0V	T_A = 25°C		11.4			11.4		pF
I_{CC}	Positive Supply Current	All Digital Inputs Grounded	T_A = 25°C		7.4	10		7.4	12	mA
					9.2	13		7.9	15	mA
I_{EE}	Negative Supply Current	All Digital Inputs Grounded	T_A = 25°C		2.7	4.5		2.7	5	mA
					2.9	5.5		2.8	6	mA

Notes

Note 1: If the analog input voltage exceeds this limit, the input current should be limited to less than 10 mA.

Note 2: The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by T_{jMAX}, θ_{jA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_D = (T_{jMAX} - T_A)/\theta_{jA}$ or the 25°C P_{DMAX}, whichever is less.

Note 3: These specifications apply for $V_S = \pm 15V$ and over the absolute maximum operating temperature range ($T_L \leq T_A \leq T_H$) unless otherwise noted.

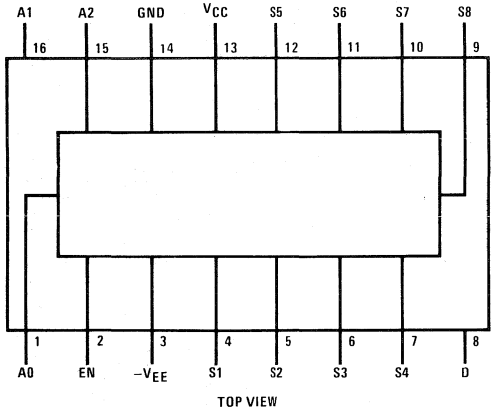
Note 4: Conditions applied to leakage tests insure worse case leakages. Exceeding 11V on the analog input may cause an "OFF" channel to turn "ON".

Note 5: Lots are sample tested to this parameter. The measurement conditions of *Figure 1* insure worse case transition time.

Note 6: "OFF" isolation is measured with all switches "OFF" and driving a source. Crosstalk is measured with a pair of switches "ON", driving channel A and measuring channel B. $R_L = 200$, $C_L = 7$ pF, $V_S = 3$ Vrms, f = 500 kHz.

Connection Diagrams

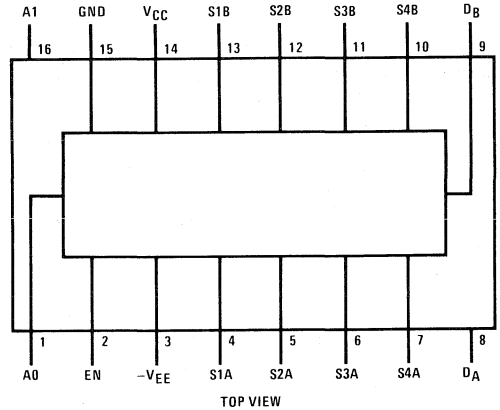
Dual-In-Line Package



TOP VIEW

Order Numbers LF11508D, LF12508D, LF13508D or LF13508N
See Packages 17 and 22

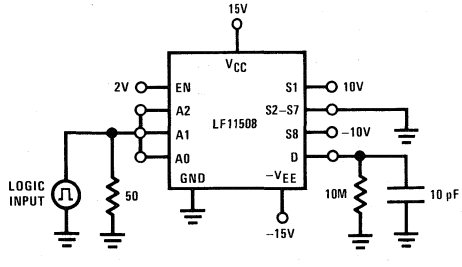
Dual-In-Line Package



TOP VIEW

Order Numbers LF11509D, LF12509D, LF13509D or LF13509N
See Packages 17 and 22

AC Test Circuits and Switching Time Waveforms



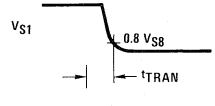
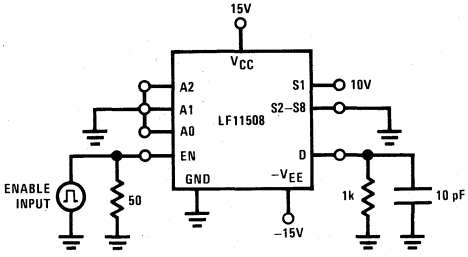


FIGURE 1. Transition Time

AC Test Circuits and Switching Time Waveforms (Continued)



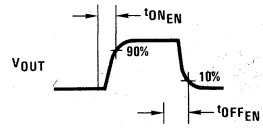
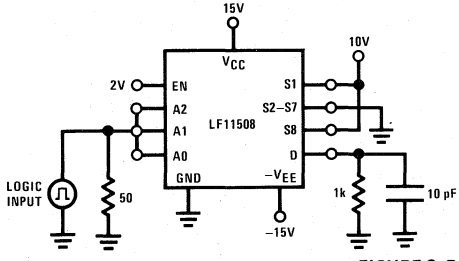


FIGURE 2. Enable Times



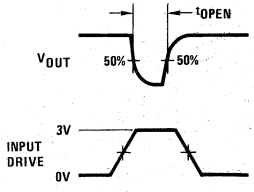
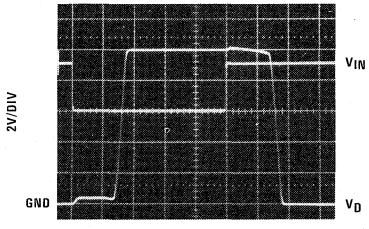


FIGURE 3. Break-Before-Make

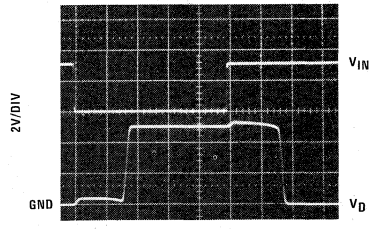
Transition Times and Transients

V_A = 10V



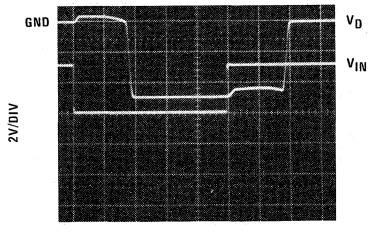
1 μS/DIV

V_A = 5V



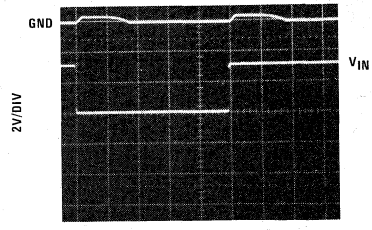
1 μS/DIV

V_A = 0V



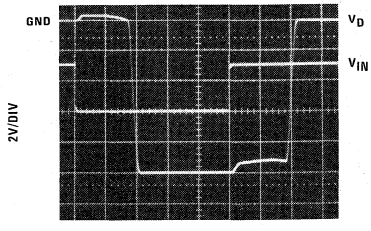
1 μS/DIV

V_A = –5V



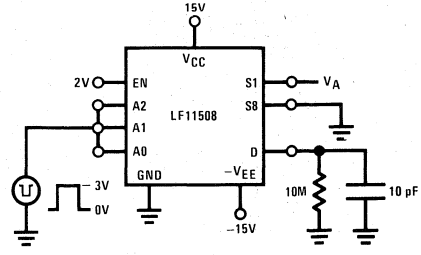
1 μS/DIV

V_A = –10V



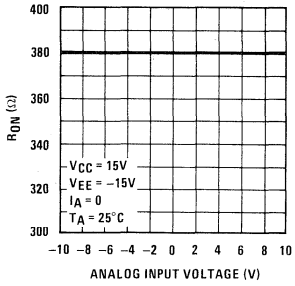
1 μS/DIV

Test Circuit

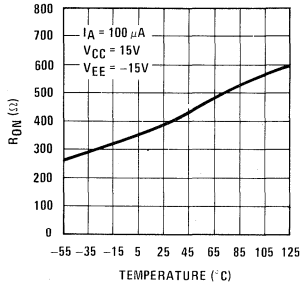


Typical Performance Characteristics

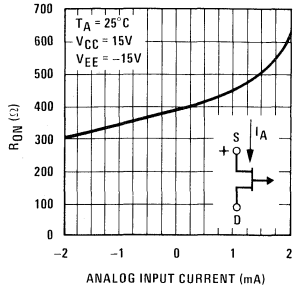
"ON" Resistance



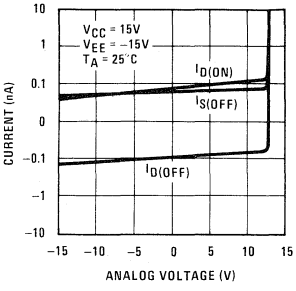
"ON" Resistance



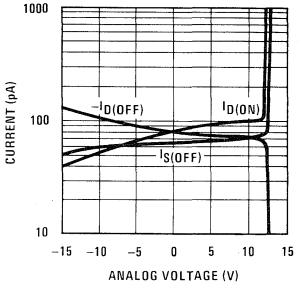
"ON" Resistance



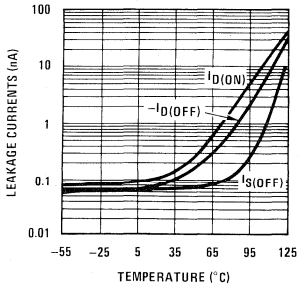
Switch Leakage Currents



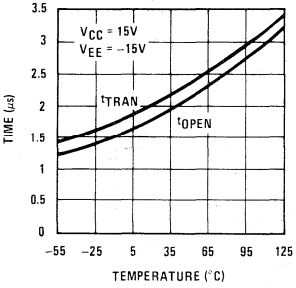
Switch Leakage Currents



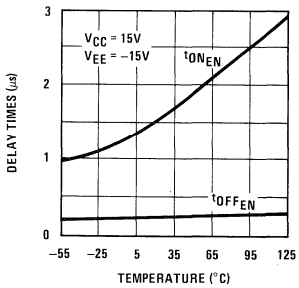
Switch Leakage Currents



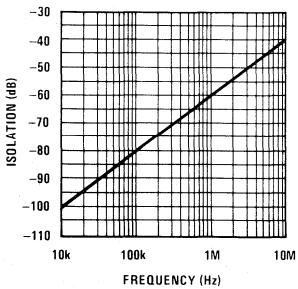
Switching Times (Figures 1 and 3)



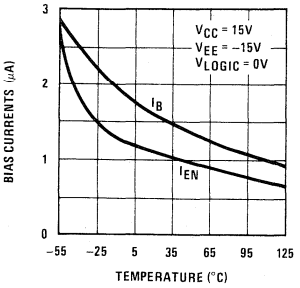
Enable Delay Times (Figure 2)



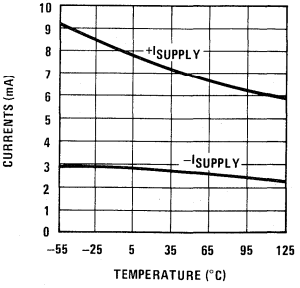
"OFF" Isolation and Crosstalk



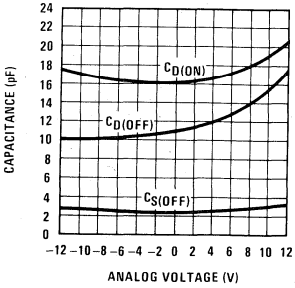
Bias Currents



Supply Currents



Switch Capacitances



Application Hints

The LF11508 series is an 8-channel analog multiplexer which allows the connection of a single load to 1 of 8 different analog inputs. These multiplexers incorporate JFETs in a switch configuration which insures a constant "ON" resistance over the analog voltage range of the device. Four TTL compatible inputs are provided; a 3-bit binary decode to select a particular channel and an enable input used as a package select. The switches operate with a break-before-make action preventing the temporary connection of 2 analog inputs during switching. Because these multiplexers are fabricated with the BI-FET process rather than CMOS, they do not require special handling.

The LF11509 series is a 4-channel differential multiplexer which allows two loads to be connected to 1 of 4 different pairs of analog inputs. The LF11509 series also has all the features of the LF11508.

ANALOG VOLTAGE AND CURRENT

The "ON" resistance, R_{ON}, of the analog switches is constant over a wide input range from positive (V_{CC}) supply to negative ($-V_{EE}$) supply.

The analog input should not exceed either positive or negative supply without limiting the current to less than 10 mA; otherwise the multiplexer may get damaged. For proper operation, however, the positive analog voltage should be kept equal to or less than $V_{CC} - 4V$ as this will increase the switch leakage in both "ON" and "OFF" state and it may also cause a false turn "ON" of a normally "OFF" switch. This limit applies over the full temperature range.

The maximum allowable switch "ON" voltage (the drop across the switch in the "ON" condition) is ±0.4V over temperature. If this number is to exceed the input current should be limited to 10 mA.

The "ON" resistance of the multiplexing switches varies slightly with analog current because they are JFETs running at 0V gate to source. The JFET characteristics shown in *Figure 4* indicates how R_{ON} tends to vary with current. A lower R_{ON} is possible when the source voltage is negative with respect to the drain voltage because the JFET becomes enhanced. Caution should be used when operating in this mode as this may forward-bias an internal transistor and cause high currents to flow in the switches. Thus, the drain voltage should never be greater than 0.4V positive with respect to the source voltage without limiting the drain current to less than 10 mA.

LEAKAGE CURRENTS

Leakage currents will remain within the specified value as long as the drain and source remain within the specified analog voltage range. As the switch terminals exceed the positive analog voltage range "ON" and "OFF" leakage currents increase. The "ON" leakage increases due to an internal clamp required by the switch structure. The "OFF" leakage increases because the gate to source reverse bias has been decreased to the point where the switch becomes active. Leakage currents vary slightly with analog voltage and will approximately double for every 10°C rise in temperature.

SWITCHING TIMES AND TRANSIENTS

These multiplexers operate with a break-before-make switch action. The turn off time is much faster than the turn on time to guarantee this feature over the full range of analog input voltage and temperature. Switching transients are introduced when a switch is turned "OFF". The amplitude of these transients may be reduced by increasing the load capacitance or decreasing the load resistance. The actual charge transfer in the transient may be reduced by operating on reduced power supplies. Examples of switching times and transients are shown in the typical characteristic curves. The enable function switching times are specified separately from switch-to-switch transition times and may be thought of as package-to-package transition times.

LOGIC INPUTS AND ENABLE INPUT

Switch selection in the LF11508 series is accomplished by using a 3-bit binary decode while the LF11509 series uses a 2-bit decode. These binary logic inputs are compatible with both TTL and CMOS logic voltage levels. The maximum positive voltage applied to these inputs may exceed V_{CC} but should not exceed $-V_{EE} + 36V$. The maximum negative voltage should not be less than 4V below ground as this will cause an internal device to zener and all the switches will turn "ON".

As shown in the schematic diagram, the logic low bias current will flow until the PNP input is raised above the 3 diode reference (≈ 2.1V). Above this voltage the input device becomes reverse biased and the input current drops to the leakage of the reverse biased junction (< 0.1 μA).

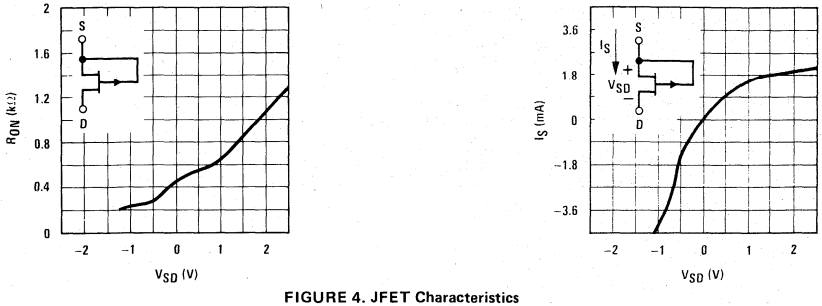


FIGURE 4. JFET Characteristics

Typical Applications

DATA ACQUISITION SYSTEM

A SIMPLIFIED SYSTEM DISCUSSION

Analog multiplexers (MUX) are usually used for multi-channel Data Acquisition Units (DAU). *Figure 5* shows a system in which 8 different analog inputs are sampled and converted into digital words for further processing. The sample and hold circuit is optional, depending on input speed requirements and on A/D converter speed.

Parameters characterizing the system are:

System Channels: The number of multiplexer channels.

Accuracy: The conversion accuracy of each individual sample with the system operating at the throughput rate.

Speed or Throughput Rate: Number of samples/second/channel the system can handle.

For a discussion on system structure, addressing mode and processor interfacing, see application note AN-159.

A. ACCURACY CONSIDERATIONS

1. Multiplexer's Influence on System Accuracy *(Figure 6)*.

   a. The error, (E), caused by the finite "ON" resistance, R_{ON}, of the multiplexing switches is given by:

   $$E(\%) = \frac{100}{1 + R_{IN}/(R_{ON} + R_S + \Delta R_{ON})}$$ where:

   R_{IN} = following stage input impedance

   ΔR_{ON} = "ON" resistance modulation which is negligible for JFET switches like the LF11508

   Example: Let R_{ON} = 450 Ω, ΔR_{ON} = 0, R_S = 0, T_A = 25°C and allowable E = 0.01% which is equivalent to 1/2 LSB in a 12-bit system:

   $$R_{IN}\Big|_{min} = \frac{R_{ON}\,(100-E)}{E} = 4.5\ M\Omega$$

   Note that if temperature effects are included, some gain (or full scale) drift will occur; but effects on linearity are small.

   b. Multiplexer settling time (t_s):

   $t_{s(ON)}$: is the time required for the MUX output to settle within a predetermined accuracy, as shown in Table I.

   C_S *(Figure 6):* MUX output capacitance + following stage input capacitance + any stray capacitance at this node.

TABLE I.

ERROR %	BITS	$t_{s(ON)}$ TO 1/2 LSB
0.2	8	6.2t
0.05	10	7.6t
0.01	12	9t
0.0008	16	11.8t

$t = C_S\,(R_{ON} + R_S)\|R_{IN}$

$t_{s(OFF)}$: is the time it takes to discharge C_S within a tolerable error. The "OFF" settling time should be taken into account for bipolar inputs where its effects will appear as a worse case doubling of the $t_{s(ON)}$.

2. Sample and Hold Influence on System Accuracy

   The sample and hold, if used, also introduces errors into the system accuracy due to:

   - Offset voltage of sample and hold
   - Droop rate in the Hold mode
   - T_A: Aperture time or time delay between the time of a digital Hold command and the actual Hold occurance
   - Taq: Acquisition time or time it takes to acquire an analog input and settle within a predetermined error band
   - Hold step: Error created during the Sample to Hold mode caused by an undesirable charge injected into the Hold capacitor C_h.

   For more details on sample and hold errors, see the LF198/LF298/LF398 data sheet.

3. A/D Converter Influence on System Accuracy

   The "accuracy" of the A/D converter is the best possible system accuracy. In most data acquisition systems, the A/D converter is the most expensive single component, so its error will often dominate system error. Care should be taken that MUX, S/H and input source errors do not exceed system error requirements when *added* to A/D errors. For instance, if an 8-bit accuracy system is desired and an 8-bit A/D converter is used, the accuracy of the MUX and S/H should be far better than 8 bits.

For details on A/D converter specifications, see AN-156.

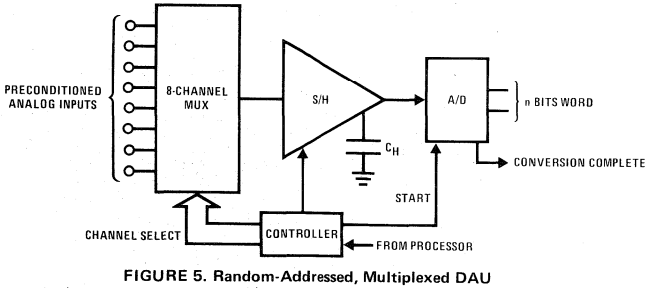


FIGURE 5. Random-Addressed, Multiplexed DAU

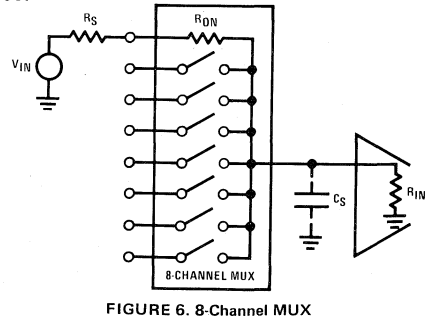


FIGURE 6. 8-Channel MUX

Typical Applications (Continued)

B. SPEED CONSIDERATIONS

In the system of *Figure 5* with the S/H omitted, if n-bit accuracy is desired, the change of the analog input voltage should be less than ±1/2 LSB over the A/D conversion time T_C. In other words, the analog input slew rate, (rate of change of input voltage), will cause a slew-induced error and its magnitude, with respect to the total system error, will depend on the particular application.

$$\left.\frac{\Delta V_{IN}}{\Delta t}\right|_{max} < \frac{\pm 1/2\ LSB}{T_C} = \frac{V_{FS}}{2^n \times T_C}$$

where V_{FS} is the full scale voltage of the A/D. Note that slew induced errors are not affected by the MUX switch time since we can let the unit settle before starting conversion.

Example: Let T_C = 40 μs (MM4357), V_{FS} = 10V and n = 8.

$$\left.\frac{\Delta V_{IN}}{\Delta t}\right|_{max} < \frac{1\ mV}{\mu s}$$

which is a very small number. A 10 Vp-p sine wave of a frequency greater than 32 Hz will have higher slew rate than this. The maximum throughput rate of the above 8-channel system would be calculated using both the A/D conversion time and the sum of MUX switch "ON" time and settling time, i.e.:

$$\text{Th. R}\Big|_{max} = \frac{1}{8\ (T_C + T_{MUX})} = \text{3k samples/sec/channel}$$

$$T_{MUX} = T_{ON} + T_{S(ON)}$$

Also notice that Nyquist sampling criteria would allow each channel to have a signal bandwidth of 1.5 kHz max, while the slew limit dictates a maximum frequency of 32 Hz. If the input signal has a peak-to-peak voltage less than 10V, the allowable maximum input frequency can be calculated by:

$$f_{MAX} = \frac{(\text{Slew Rate})_{max}}{\pi\ V_{p\text{-}p}}$$

On the other hand, if the input voltage is not band-limited a low pass filter with an attenuation of 30 dB or better at 1.5 kHz, should be connected in front of the MUX.

1. Improving System Speed with a Sample and Hold

The system speed can be improved by using the S/H shown in *Figure 5*. This allows a much greater rate of change of V_{IN}.

$$\left.\frac{\Delta V_{IN}}{\Delta t}\right|_{max} < \frac{V_{FS}}{2^n \times T_A}$$

where T_A is the aperture time of the S/H. This represents an input slew rate improvement by a factor: T_C/T_A. Here again, the slew rate error is not affected by the acquisition time of the Sample and Hold since conversion will start after the S/H has settled. *An important thing to notice is that the sample and hold errors will add to the total system error budget; therefore, the inequality of the $\Delta V_{IN}/\Delta t$ expression should become more stringent.*

Example: T_C = 40 μs, T_A=0.5 μs, n = 8: T_C/T_A = 80

So the use of a S/H allows a speed improvement by nearly two orders of magnitude.

The maximum throughput rate can be calculated by:

$$\text{Th. R}\Big|_{max} = \frac{1}{8\ (T_A + Taq + T_C)}$$

Notice that T_{MUX} does not affect the $\Delta V_{IN}/\Delta t$ expression *nor the throughput rate* of the system since it may be switched and settled while the Sample and Hold is in the Hold mode. This is true, provided that: $T_{MUX} < T_A + T_C$.

C. SYSTEM EXAMPLE *(Figure 7)*

The LF398 S/H with a 1000 pF hold capacitor, has an acquisition time of 4 μs to 0.1% (1/4 LSB error for 8 bits) and an aperture time of less than 200 μs. On the other hand, after the hold command, the output will settle to ±0.05 mV in 1 μs. This, together with the acquisition time, introduces approximately a ±1/4 LSB error. Allowing another 1/4 LSB error for hold step and gain non-linearity, the maximum slew error ($\Delta V_{IN}/\Delta t$) should not exceed 1/4 LSB or:

$$\frac{\Delta V_{IN}}{\Delta t} \leq \frac{1}{4} \times \frac{1}{256} \times \frac{1}{T_A} \approx 5\ mV/\mu s$$

(which is the maximum slew rate of a 5 V peak sine wave. Also notice that, due to the above input slew restrictions, the analog delay caused by the finite BW of the S/H and the digital delay caused by the response time of the controller will be negligible. The maximum throughput rate of the system is:

$$\text{Th. R}\Big|_{max} = \frac{1}{8\ (5 + 40)\ 10^{-6}} = \text{2800 samples/sec/ch.}$$

If the system speed requirements are relaxed, but the A/D converter is still too slow, then an inexpensive S/H can be built by using just a capacitor and a low cost FET input op amp as shown in *Figure 8.*

Typical Applications (Continued)

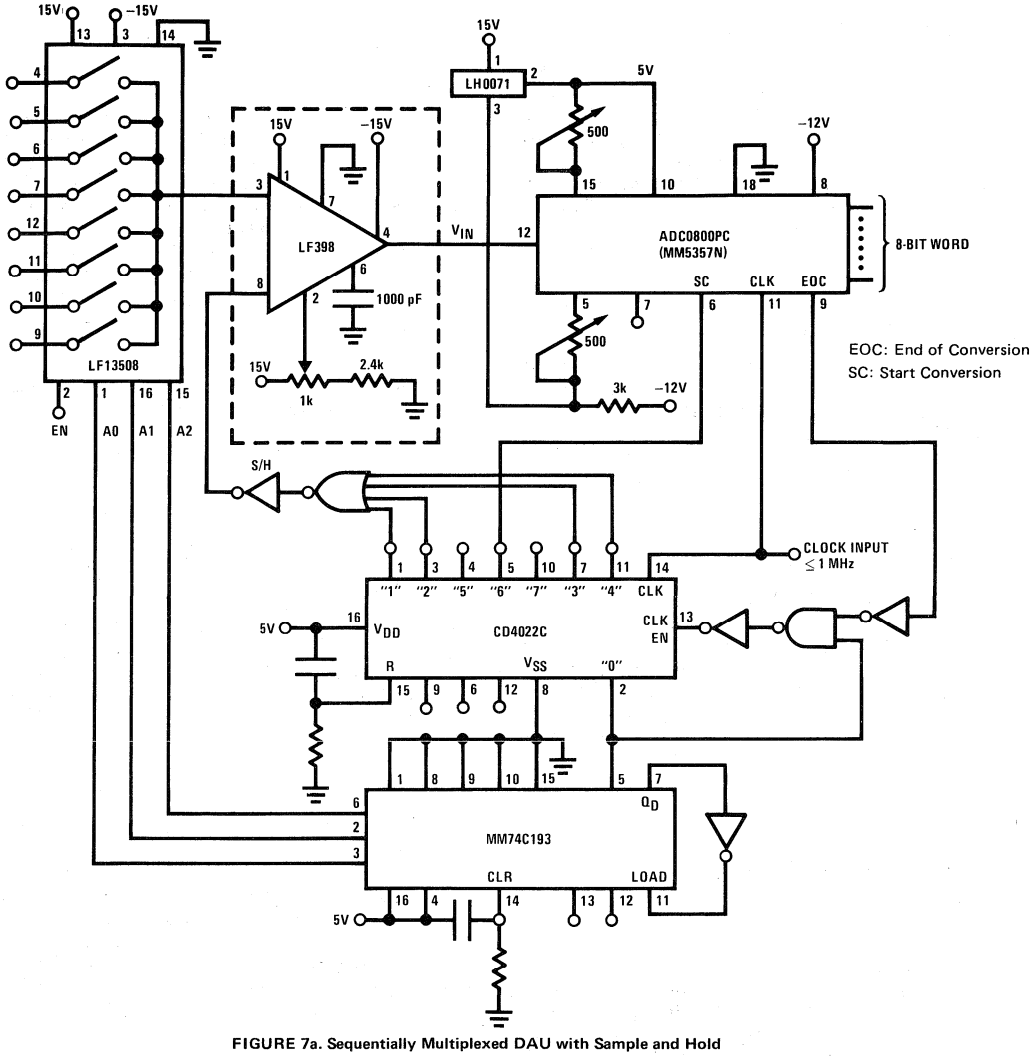


FIGURE 7a. Sequentially Multiplexed DAU with Sample and Hold

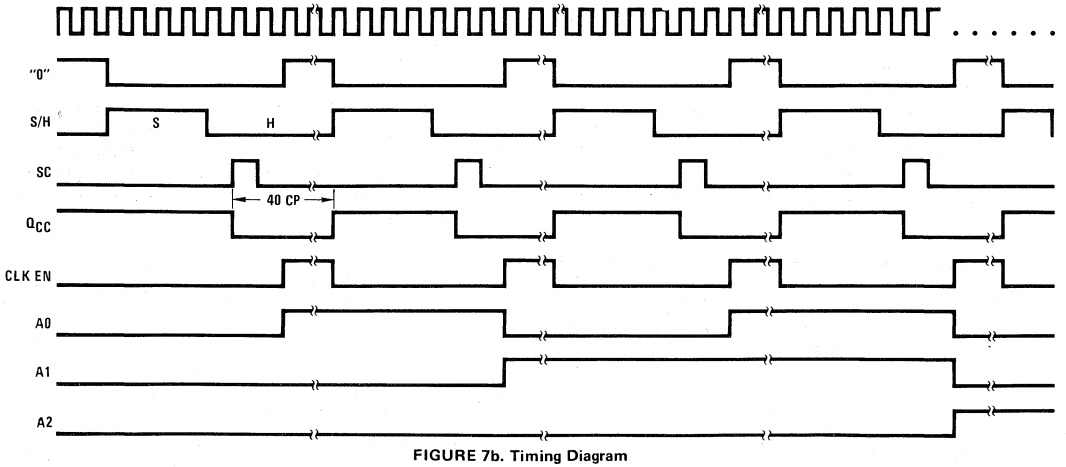


FIGURE 7b. Timing Diagram

Typical Applications (Continued)

D. DOUBLING THE SYSTEM CHANNEL CAPABILITY

This is done in two different ways. First, we can use second level multiplexing with speed benefits, as shown in *Figure 9*. A fast 2-channel multiplexer, made by the dual analog switch AM182, accepts the outputs of each 8-channel MUX, LF13508, and then feeds them sequentially into an 8-bit successive approximation A/D converter. With this technique, the throughput rate of the system can again be made independent of the the LF13508 speed. Looking at the timing diagram, when the A/D converter converts the analog value of an upper multiplexer channel, we switch channels in the lower multiplexer for the next conversion. This can be done provided that:

$$T_{MUX} \leq T_C + 1\ CP$$

The LF356 connected as unity gain buffers are used because of the low input impedance of the A/D; they are connected between multiplexers for speed optimization. With a maximum clock frequency of 4.5 MHz:

$$\text{Th. R} = \frac{10^6}{16 \times 2} = 31.25\text{k samples/sec/channel}$$

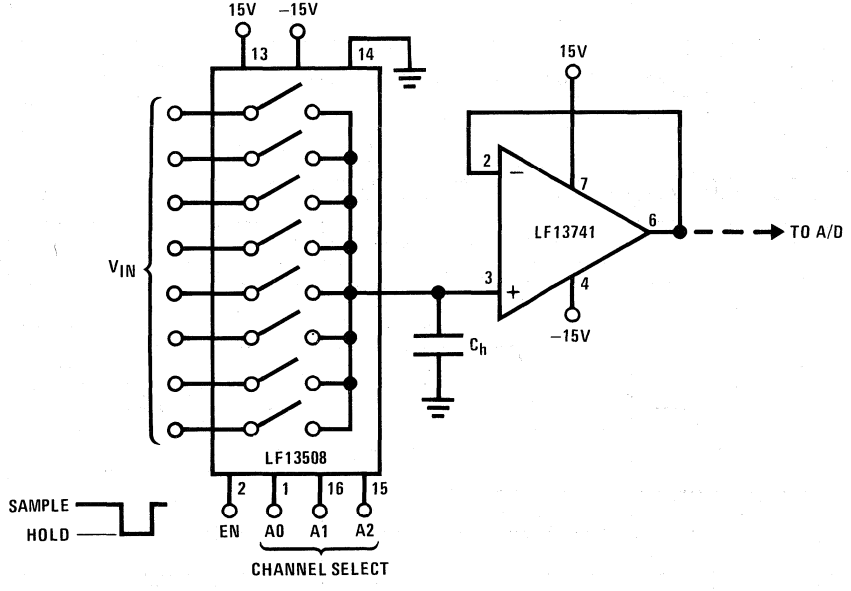
and

$$\left.\frac{\Delta V_{IN}}{\Delta t}\right|_{max} < \frac{10}{256} \times \frac{1}{2\ \mu s} = 19.5\ mV/\mu s \text{ for } 10V_{FS}$$

An alternate way to increase the system channel is shown in *Figure 10*, where the enable pins are used to disable one MUX while the other is sampling. With this method, many 8-channel multiplexers can be connected, but the parasitic capacitance at the common output node will keep increasing and will eventually degrade the settling time, $t_s(ON)$. Also, the MUX speed will now affect the system throughput. If, for instance, this method was used instead of second level multiplexing, the system of *Figure 9* will lose half of its speed. If, however, speed is not the prime system requirement, the approach of *Figure 10* is more cost effective.

E. DIFFERENTIAL INPUT SYSTEMS

Systems operating in industrial environments may require an instrumentation amplifier to separate the desired analog signal from any common-mode signal present. The LF11509 was designed to provide 4 pairs of differential input signals to the input of an instrumentation amplifier for further process. A 4-channel preconditioning circuit is shown in *Figure 11* and a complete system is shown in *Figure 12*.



- The acquisition time, T_A, of the Sample and Hold depends upon: R_{ON}, I_{DSS} of switches, Z_{OUT} of switches
- $I_{DSS} \cong 1.5$ mA, $Z_{OUT} = 40$ kΩ
- $V_{IN} = 10V$, $C_h = 1000$ pF, $T_A = 20\ \mu s$ to 0.1%
- Error created by charge injection during Hold mode: $\Delta V_E \simeq 10\ pF\ (14.5V - V_{IN})/C_h$

FIGURE 8. Inexpensive Sample and Hold

Typical Applications (Continued)

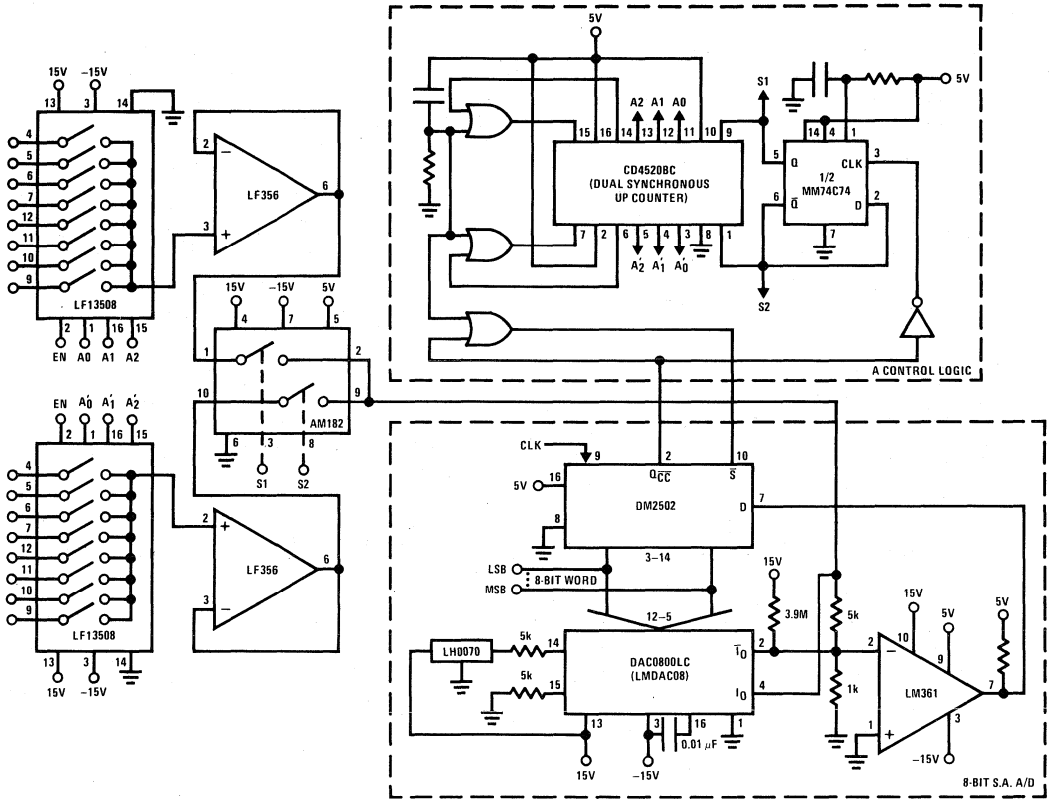


FIGURE 9a. A Fast 16-Channel DAU with Second Level Multiplexing

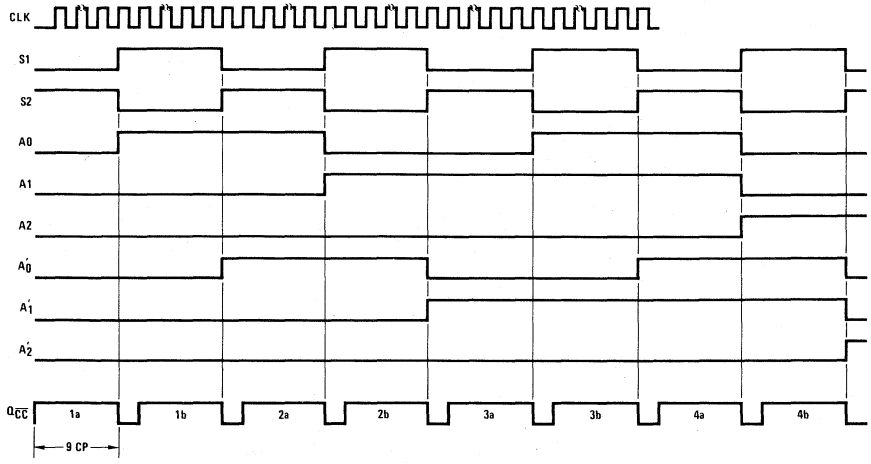


FIGURE 9b. Timing Diagram

Typical Applications (Continued)

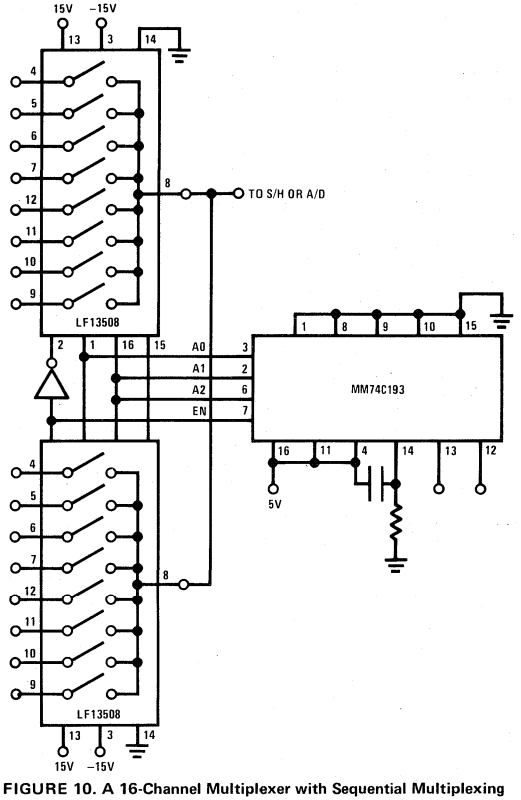
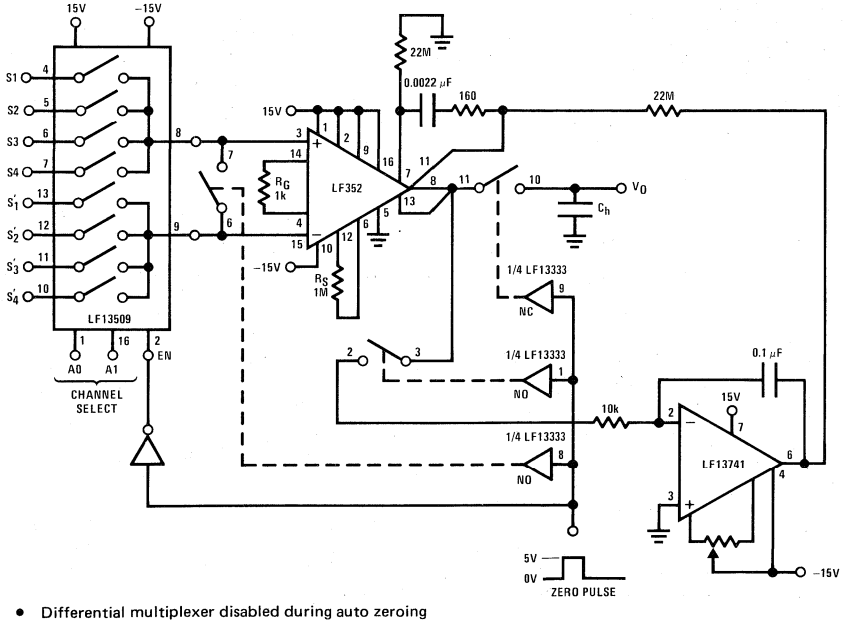


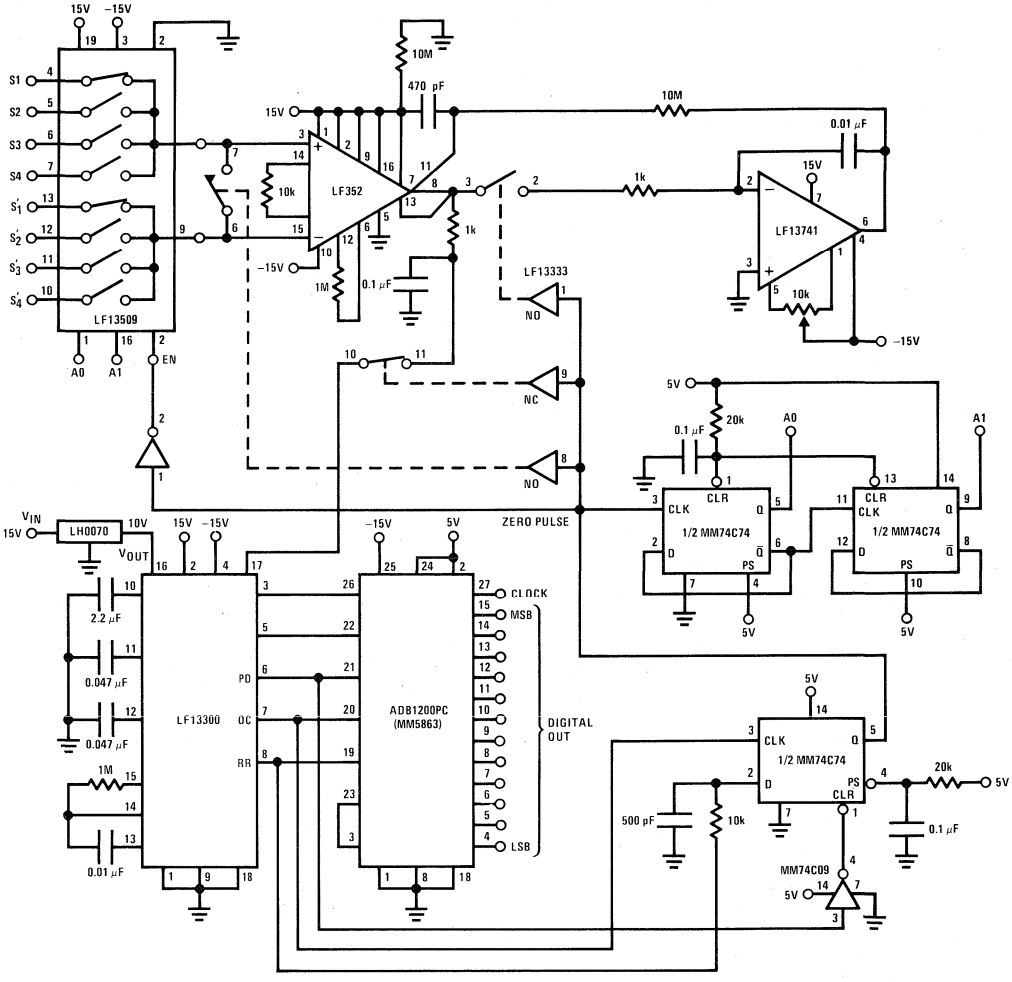
FIGURE 10. A 16-Channel Multiplexer with Sequential Multiplexing



- Differential multiplexer disabled during auto zeroing
- Minimum zeroing pulse width will depend upon the integrator R1C
- This scheme provides input offset adjust especially useful with high gain connections. The device, LF352, provides pins for output offset adjust. For more details, see LF352 data sheet.

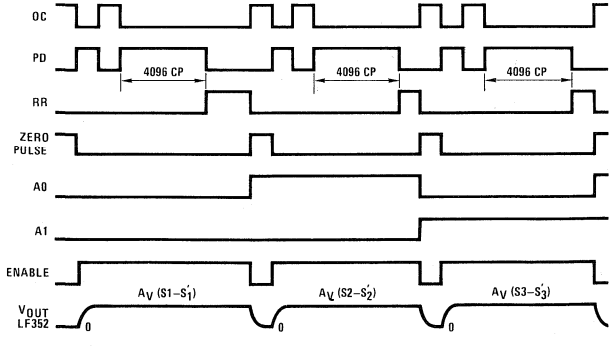
FIGURE 11. 4-Channel Differential Multiplexer with Auto Zeroed Instrumentation Amplifier

Typical Applications (Continued)



- f_{CLOCK} max = 200 kHz
- The LF352 instrumentation amplifier is auto zeroed during offset correction cycle of the LF13300 A/D
- The system accuracy will mostly depend on the instrumentation amplifier gain linearity

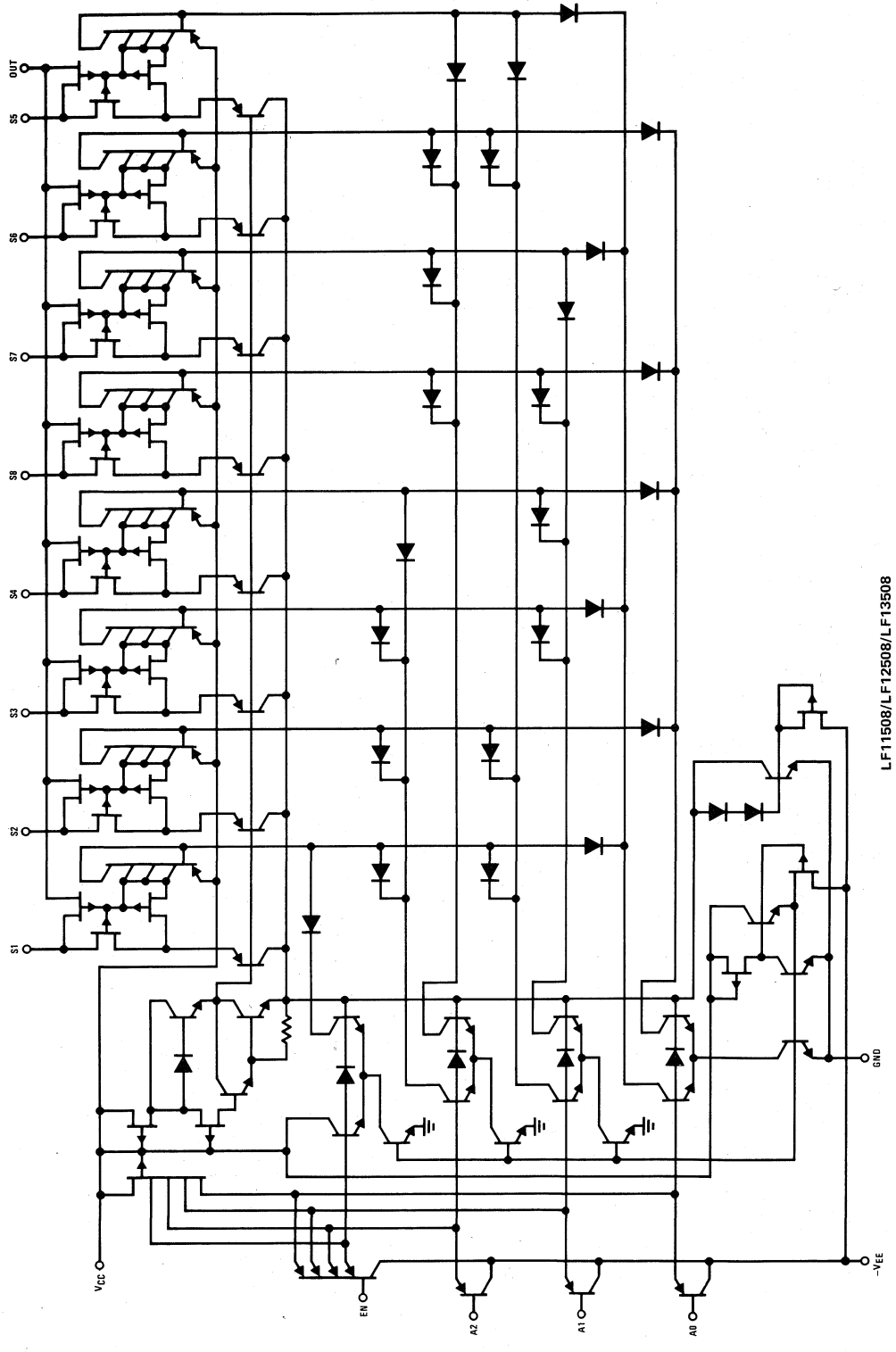
FIGURE 12a. 4-Channel Differential Multiplexer with Auto Zeroed Instrumentation Amplifier and 12-Bit A/D Converter



PD: Polarity Detection
OC: Offset Correction
RR: Ramp Reference
For more details, see LF13300 data sheet

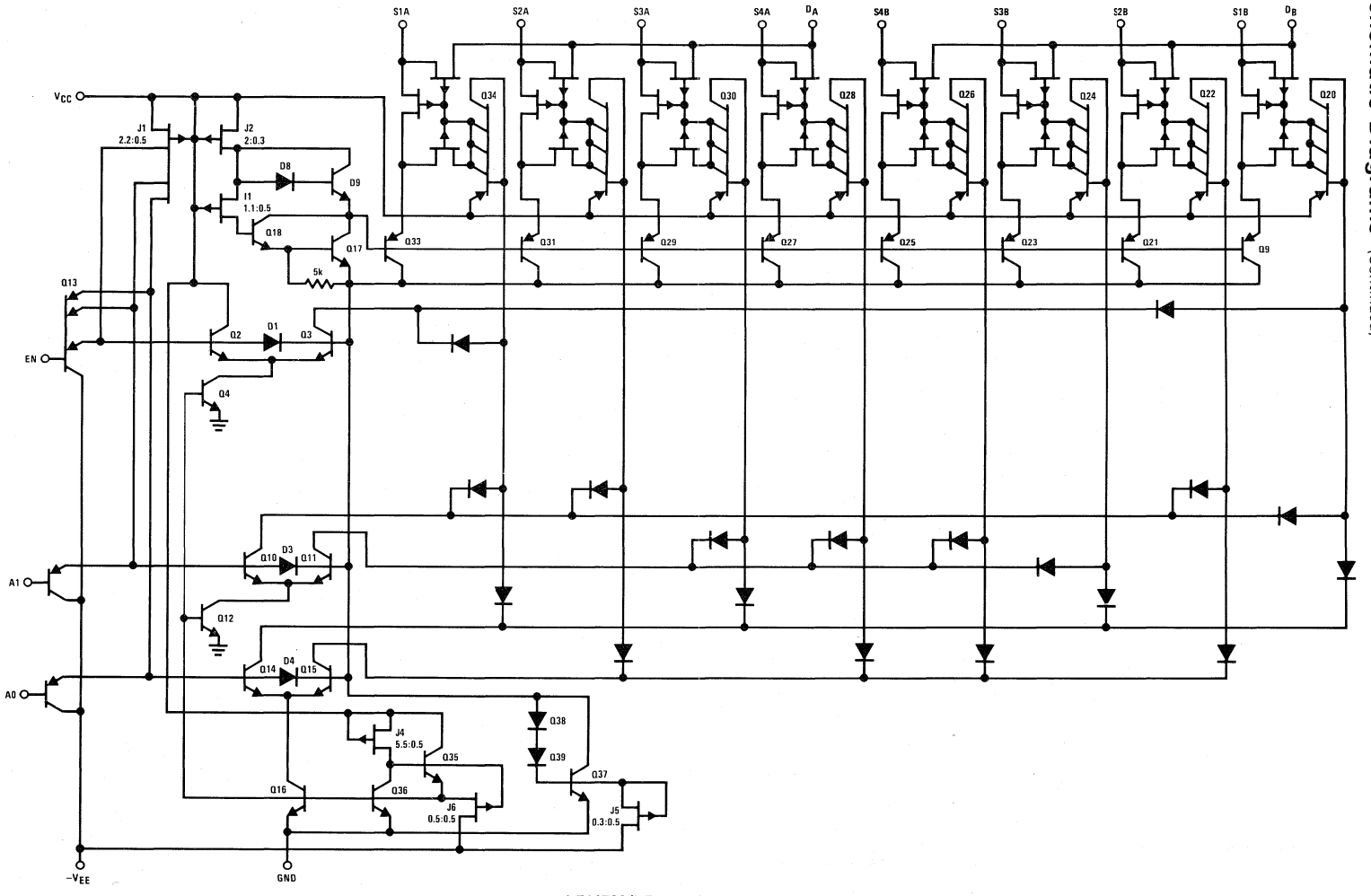
FIGURE 12b. System Timing Diagram for Differential MUX

Schematic Diagrams



LF11508/LF12508/LF13508

Schematic Diagrams (Continued)



LF11509/LF12509/LF13509

MM450/MM550, MM451/MM551, MM452/MM552, MM455/MM555 MOS Analog Switches

General Description

The MM450, and MM550 series each contain four p channel MOS enhancement mode transistors built on a single monolithic chip. The four transistors are arranged as follows:

MM450, MM550	Dual Differential Switch
MM451, MM551	Four Channel Switch
MM452, MM552	Four MOS Transistor Package
MM455, MM555	Three MOS Transistor Package

These devices are useful in many airborne and ground support systems requiring multiplexing, analog transmission, and numerous signal routing applications. The use of low threshold transistors (V_{TH} = 2 volts) permits operations with large analog input swings (± 10 volts) at low gate voltages (−20 volts). Significant features, then, include:

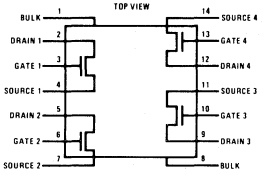
- Large Analog Input Swing ±10 Volts
- Low Supply Voltage V_{BULK} = +10 Volts, V_{GG} = −20 Volts
- Low ON Resistance V_{IN} = −10V 150Ω, V_{IN} = +10V 75Ω
- Low Leakage Current 200 pA @ 25°C
- Input Gate Protection
- Zero Offset Voltage

Each gate input is protected from static charge build-up by the incorporation of zener diode protective devices connected between the gate input and device bulk.

The MM450, MM451, MM452 and MM455 are specified for operation over the −55°C to +125°C military temperature range. The MM550, MM551, MM552 and MM555 are specified for operation over the −25°C to +70°C temperature range.

Schematic and Connection Diagrams

Dual-In-Line and Flat Package

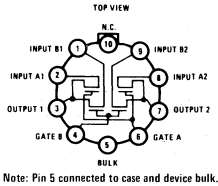


Note 1: Pins 1 and 8 connected to case and device bulk. Drain and Source may be interchanged. MM452F, MM552F.

Note 2: MM452D and MM552D (dual-in-line packages) have same pin connections as MM452F and MM552F shown above.

Order Number MM452F or MM552F
See Package 23
Order Number MM452D or MM552D
See Package 14

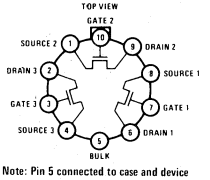
Metal Can Package



Note: Pin 5 connected to case and device bulk.

Order Number MM450H or MM550H
See Package 1

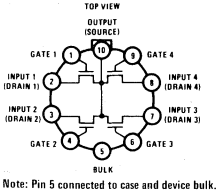
Metal Can Package



Note: Pin 5 connected to case and device bulk. Drain and Source may be interchanged.

Order Number MM455H or MM555H
See Package 1

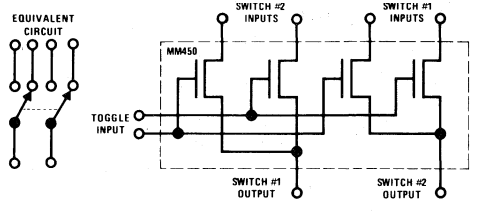
Metal Can Package



Note: Pin 5 connected to case and device bulk.

Order Number MM451H or MM551H
See Package 1

Typical Applications



DPDT Analog Switch

Absolute Maximum Ratings

	MM450, MM451, MM452, MM455	MM550, MM551, MM552, MM555
Gate Voltage (V_{GG})	+10V to −30V	+10V to −30V
Bulk Voltage (V_{BULK})	+10V	+10V
Analog Input (V_{IN})	+10V to −20V	+10V to −20V
Power Dissipation	200 mW	200 mW
Operating Temperature	−55°C to +125°C	−25°C to 70°C
Storage Temperature	−65°C to +150°C	−65°C to +150°C

Electrical Characteristics

STATIC CHARACTERISTICS (Note 1)

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Analog Input Voltage				±10	V
Threshold Voltage ($V_{GS(T)}$)	V_{DG} = 0, I_D = 1 μA	1.0	2.2	3.0	V
ON Resistance	V_{IN} = −10V		150	600	Ω
ON Resistance	V_{IN} = V_{SS}		75	200	Ω
OFF Resistance			10^{10}		Ω
Gate Leakage Current (I_{GSB})	V_{GS} = −25V, V_{BS} = 0, T_A = 25°C		20		pA
Input (Drain) Leakage Current					
MM450, MM451, MM452, MM455	T_A = 25°C		.025	100	nA
	T_A = 85°C		.002	1.0	μA
	T_A = 125°C		.025	1.0	μA
Input (Drain) Leakage Current					
MM550, MM551, MM552, MM555	T_A = 25°C		0.1	100	nA
	T_A = 70°C		.030	1.0	μA
Output (Source) Leakage Current					
MM450, MM451, MM452, MM455	T_A = 25°C		.040	100	nA
Output (Source) Leakage Current					
MM450	T_A = 85°C			1.0	μA
MM451	T_A = 85°C			1.0	μA
MM452, MM455	T_A = 85°C			1.0	μA
MM450, MM451, MM452, MM455	T_A = 125°C			1.0	μA
Output (Source) Leakage Current					
MM550	T_A = 70°C			1.0	μA
MM551	T_A = 70°C			1.0	μA
MM552, MM555	T_A = 70°C			1.0	μA
DYNAMIC CHARACTERISTICS					
Large Signal Transconductance	V_{DS} = −10V, I_D = 10 mA f = 1 kHz		4000		μmhos

CAPACITANCE CHARACTERISTICS (Note 2)

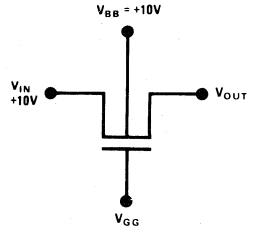
PARAMETER	DEVICE TYPE	MIN	TYP	MAX	UNITS
Analog Input (Drain) Capacitance (C_{DB})	ALL		8	10	pF
Output (Source) Capacitance (C_{SB})	MM450, MM550		11	14	pF
	MM451, MM551		20	24	pF
	MM452, MM552		7.5	11	pF
	MM455, MM555		7.5	11	pF
Gate Input Capacitance (C_{GB})	MM450, MM550		10	13	pF
	MM451, MM551		5.5	8	pF
	MM452, MM552		5.5	9	pF
	MM455, MM555		5.5	9	pF
Gate to Output Capacitance (C_{GS})	ALL		3.0	5	pF

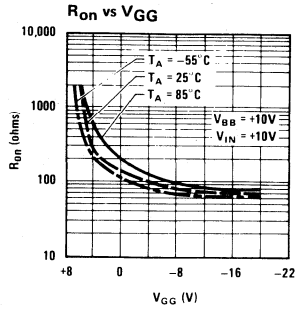
Note 1: The resistance specifications apply for $-55°C \leq T_A \leq +85°C$, V_{GG} = −20V, V_{BULK} = +10V, and a test current of 1 mA. Leakage current is measured with all pins held at ground except the pin being measured which is biased at −25V.

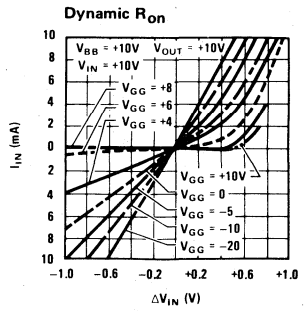
Note 2: All capacitance measurements are made at 0 volts bias at 1 MHz.

Typical Dynamic Input Characteristics (T_A = 25°C Unless Otherwise Noted)

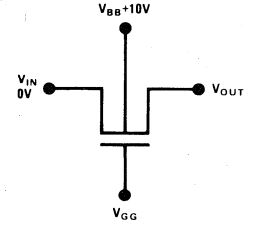
CONDITION 1:
ANALOG INPUT VOLTAGE
AT +10 VOLTS

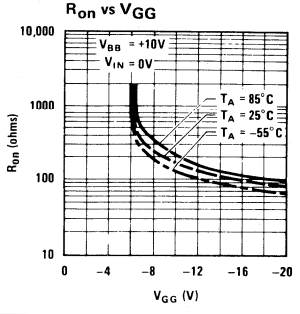


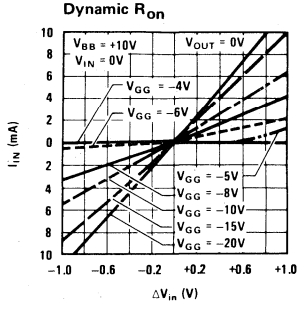




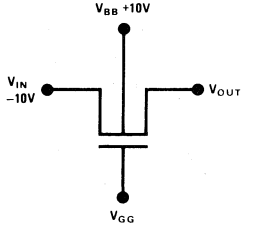
CONDITION 2:
ANALOG INPUT VOLTAGE
AT 0 VOLTS

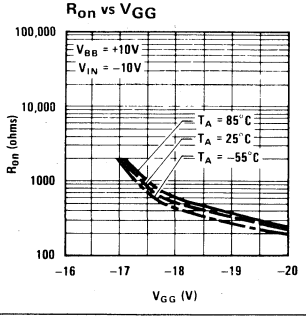


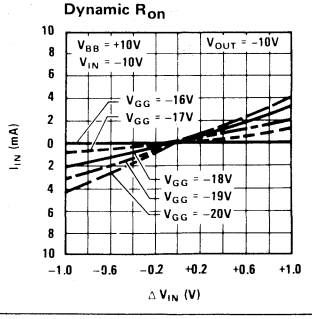


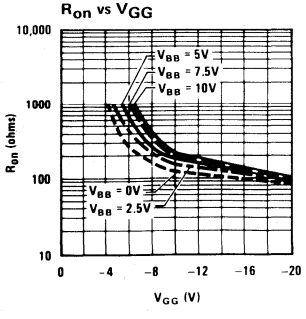


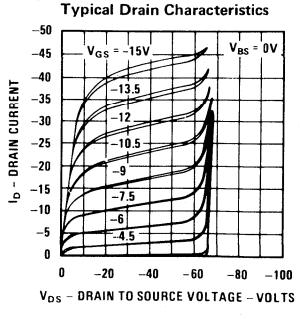
CONDITION 3:
ANALOG INPUT VOLTAGE
AT −10 VOLTS

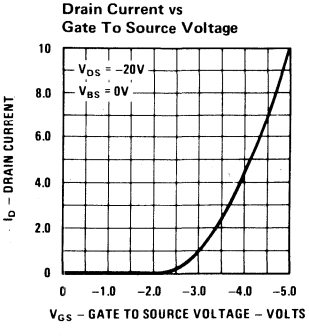






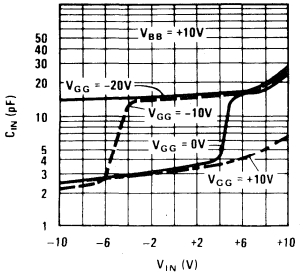




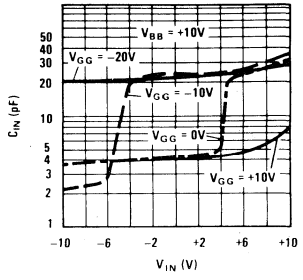


Typical Input Capacitance Characteristics

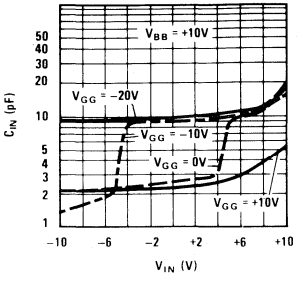
MM450, MM550
C_{IN} vs V_{IN}



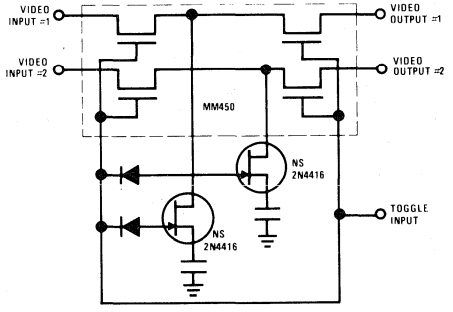
MM451, MM551
C_{IN} vs V_{IN}



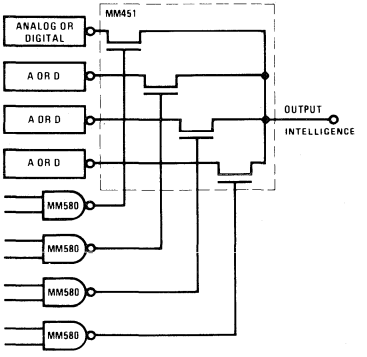
MM452, MM552, MM455, MM555
C_{IN} vs V_{IN}



Typical Applications (Continued)



DPST High-Frequency Switch



4-Channel Multiplexer*

*Expansion in the number of data input lines is possible by using multiple level series switches allowing the same decode gates to be used for all lower rank decoding.

MM454/MM554 4-Channel Commutator

General Description

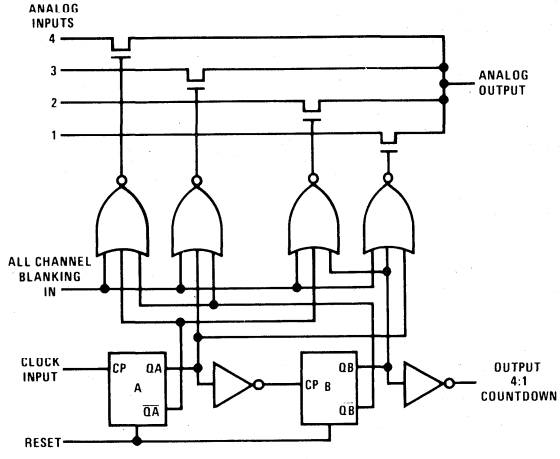
The MM454/MM554 is a 4-channel analog commutator capable of switching four analog input channels sequentially onto an output line. The device is constructed on a single silicon chip using MOS P Channel enhancement transistors; it contains all the digital circuitry necessary to sequentially turn ON the four analog switch transistors permitting multiplexing of the analog input data. The device features:

- High Analog Voltage Handling ±10V
- High Commutating Rate 500 kHz
- Low Leakage Current (T_A = 25°C) 200 pA
  (T_A = 85°C) 50 nA
- All Channel Blanking input provided
- Reset capability provided
- Low ON Resistance 200Ω

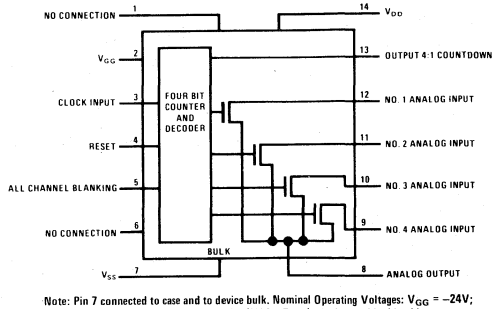
In addition, the MM454/MM554 can easily be applied where submultiplexing is required since a 4:1 clock countdown signal is provided which can drive the clock input of subsequent MM454/MM554 units.

The MM454 is specified for operation over the −55°C to +125°C military temperature range. The MM554 is specified for operation over the −25°C to +70°C temperature range.

Schematic and Connection Diagrams



Flat Package



Note: Pin 7 connected to case and to device bulk. Nominal Operating Voltages: V_{GG} = −24V; V_{DD} = 0V; V_{SS} = +12V, Reset Bias = +12V (0V for Reset), all channel blanking bias = +12V (0V for blanking)

Order Number MM454F or MM554F
See Package 23

Absolute Maximum Ratings (Note 1)

Gate Voltage (V_{GG})		+10V to −30V
Bulk Voltage (V_{SS})		+10V
Analog Input (V_{IN})		+10V to −20V
Power Dissipation		200 mW
Operating Temperature	MM454	−55°C to +125°C
	MM554	−25°C to +70°C
Storage Temperature		−65°C to +150°C

Static Characteristics (Note 2)

PARAMETER		CONDITION	MIN	TYP	MAX	UNITS
Analog Input Voltage					±10	V
ON Resistance		V_{IN} = −10V		170	600	Ω
ON Resistance		V_{IN} = V_{SS}		90	200	Ω
OFF Resistance				10^{10}		Ω
Analog Input Leakage Current	MM454	T_A = 25°C		.050	100	nA
	MM454	T_A = 85°C		.006	1.0	μA
	MM554	T_A = 25°C		.0001	100	nA
	MM554	T_A = 70°C		.030	1.0	μA
Analog Output Leakage Current	MM454	T_A = 25°C		0.100	100	nA
	MM454	T_A = 85°C		30	1.0	μA
	MM554	T_A = 25°C		.0001	100	nA
	MM554	T_A = 70°C		.030	1.0	μA
V_{SS} Supply Current Drain		V_{SS} = +12V		3.8	5.5	mA
V_{GG} Supply Current Drain		V_{GG} = −24V		2.4	3.5	mA

Capacitance Characteristics

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Analog Input Capacitance Channel OFF	I_{IN} = 0		4	6	pF
Analog Input Capacitance Channel ON	I_{IN} = 0		20	24	pF
Analog Output Capacitance	I_{IN} = 0		20	24	pF
Clock Input	V_{CL} = +12V		2.0		pF
Reset Input	V_{RESET} = +12V		2.0		pF
Blanking Input	V_{BLANK} = +12V		2.0		pF

Clock Characteristics (Note 3)

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Clock Input (HIGH)[4]		V_{SS} − 2		V_{SS}	V
Clock Input (LOW)		−5	0	+5	V
Clock Input Rise Time (POS GOING)		No requirement			
Clock Input Fall Time (NEG GOING)				20	μsec
Countdown Output (POS) V_{OH}		V_{SS} −2		V_{SS}	V
Countdown Output (NEG) V_{OL}			0		V
Maximum Commutation Rate		0.5	2.0		MHz
V_{SS}		+10.0	+12	+14	V

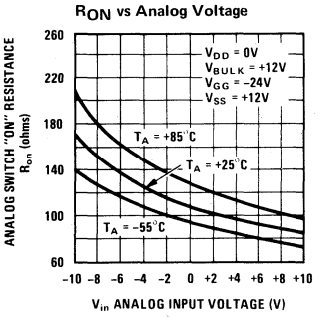
Note 1: Maximum ratings are limiting values above which the device may be damaged. All voltages referenced to V_{DD} = 0.

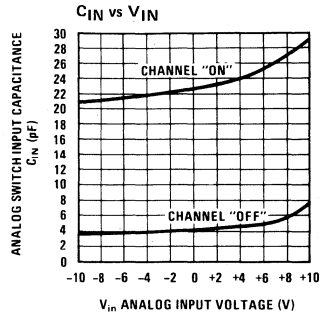
Note 2: These specifications apply over the indicated operating temperature range for V_{GG} = −24V, V_{DD} = 0V, V_{SS} = +12V, V_{RESET} = +12V, V_{BLANK} = +12V. ON resistance measured at 1 mA, OFF resistance and leakage measured with all analog inputs and output common. Capacitance measured at 1 MHz.

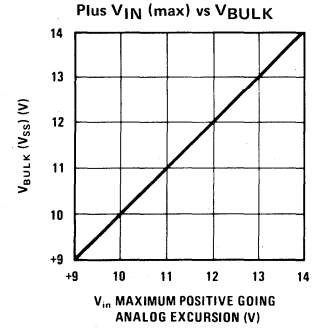
Note 3: Operating conditions in Note 2 apply. V_{SS} to V_{DD} (0V) voltage is applied to counting and gating circuits. V_{GG} is required only for analog switch biasing. All logic inputs are high resistance and are essentially capacitive.

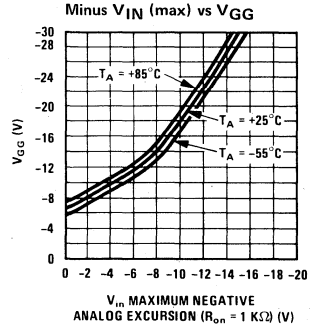
Note 4: Logic input voltage must not be more positive than V_{SS}.

Typical Performance Characteristics

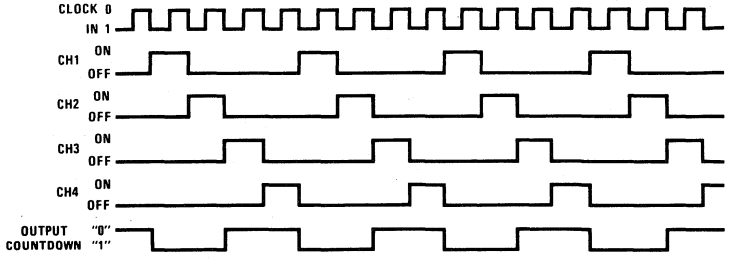








Timing Diagram



NOTE: "0" LEVEL = +12V
"1" LEVEL = 0V (GND)

Section 6

Applications

6

FET Application Guide

National Semiconductor manufactures a broad line of silicon Junction Field Effect Transistors (JFETs). National's JFETs provide excellent performance in many areas such as RF amplifiers, analog switching, low input current amplifiers, ultra low noise amplifiers and outstanding matched duals for operational amplifiers input applications.

The following chart is a guide to enable the user to determine what parameters are important in each application.

APPLICATIONS AND THEIR PARAMETERS LISTED IN APPROXIMATE ORDER OF IMPORTANCE

LOW FREQUENCY AMPLIFIER	SOURCE FOLLOWER	ELECTROMETER AMPLIFIERS	LOW DRIFT AMPLIFIER	LOW NOISE AMPLIFIER	HIGH FREQUENCY AMPLIFIER	OSCILLATOR	DIFFERENTIAL AMPLIFIER	ANALOG AND DIGITAL SWITCHING
Y_{fs}	Y_{fs}	I_G	I_{DZ}	e_n	$Re(Y_{fs})$	Y_{fs}	$\lvert V_{GS1}-V_{GS2}\rvert$	$r_{DS(ON)}$
I_{DSS}	I_G	Y_{fs}	Y_{fs} @ I_{DZ}	I_G, i_n	$Re(Y_{is})$	I_{DSS}	$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	$I_{D(OFF)}$
$V_{GS(OFF)}$	C_{rss}	I_{DZ}	V_{GS} @ I_{DZ}	Y_{fs}	NF	C_{rss}		C_{iss}
C_{iss}	C_{iss}	e_n	I_G	I_{DSS}	C_{rss}	C_{iss}	$\lvert I_{G1}-I_{G2}\rvert$	C_{rss}
C_{rss}	I_{DSS}	g_{os}	BV_{GSS}	$V_{GS(OFF)}$	$Re(Y_{os})$	$V_{GS(OFF)}$	I_G	$V_{GS(OFF)}$
e_n	$V_{GS(OFF)}$				I_{DSS}	BV_{GSS}	Y_{fs}	BV_{GSS}
BV_{GSS}	BV_{GSS}				$V_{GS(OFF)}$		Y_{fs1}/Y_{fs2}	
							$\lvert Y_{os1}-Y_{os2}\rvert$	
							CMRR	
							$V_{GS(OFF)}$	

JFET Parameter Relationships

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_{GS(OFF)}}\right)^2$$

Variation of drain current with gate bias. Square low transfer characteristic.

$$V_{GS(OFF)} = \frac{2\,I_{DSS}}{g_{fso}}$$

Gate-source cutoff voltage in terms of I_{DSS} and g_{fso}.

$$V_{GS}=V_{GS(OFF)}\left(1-\left(\frac{I_D}{I_{DSS}}\right)^{1/2}\right)$$

Gate-source voltage in terms of operating current I_D, I_{DSS}, and $V_{GS(OFF)}$.

$$g_{fso} = K\,\frac{I_{DSS}}{V_{GS(OFF)}}$$

Transconductance at zero gate voltage in terms of I_{DSS} and $V_{GS(off)}$. K = 1.1 to 2.5. Typically 2 for N-channel JFETs.

$$g_{fs} = g_{fso}\left(1-\frac{V_{GS}}{V_{GS(OFF)}}\right)$$

Variation in transconductance with gate bias.

$$g_{fs} = g_{fso}\sqrt{I_D/I_{DSS}}$$

Variation in transconductance with drain current.

$$r_{DS} \approx \frac{1}{g_{fs}}$$

Relationship between r_{DS} and g_{fs} in the triode region (i.e., $V_{DS} < V_{GS(OFF)}$).

$$r_{DS} \approx \frac{r_{DS(0)}}{1-\frac{V_{GS}}{V_{GS(OFF)}}}$$

Variation of drain resistance with gate bias in terms zero bias resistance (r_{DSO}) and $V_{GS(OFF)}$.

$$r_{DS} \approx \frac{K\,V_{GS(OFF)}^2}{I_{DSS}(V_{GS(OFF)}-V_{GS})}$$

K = 0.5 – 0.9

Variation of drain resistance in terms of V_{GS}, and $V_{GS(OFF)}$ I_{DSS}.

$$r_{DST} \approx r_{DS}\,@\,25^\circ C\,(1 + 0.007\,(\Delta T))$$

Variation of ON resistance as a function of temperature.

Monolithic Dual FETs vs 2-Chip Dual FETs

National Semiconductor
February 1977

INTRODUCTION

Recent development of a monolithic dual field effect transistor offers distinct cost and design advantages to the dual FET user. In this article, we have pointed out these advantages on the basis of a comparison that was made between this monolithic structure and the 2-chip dual. Finally, a typical application for this FET is presented and evaluated.

GENERAL

Most dual junction field effect transistors that are available today are the 2-chip variety. These devices are costly to manufacture since 2 FET dice must be found whose electrical characteristics match under a certain set of bias conditions. Finding the matched pair is accomplished by collecting data on a large number of dice and, with the help of a computer, selecting 2 devices with identical characteristics. The result is a device that exhibits excellent end point temperature characteristics as long as the device is operated at the manufacturer specified bias conditions. If the device is operated at bias levels that deviate too much from the specified conditions, the user runs the risk of poor temperature performance. In addition, even if the device is biased at the specified drain current operating point, there still is no guarantee that the device will be well behaved between the temperature end points.

The dual FET manufacturer and user alike would like to have a device that exhibits none of the above shortcomings. They are:

1. High price because of the device selection process.
2. Poor temperature tracking characteristics at currents other than those specified by the manufacturer.
3. Non-linear temperature tracking performance between the manufacturer specified end point temperatures.

Recent development by National of a complete family of dual monolithic junction FETs has virtually eliminated these shortcomings. National's family of duals include general purpose dual process 83 (2N3954 family, etc.), ultra low leakage dual process 84 (2N5902 family), wideband RF dual process 93 (2N5911 family) instrumentation dual cascode process 94 (NDF9400 family), low noise dual process 95 (2N5515 family), and wideband chopper switch dual process 96 (2N5564 family). While some other companies now manufacture a monolithic dual g.p. FET similar to process 83, National is the only "all monolithic" dual manufacturer. These devices (illustrated in *Figures 1a and 1b*) consist of 2 diffused isolated junction FETs.

Since these devices are a monolithic structure, no dice matching is required. The FETs that make up the chip either match or they don't. Units that do not match are eliminated at the wafer sorting stage. Units that do match and exhibit good temperature tracking characteristics at a specified drain current also exhibit good temperature tracking characteristics at other current levels. These devices display a linear differential gate-source voltage relationship to temperature. This is very important to the operational amplifier manufacturer since it allows him to temperature compensate the dual FET, or his entire amplifier circuit for that matter, such that temperature coefficient approaching 0 $\mu V/^{\circ}C$ can be achieved. Since the 2 FETs that constitute the monolithic structure are isolated by a diffusion, they can be operated at different potentials without device interaction.

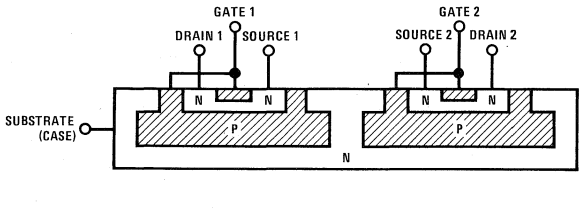


FIGURE 1a. Typical National Monolithic Dual FET Cross-Section (Processes 83, 84, 93, 94, 95 and 96)

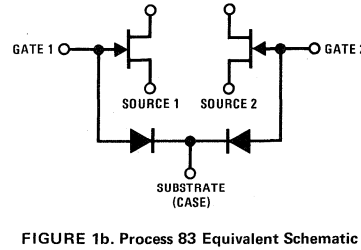


FIGURE 1b. Process 83 Equivalent Schematic

FET TEMPERATURE CHARACTERISTICS

Figure 2 illustrates the gate-source voltage temperature dependence of the 2N3954 (process 83) monolithic FET for various values of drain current. All junction FETs, whether they are monolithic or single unit construction, display similar characteristics. It becomes evident, upon examination of this curve, that a very slight change in drain current results in a substantial change in the gate to source voltage (V_{GS}) temperature coefficient.

Figure 3 illustrates just exactly how dependent V_{GS} is to an I_D change. For example, suppose a device is biased at a 200 μA drain current level. The curve in *Figure 4* tells us that a drain current change of 1 μA will change the V_{GS} temperature coefficient 4.8 μV/°C. The fact the V_{GS} temperature coefficient can be predictably changed by slight variation in the drain current implies that the differential gate-source voltage temperature coefficient can be adjusted to 0 μV/°C by a change in drain current. A 2-chip dual FET can also be temperature compensated in this same manner provided the differential V_{GS} temperature coefficient is constant at all temperatures. The temperature coefficient of the 2-chip system, however, is generally not constant over the specified operating temperature range, therefore making this type compensation difficult. To illustrate the difference in temperature tracking characteristics of the 2-chip FET and the monolithic structure, a 2-chip 10 μV/°C device was compared to a monolithic 10 μV/°C unit.

Figure 4 illustrates how the differential gate-source voltage of the monolithic 2N3954 varies as a function temperature. When both sides of the dual FET are biased at the specified 200 μA ±0.01% level, the temperature coefficient is constant and equal to 6 μV/°C. Also, note that the ΔV_{GS} temperature coefficient can be adjusted to about 0 μV/°C by increasing the drain current in Q2 to 201 μA. The ΔV_{GS} temperature characteristics for the 2-chip 2N3954 dual FET are shown in *Figure 5*. Note that if one employs the definition of temperature coefficient set forth in Note 1, the ΔV_{GS} temperature coefficient of the 2-chip dual is about 8 μV/°C. It would be impossible, however, to achieve a temperature coefficient much better than 8 μV/°C (by adjusting the drain current), because the ΔV_{GS} temperature curve is non-linear.

The ΔV_{GS} temperature characteristics of the 2-chip dual and the monolithic dual were then measured at 500 μA of drain current. The results are illustrated in *Figures 6 and 7*.

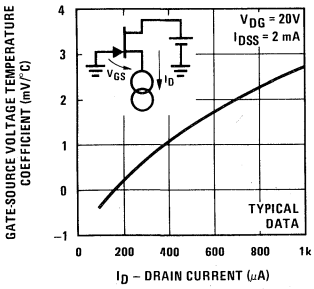


FIGURE 2. Gate-Source Voltage Temperature Coefficient vs Drain Current (Single Device)

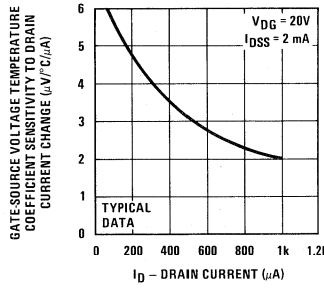


FIGURE 3. Gate-Source Voltage Temperature Coefficient Sensitivity to Drain Current Change vs Drain Current (Single Device)

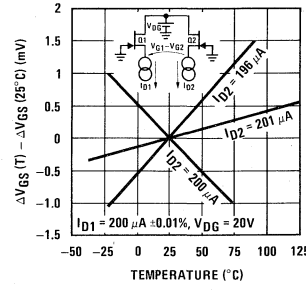


FIGURE 4. Differential Gate-Source Voltage vs Temperature for a Typical Monolithic Dual JFET

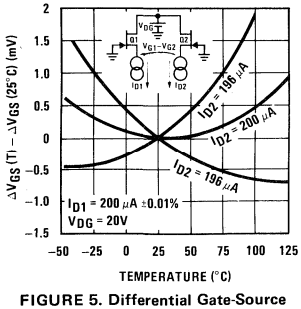


FIGURE 5. Differential Gate-Source Voltage vs Temperature for a Typical 2-Chip Dual JFET (10 μV/°C Unit)

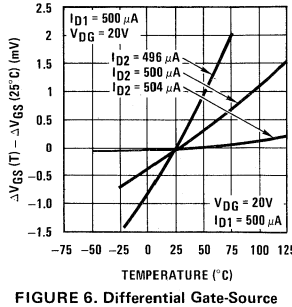


FIGURE 6. Differential Gate-Source Voltage vs Temperature for the Same Monolithic JFET in *Figure 4*, Only the Drain Current has been Changed to 500 μA.

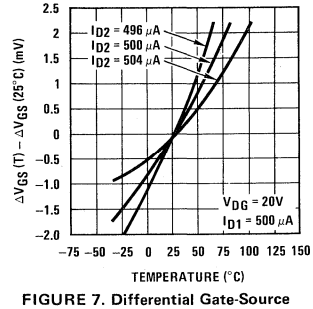


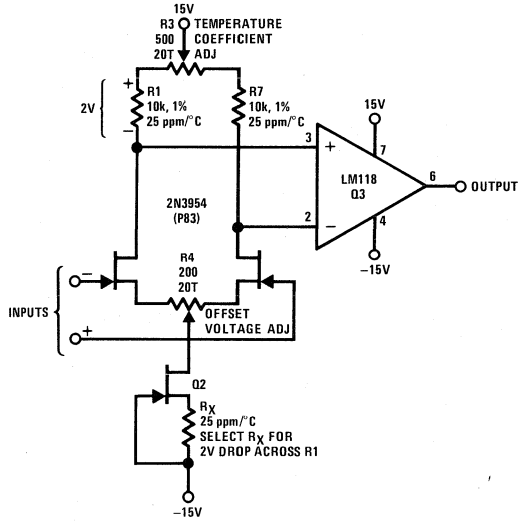
FIGURE 7. Differential Gate-Source Voltage vs Temperature for the Same 2-Chip Dual FET in *Figure 5*, Only the Drain Current is 500 μA

Note that the monolithic dual exhibits good ΔV_{GS} temperature characteristics (TC $\simeq$ 15 μV/°C) while the 2-chip dual has a temperature coefficient greater than 50 μV/°C. The data displayed in *Figures 4–7* is for 2 specific devices; however, it is representative of the data accumulated on a number of process 83 and 2-chip dual FETs.

Another point that warrants discussion is the fast thermal transient response of the monolithic dual FET. This type device is generally employed as the input stage for an operational amplifier; therefore, it may be subjected to electrical overload such as input voltage transients. This condition causes 1 side of the dual FET to dissipate more power than the other, which in turn results in a temperature differential between the 2 sides of the device. The ΔV_{GS} error will disappear once the devices are again in thermal equilibrium. The time for the 2-chip dual FET to reach thermal equilibrium, after a thermal transient, is considerable since the FET chips making up the 2-chip dual are located some distance apart. On the other hand, the monolithic structure recovers from thermal transients very rapidly because the 2 FETs, constituting the chip, are in intimate contact.

APPLICATIONS

A typical operational amplifier application is illustrated in *Figure 8*. This circuit employs the 2N3954 monolithic dual FET as the input device. The drain current level is set by FET Q2 and resistor R_X. FET Q2 is a 2N5457. This device exhibits a 0 TC drain current operating point



Note 1: The temperature coefficient can typically be adjusted (by R3 and R4) to less than 5 μV/°C from −25°C to +85°C.

Note 2: The common-mode rejection ratio is typically greater than 100 dB for input voltage swings of 5V.

FIGURE 8. Low Temperature Coefficient Operational Amplifier

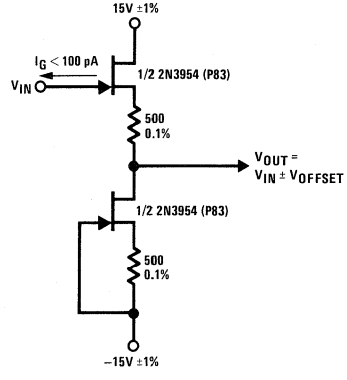


FIGURE 9

at about 400 μA. In addition, the Q2–R$_X$ combination exhibits an output impedance typically greater than 10 MΩ. This characteristic, coupled with the high output impedance of the IMF3954, contribute to a CMRR of greater than 100 dB for this amplifier. Input offset voltage can be adjusted to 0 with R4. This control exhibits sensitivity of 2 mV/turn. The temperature coefficient can be compensated by R3 with an approximate sensitivity of 5 μV/°C/turn. The temperature performance of a typical amplifier of this type is illustrated in *Figure 10*.

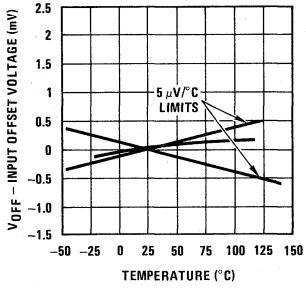


FIGURE 10. Input Offset Voltage vs Temperature

CONCLUSION

The junction isolated dual monolithic junction FET does exhibit a more linear ΔV_{GS} temperature relationship than does the 2-chip dual FET. In addition, the monolithic structure exhibits good temperature tracking characteristics at drain currents other than the specified I_D. This is generally not the case for the 2-chip system. Since all National duals are monolithic structures, the cumbersome process of matching individual dice is not required.

This, of course, makes the monolithic dual less expensive then its 2-chip counterpart. And finally, the monolithic dual FET maintains excellent tracking characteristics when the device is subjected to thermal transients or momentary voltage overloads. This is not the case with the 2-chip dual since these devices are thermally isolated from one another.

Note 1:

Definition of temperature coefficient:

$$(TC)_L = \frac{|\Delta V_{GS}(T_O) - \Delta V_{GS}(T_L)|}{T_O - T_L} \times 10^6\ \mu V/^\circ C$$

$$(TC)_H = \frac{|\Delta V_{GS}(T_H) - \Delta V_{GS}(T_O)|}{T_H - T_O} \times 10^6\ \mu V/^\circ C$$

Where $T_O = 25^\circ C$
T_H – High temperature limit ($T_H = 85$ or $125^\circ C$)
T_L – Low temperature limit
$\Delta V_{GS}(T_O)$ in the differential gate-source offset voltage at T_O (volts)
$\Delta V_{GS}(T_H)$ – Differential gate-source offset voltage at T_H
$\Delta V_{GS}(T_L)$ – Differential gate-source offset voltage at T_L

Why Use Cascode Dual FETs?

National Semiconductor
FET Brief 2
Mike Turner
March 1977

National Semiconductor's cascode dual JFET is a unique structure in which each half of a monolithic dual is actually 2 FETs connected in cascode. *Figure 1a and 1b* show the comparison. The advantages of a cascode structure are low dynamic leakage (I_G) and greatly improved common-mode rejection ratio. National's processes 84 and 94 use the cascode configuration.

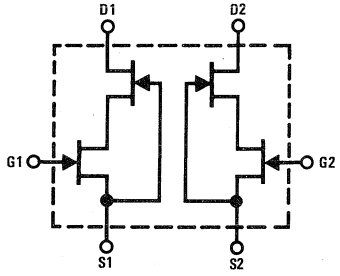


FIGURE 1a. Cascode Configuration

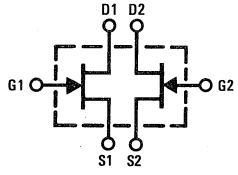


FIGURE 1b. Triode Configuration

The cascode FET device offers a significant improvement in gain/input current ratio when compared to standard FET triodes. Specifically, the NDF9406 series devices are specified at $I_G < 5$ pA under operating conditions, and they exhibit operating g_{fs} of 1200 μmho typical. This compares favorably with non-cascode duals exhibiting 3–10 times the I_G.

Furthermore, the NDF9406 series will maintain this low input current over a common-mode input range of up to ±15V, while triode devices are limited to approximately ±5V for the same performance.

Table I compares popular junction dual devices available in the marketplace.

It is important to remember that I_G is a dynamic characteristic. The data supplied by major FET suppliers clearly shows the effect of operating voltage and current on I_G and the considerable difference between I_G and the static parameter I_{GSS}.

Figure 2 explores the differences between cascode devices such as NDF9406–NDF9409 and a triode configured 2N5196. It is easily seen that severe gate current modulation will result in triode devices with even relatively small change in V_{DG}. Gate current variations will cause variations in offset bias currents, offset voltage and common-mode rejection. This is especially true in high impedance circuits where gate impedances are not matched.

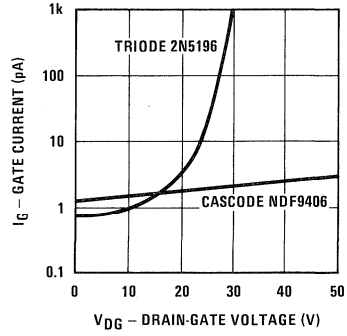


FIGURE 2. Typical Gate Current vs Drain-Gate Voltage @ I_D = 200 μA

The second major advantage of the cascode configuration is improved common-mode rejection ratio. The input FETs are effectively shielded from large changes in operating point by the drain load FETs.

TABLE I

DEVICE SERIES	BV	I_G V_{DG}/I_D	g_{fs} I_D
2N3954–2N3958	>50V	<50 pA @ 20V/200 μA	1000 @ 200 μA*
2N5196–2N5199	>50V	<15 pA @ 20V/200 μA	>700 @ 200 μA
NDF9406–NDF9409	>50V	<5 pA @ 35V/200 μA	>950 @ 200 μA

*Limits not specified on the published data sheet.

The inherent matching of all devices because of monolithic construction further reduces the effects of common-mode signals.

Figure 3 compares CMRR of a monolithic triode dual FET (National P83) with a cascode structure (National P94).

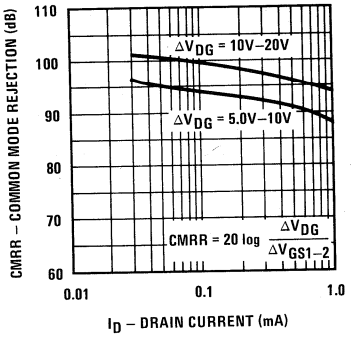


FIGURE 3a. Triode Construction

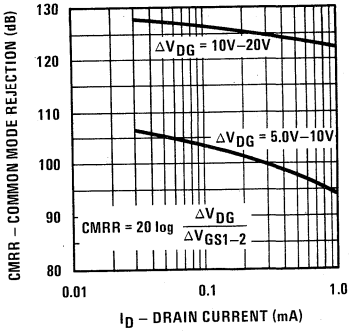
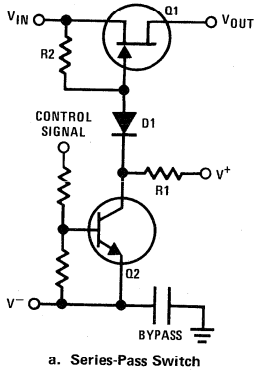


FIGURE 3b. Cascode Construction

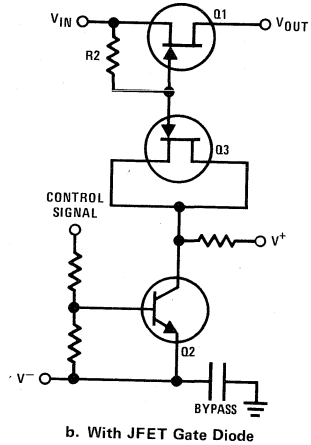
Simple VHF Analog Switches

National Semiconductor
FET Brief 1
Mike Turner
February 1977

Simple JFET switches like those in *Figure 1* will toggle at rates to about 10 MHz and switch analog signals with frequencies to above 100 MHz. They accomplish this by resolving in the gate-driver design the contradictory performance goals that even the best switching transistors cannot meet.



a. Series-Pass Switch



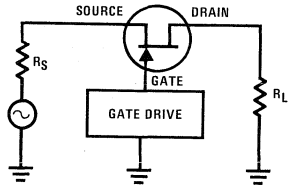
b. With JFET Gate Diode

FIGURE 1. High-Frequency JFET Switching Circuits

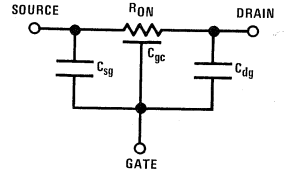
To switch high-frequency signals, the JFET should have low ON impedance, $r_{ds(on)}$ or R_{ON}, and low input capacitance, C_{iss}. The switch's RC time constant is established by these 2 parameters, and they also indicate the bandwidth capability. JFETs have been developed that come close to being ideal, but unfortunately the real-world nature of semiconductor devices makes it impossible to achieve optimum values of both parameters in the same device. Low R_{ON} calls for a physically large JFET. On the other hand, the very low capacitance needed for fast toggle rates implies small size.

At a casual glance, gate drive impedance does not appear very important. However, the JFET device conflict between R_{ON} and C_{iss} may be overcome by using the proper gate driver. The drive circuit should have a low impedance when the JFET is turned OFF and a high impedance when the JFET is turned ON. The low-impedance path is needed to prevent analog-signal feedthrough and the high impedance to minimize signal attenuation through the driver while the JFET is conducting. A well-designed driver can do both.

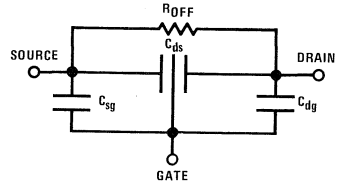
The relationships among JFET and driver characteristics can be sorted out with the help of *Figure 2*, which shows a typical series-pass switch and the equivalent circuits of the JFET in its ON and OFF conditions. A JFET operates best as a series-pass switch when the ON condition allows R_{ON} and shunt capacitance to be low, and series-pass capacitance to be high. But in the OFF condition, it should exhibit low series-pass capacitance and high series-pass resistance (R_{OFF}). The JFET will have these characteristics when properly matched to the driver.



a. Series-Pass JFET Switch



b. JFET On



c. JFET Off

C_{dg} = drain-gate capacitance
C_{gc} = gate-channel distributed capacitance
C_{sg} = source-gate capacitance
C_{ds} = drain-source capacitance
R_{ON} = ON impedance
R_{OFF} = OFF impedance

FIGURE 2. Series-Pass Switch and JFET Equivalent Circuits

Getting down to a low R_{ON} when the gate is turned ON is no problem. A JFET such as the 2N4391 has a maximum R_{ON} of 30Ω (see $r_{ds(on)}$ in Table I). However, the parallel capacitance in the signal path can become fairly high—about 15 pF when drain, source and gate have the same potential ($V_{DS} = V_{GS} = 0$). The simple answer to this dilemma is to drive the gate with a high AC impedance when the switch is closed. The shunt capacitance will be in series with a high impedance. Virtually all of the signal will then go through the JFET, the path of least resistance, rather than through the gate-to-ground connection.

Next problem. When the switch is OFF, high-frequency attenuation is the name of the game. It is depended upon to prevent the signal at the input from reaching the output. The JFET channel is, for all practical purposes, an open circuit because R_{OFF} of a quality JFET is over $10^{12}\Omega$ although this decreases as frequency goes up. However, capacitive feedthrough is the most significant route across the switch. From *Figure 2c*,

$$C_{FEEDTHROUGH} = C_{ds} + \frac{C_{sg}C_{dg}}{C_{sg} + C_{dg}}$$

Feedthrough capacitance can be significant if the gate is not operated at AC ground. Minimizing the right-hand term by operating the gate at AC ground allows C_{ds} to become the pacing factor. If the gate is grounded, C_{ds} will be approximately 0.2 pF. In other words, the effective R_{OFF} of the switch depends directly on circuit design, not the JFET.

Now to put these principles to work. The best high-frequency switch is an N-channel JFET. Its gate should be biased positive from a high-impedance source for turn-on and biased negative through a low-impedance path for turn-off. Driving the switch ON through an RF choke sounds tempting, but it would be difficult to avoid resonances and oscillation bursts during some switching conditions. DC resistances could be increased to equal or exceed R_S in parallel with R_L, but then the toggle rate would be kept down by the very high drive impedance.

We prefer the circuits in *Figure 1*, which are fairly fast and not tricky. When NPN transistor Q2 is in saturation, Q1 is biased OFF through a low-impedance path. The diode is slightly forward-biased and exhibits high capacitance. When Q2 turns OFF, D1's cathode is driven positive by R1. Now the diode is reverse-biased and exhibits high impedance and low capacitance. The charge that was stored on D1 discharges into the gate of Q1, allowing the JFET to be turned ON. Because there is no good discharge path available to the charge stored on Q1's gate, the gate will "follow" any signal swing in the analog input voltage. Adding R2 will ensure that the gate follows the signal even during DC conditions. Remember, however, that the $R2/C_{sg}$ time constant will effect switching time and gate-source signal tracking.

Don't expect just any diode to work well; D1's capacitance is critical and should match that of the JFET ($C_{D1} = C_{Q1}$). One good way of making sure that the JFET and the diode are well mated is to use the same type of JFET for both. The gate lead is 1 electrode of the diode and the drain and source leads are simply tied together to form the other electrode. The circuit in *Figure 1b* was optimized in this way.

Excellent high-frequency series switches can be made with 2N4091, 2N4092 and 2N4093 JFETs. RC time constants are short because of their low $r_{ds(on)}$ and capacitance, and leakage is low. The 2N4391, 2N4392 and 2N4393 series is even better, having only 100 pA leakage and lower C_{iss}. Even though the 2N4416 is classed as an RF amplifier, it is also listed in Table I to illustrate that many of our other JFETs can solve special switching problems. This one does well in circuits requiring very low capacitance and leakage. Although the R_{ON} of an RF transistor is not specified, it can be estimated as $r_{ds(on)} \cong 0.85/Y_{fs}$, which is typically 170Ω for the 2N4416.

TABLE I. JFETs for High-Frequency Analog Signal Switching

TYPE NO.	BV_{GSS} OR BV_{DGO} (MAX)	I_{GSS} (MAX)	C_{iss} (MAX)	C_{rss} OR C_{DGO} (MAX)	$r_{ds(on)}$ (MAX)	t_{on} (MAX)	t_{off} (MAX)
2N4091	40V	0.2 nA	16 pF	5 pF	30Ω	25 ns	40 ns
2N4092	40V	0.2 nA	16 pF	5 pF	50Ω	35 ns	60 ns
2N4093	40V	0.2 nA	16 pF	5 pF	80Ω	60 ns	80 ns
2N4391	40V	0.1 nA	14 pF	3.5 pF	30Ω	15 ns	20 ns
2N4392	40V	0.1 nA	14 pF	3.5 pF	60Ω	15 ns	35 ns
2N4393	40V	0.1 nA	14 pF	3.5 pF	100Ω	15 ns	50 ns
2N4416	30V	0.1 nA	4 pF	0.8 pF	170Ω*		
2N4416A	35V	0.1 nA	4 pF	0.8 pF	170Ω*		

*This value is not specified in RF amplifier JFETs; 170Ω is typical

Noise of Sources

National Semiconductor
John Maxwell
February 1977

INTRODUCTION

The elimination or minimization of noise is one of the most perplexing problems facing engineers today. Many preamplifiers and components come with outstanding noise specifications, only to disappoint the user. The problem is the difference between specification and application, as the amplifiers are specified under ideal conditions not the real conditions, (i.e., a transducer connected to the input). Many times the transducer noise is as large or even greater than the amplifier noise, degrading the signal to noise ratio. Before amplifier or component noise can be considered, familiarity with the source noise is essential.

REVIEW OF NOISE BASICS

There are 3 types of transducers: resistive, capacitive and inductive. The noise of a passive network is thermal noise, generated by the real part of the complex impedance, as given by Nyquist's relation:

$$\overline{V_n^2} = 4kTRe(Z)\,\Delta f \qquad (1)$$

$\overline{V_n^2}$ = Mean square noise voltage (V^2)

k = Boltzmann's constant (1.38×10^{-23} VAS/°K)
T = Absolute temperature (°K)
Re(Z) = Real part of complex impedance (Ω)
Δf = Noise bandwidth (Hz)

The noise may be represented as a spectral density (V^2/Hz) or more commonly in $\mu V/\sqrt{Hz}$ or $nV/\sqrt{Hz}$ and is given by:

$$e_n^2 = \frac{\overline{V_n^2}}{\Delta f} \qquad (2)$$

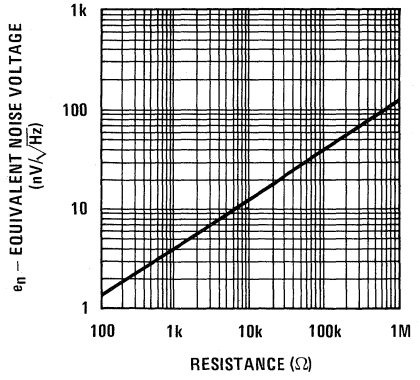


FIGURE 1. Thermal Noise Voltage vs Resistance

The total noise voltage in a frequency band can be readily calculated if it is white noise (i.e., Re(Z) is frequency independent). This is not the case for capacitive or inductive sources or most real world noise problems. Rapidly changing network impedance and amplifier gain equalization combine to complicate the issue. The total source noise in a non-ideal case can be calculated by breaking the noise spectrum into several small bands where the noise (Re(Z)) is nearly white and calculating the noise of each band. The total source noise is the RMS sum of the noise in each of the bands N_1–N_n.

$$V_{NOISE} = (V^2_{N_1} + V^2_{N_2} + - - - + V^2_{N_n})^{1/2} \qquad (3)$$

The expression does not take amplifier gain equalization (like RIAA) into account, which will change the character of the noise at the amplifier output. By reflecting the gain equalization to the amplifier input and normalizing the gain to 0 dB at 1 kHz, the equalized source noise may then be calculated.

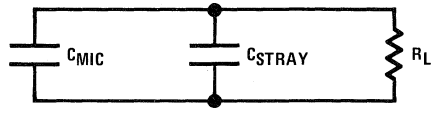
$$V_{EQ} = (|A_1|^2 V^2_{N_1} + |A_2|^2 V^2_{N_2} + - - - + |A_n|^2 V^2_{N_n})^{1/2} \qquad (4)$$

Where V_{EQ} = equalized source noise (μV) and
$|A_n|$ = magnitude of the equalized gain at the center of each noise band (V/V).

SOURCE NOISE

Models are needed for capacitive and inductive systems such that noise calculations can be made. Namely, the real part of the impedance needs to be determined.

A lumped model of a capacitive source, such as condenser or electret microphone, consists of the microphone and stray capacitance shunted by a load resistance.



$$Z = Re(Z) + jIM(Z) \qquad (5)$$

$$Re(Z) = \frac{R}{1 + \omega^2 R^2 C^2}$$

$$|Z| = \left(\frac{R^2}{1 + \omega^2 R^2 C^2}\right)^{1/2}$$

FIGURE 2. Lumped Model of a Capacitive Microphone

It should be noted that for any particular microphone, the noise of the network ($(C_m + C_s)//R_L$) is reduced by increasing R_L because Re(Z) (the real part of the impedance) is inversely proportional to R_L (see equation 5).

The inductive source (phono cartridges and tape heads) is more complex to analyze because it has a much more complex model. The simplified lumped model of a phono cartridge or tape head consists of a series inductance and resistance shunted by a small capacitor. Each phono cartridge or tape head has a recommended load con-

sisting of a specified shunt resistance and capacitance. A model for the inductive source and preamp input network is shown in *Figure 3*.

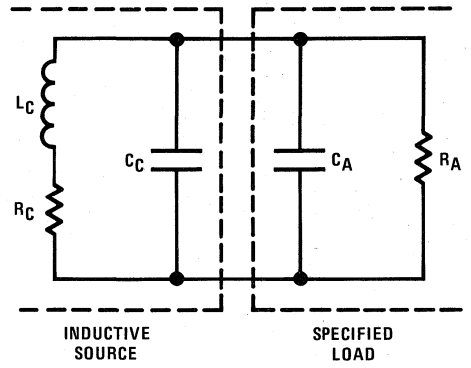
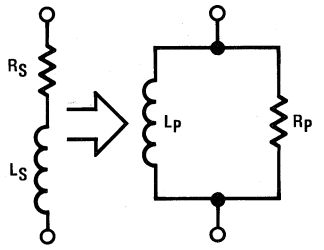


FIGURE 3. Phono Cartridge or Tape Head and Preamp Input Network

This circuit is quite formidable to analyze and needs further simplication. Through the use of Q equations, a series L-R is transformed to a parallel L-R.

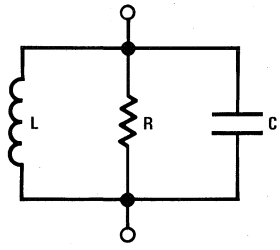


$$Q = \frac{\omega L_s}{R_s} \qquad (6)$$

$$R_p = R_s\,(1 + Q^2)$$

$$L_p = L_s\left(\frac{1 + Q^2}{Q^2}\right)$$

Simplifying the input network to:



$$R = R_A // R_p$$
$$L = L_p$$
$$C = C_s + C_c$$

FIGURE 4. Simplified Inductive Source Network

$$Re(Z) = \frac{RX_L^2X_C^2}{(RX_L - RX_C)^2 + X_L^2\,X_C^2} \qquad (7)$$

$$Z = \frac{RX_LX_C}{((RX_L - RX_C)^2 + X_L^2\,X_C^2)^{1/2}}$$

$$X_L = \omega L$$
$$X_C = 1/\omega C$$

The tools are now available to calculate the noise of a variety of transducers and see how this unspecified noise affects amplifier (S/N) performance.

EXAMPLES

Calculations of electret microphone noise with various loads and RIAA equalized phono cartridge noise is done using equations (1)–(7). Center frequencies and frequency bands must be chosen first. Values of the lumped circuit components calculated and noise calculated for each band, then summed for the total noise. Octave bandwidths starting at 25 Hz will be adequate for approximating the noise.

In this example, the microphone capacitance is 10 pF loaded with 5 pF of amplifier and stray capacitance. Two resistive loads will be used to illustrate the effect R_L has on the microphone noise. R_{L1} = 1GΩ (10^9), R_{L2} = 10GΩ (10^{10}). It is assumed that there is no gain equalization in the amplifiers that follow. The noise calculations are summarized in Table I.

The electret or condenser microphone noise (Re(Z)) is reduced when the load resistance is increased. This is one of the cases when a larger resistance means lower noise, not more noise.

The second example is the calculation of the RIAA equalized noise of an ADC 27 phono cartridge loaded with C_A = 250 pF and R_A = 47k. The cartridge constants are R_s = 1.13k and L_s = 0.75H (C_c may be neglected). The noise calculations are summarized in Table II for this example.

The RIAA equalized noise of the ADC 27 phono cartridge and preamp input network was 0.73 μV for the audio band. Typical high quality preamps have noise voltages less than 1 μV, resulting in a 3 dB or more loss in system S/N ratio when the cartridge noise is added to the preamp noise (in an RMS fashion).

CONCLUSIONS

Zero noise sources and amplifiers do not exist. Specifying amplifier noise under ideal conditions will only lead to ideal specifications, not a measure of actual performance. Methods of S/N ratio measurement should be used that reflect the true performance instead of hollow specifications.

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3. Fristoe, H.T., "The Use of Q Equations to Solve Complex Electrical Networks". Engineering Research Bulletin, Oklahoma State University, 1964.
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TABLE I. Summary of Electret Microphone Calculations

f Range (Hz)	25–50	50–100	100–200	200–400	400–800	800–1600	1600–3200	3200–6400	9600–12.8k	12.8k–20k
f Center (Hz)	37.5	75	150	300	600	1200	2400	4800	9600	16,400
f_{Bw} (Hz) for R_L = 1GΩ	25	50	100	200	400	800	1600	3200	6400	7,200
Re(Z) (Ω)	74.2M	19.6M	4.98M	1.25M	0.31M	78k	19k	4.9k	1.22k	420
|Z| (Ω)	272M	140M	70.6M	35.4M	17.7M	8.8M	4.4M	2.2M	1.1M	650
e_{nz} (nV/$\sqrt{Hz}$)	1100	560	280	140	71	36	18	9	4.5	2.8
V_{nz} (μV)	5.5	3.96	2.8	1.98	1.42	1.02	0.72	0.51	0.36	0.24
V^2_{nz} (μV^2)	30.2	15.7	7.84	3.92	2.0	1.04	0.52	0.26	0.13	0.06
$(\Sigma V^2_{nz})^{1/2} \simeq 7.9\ \mu V$										
R_L = 10GΩ										
Re(Z) (Ω)	8M	2M	0.5M	125k	31.3k	7.8k	2k	500	122	42
|Z| (Ω)	283M	141M	70.8M	35.4M	17.7M	8.8M	4.4M	2.2M	1.1M	650k
e_{nz} (nV/$\sqrt{Hz}$)	320	180	90	45	23	11.4	5.8	2.9	1.4	0.84
V_{nz} (μV)	1.6	1.3	0.9	0.64	0.46	0.32	0.232	0.16	0.112	0.07
V^2_{nz} (μV^2)	2.56	1.62	0.81	0.41	0.21	0.103	0.054	0.025	0.013	0.005
$(\Sigma V^2_{nz})^{1/2} \simeq 2.4\ \mu V$										

TABLE II. Summary of Phono Cartridge Calculations

f Range (Hz)	25–50	50–100	100–200	200–400	400–800	800–1.6k	1.6k–3.2k	3.2k–6.4k	6.4k–12.8k	12.8k–20k
f Center (Hz)	37.5	75	150	300	600	1200	2400	4800	9600	16.4k
f_{Bw} (Hz)	25	50	100	200	400	800	1600	3200	6400	7.2k
$Q = (\omega L_s/R_s)$	0.156	0.313	0.625	1.25	2.5	5	10	20	40	68.4
Q^2	0.0244	0.098	0.391	1.56	6.25	25	100	400	1600	4678.6
$1 + Q^2$	1.0244	1.098	1.391	2.56	7.25	26	101	401	1601	4679.6
$1 + Q^2/Q^2$	42	11.24	3.56	1.64	1.16	1.04	1.01	1.0	1.0	1.0
R_p (Ω)	1.16k	1.24k	1.57k	2.9k	8.2k	29.4k	114k	454k	1.8M	5.29M
L_p (H)	31.5	8.43	2.67	1.23	0.87	0.78	0.76	0.75	0.75	0.75
$R_p//R$ (Ω)	1.13k	1.21k	1.52k	2.74k	7k	18.1k	32.9k	42.6k	45.8k	46.6k
X_L (Ω)	7.42k	3.97k	2.52k	2.32k	3.28k	5.88k	11.45k	22.6k	45.2k	77.2k
X_c (Ω)	17M	8.48M	4.24M	2.12M	1.06M	0.53M	0.265M	0.133M	66.3k	38.8k
Re(Z) (Ω)	1.11k	1.11k	1.11k	1.15k	1.26k	1.73k	3.86k	12.4k	41.5k	34k
|Z| (Ω)	1.12k	1.15k	1.3k	1.77k	2.97k	5.59k	11.7k	24.4k	43.6k	40.1k
e_{nz} (nV/$\sqrt{Hz}$)	4.24	4.24	4.24	4.31	4.51	5.29	7.9	14.2	26	23.5
V_N (nV)	21.2	30	42.4	61	90.2	149.6	316	803	2080	1994
V^2_n (nV^2)	449.4	900	1798	3721	8136	22.4k	99.9k	645k	4.33M	3.98M
A^2	63.0	29.5	10.7	3.85	1.66	0.85	0.49	0.154	0.043	0.019
$A^2V^2_n$ (nV^2)	28.3k	26.6k	19.2k	13.2k	13.5k	19k	48.9k	99.3k	186k	76k

$(\Sigma V^2_n)^{1/2}$ = 3 μV unequalized noise

$(\Sigma 1An\ 12V^2_n)^{1/2}$ = 0.73 μV RIAA equalized noise

The Noise Figure Fallacy

National Semiconductor
John Maxwell
February 1977

Noise Figure (NF) can be one of the most misleading specifications confronting the engineer today. Noise Figure is defined as the ratio of total output noise power to the output noise power of the source.

$$NF = 10 \text{ Log } \frac{\text{Total output noise power}}{\text{Output noise power of the source}} \quad (1)$$

A minimum NF exists for any amplifier, but is usually far removed from the actual operating conditions. This is where the problem begins. Lowering the NF doesn't always lower the noise which is what the engineer is really interested in. NF only gives the designer insight into the ratio of the amplifier noise to the source noise, not the input noise of the amplifier or the signal to noise ratio.

Amplifier noise performance is adequately described by modeling the noise sources as a series voltage generator and a shunt current generator with a series voltage generator for the source resistance noise.

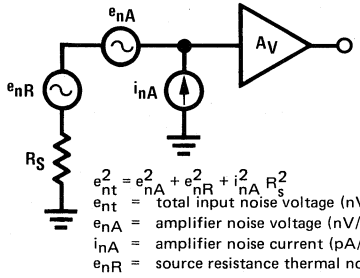
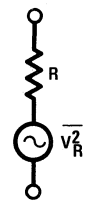


FIGURE 1. Simiplified Amplifier Noise Model

The amplifier noise data is found on vendor data sheets in the form of e_n and i_n vs frequency for bipolar transistors and e_n vs frequency for FETs and FET amplifiers.

Current noise depends on amplifier input bias current which is only a few picoamps for FETs and is therefore negligible. However, bipolar transistor amplifiers have bias currents into the microamp range where current noise is significant.

The thermal noise of the source resistance is given by Nyquist's relation.



$$\overline{V_R^2} = 4kTR\Delta f \quad (2)$$

$\overline{V_R^2}$ = mean square noise voltage (V^2)
k = Boltzmann constant (1.38×10^{-23} VAS/°K)
T = absolute temperature (°K)
R = resistance (Ω)
Δf = noise bandwidth (Hz)

with the spectral density given by e_n^2

$$e_{nR} = (\overline{V_R^2}/\Delta f)^{1/2} \quad (3)$$

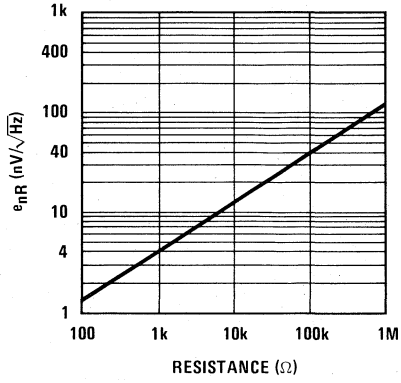


FIGURE 2. Thermal Noise vs Resistance

Using the model of *Figure 1*, an expression of noise figure in terms of the noise generators can be developed.

The noise power of the source can be found by using Nyquist's relation.

$$\text{Source Noise Power} = \frac{\overline{V_R^2}}{R^2} = \frac{e_{nR}^2 \Delta f}{R^2} \quad (4)$$

with the total output noise power at the input of the amplifier of:

$$\text{Total noise power} = \frac{e_{nR}^2 \Delta f}{R^2} + \frac{e_{nA}^2 \Delta f}{R^2} + i_{nA}^2 R^2 \Delta f \quad (5)$$

Yielding

$$NF = 10 \text{ Log } \left[1 + \frac{e_{nA}^2 + i_{nR}^2 R^2}{e_{nR}^2} \right] \quad (6)$$

Noise figure has a minimum that occurs at an optimum source resistance R_{opt}.

$$R_{opt} = \frac{e_{nA}}{i_{nA}} \quad (7)$$

Artifically changing the source resistance for minimum NF will generally increase the circuit noise as demonstrated by the following example.

Example:

An amplifier is needed to boost the signal from a resistive transducer.

Amplifier requirements

Av = 100
f = 10 Hz to 10 kHz
Transducer = 10 kΩ

Amplifier—LF356
Noise data, e_n = 12 nV/$\sqrt{Hz}$ @ 1 kHz
i_n = 0.01 pA/$\sqrt{Hz}$ @ 1 kHz

The optimum source resistance for the amplifier is found to be 12M (using equation (7)). Using *Figure 2*, the noise of the transducer is 12 nV/$\sqrt{Hz}$ and the noise of the optimum source resistance is 140 nV/$\sqrt{Hz}$.

Using the non-inverting amplifier configuration, we'll view the effect of R_{opt}. In one case, resistance will be added to the source to equal the amplifier optimum source resistance (not affecting gain). The other case will only have the transducer connected to the input.

We will neglect the noise of the feedback resistors and determine the input noise and NF for both configurations using equations (1)—(6).

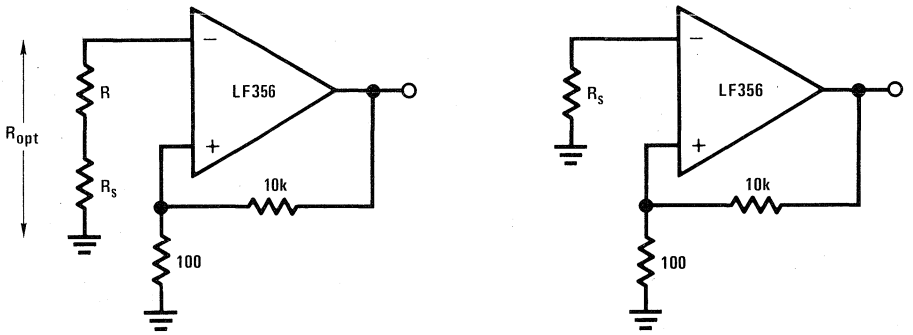
Case A, minimum NF

Total input noise $V_n = e_{nt}(\Delta f)^{1/2} = 14\ \mu V$
NF= 0.06 dB

Case B, minimum noise

V_n = 1.7 μV
NF = 3 dB

Noise figure is only a measurement of the amplifier noise relative to the source noise. The example used was radical, but it illustrated a very important point. Resistance should never be added in series with the source to improve the NF. The NF will improve but the input noise will suffer, degrading performance. Total input noise should always be considered allowing problem sources to be identified and minimized to meet the system's specific noise requirements.



a. Minimum NF

b. Minimum Noise

FIGURE 3. 2 Amplifier Solutions

Low Noise FET Amplifiers

National Semiconductor
John Maxwell
March 1977

INTRODUCTION

Discrete JFETs reign supreme as low noise amplifiers. JFETs are virtually free from the problems of current noise, popcorn noise and limited bandwidth which plague bipolar transistors and bipolar input op amps.

Unfortunately, JFETs are cumbersome to use because of low gain and the need of extensive biasing networks. However, monolithic op amps are cheap and easy to use but suffer from poor noise performance. By combining JFETs with an op amp yields single and differential input amplifiers that have the best of both worlds; low noise, high gain and ease of use.

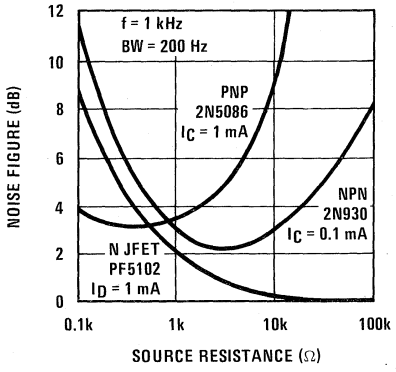


FIGURE 1. Bipolar and JFET Transistor Noise Comparison

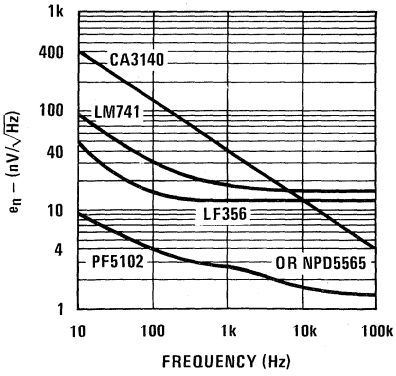
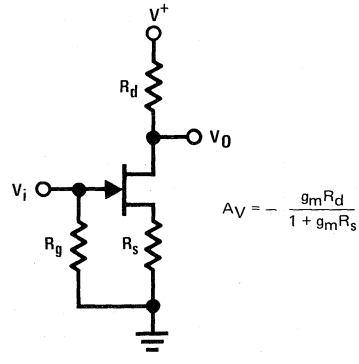
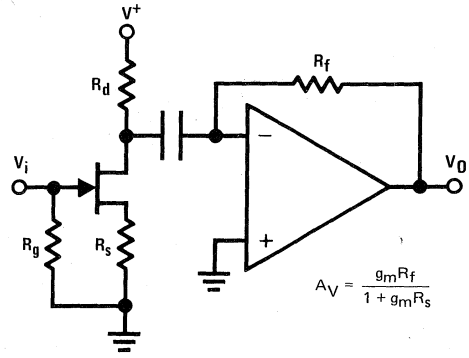


FIGURE 2. Discrete JFET and Op Amp Noise Comparison

The main problem with JFETs is that the voltage gain is limited by the size of the load resistance which is limited by the power supply voltage and the FET operating current. The voltage gain can be increased by combining the JFET (a transconductance amplifier) with an op amp current to voltage (I/V) amplifier, circumventing the limited load resistor.



a. Single FET Stage



b. FET with I/V Amplifier

FIGURE 3. FET Gain Stages

In the FET/op amp configuration, the FET AC drain current is shunted to the op amp virtual ground and through its feedback resistor, bypassing the FET drain resistor, R_d. The drain resistor is used to bias the FET in a linear region with the feedback resistor, R_f, used to set the gain.

Biasing problems associated with Iot and device to device parameter variations are minimized by biasing the source through a large resistor to the negative supply of the op amp. A portion of the source resistor should be unbypassed to minimize gain variations between FETs.

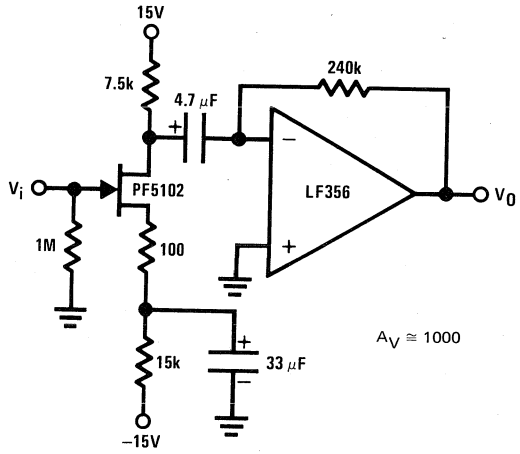
From a design standpoint, the maximum AC drain current should be 1/10 of the FET quiescent current for low distortion. The unbypassed portion of the source resistor should be limited to 220Ω for minimum noise and to increase the op amp feedback resistor (decreased AC current).

Expressions for the single and differential amplifier configurations are needed for optimizing the noise to meet system noise requirements.

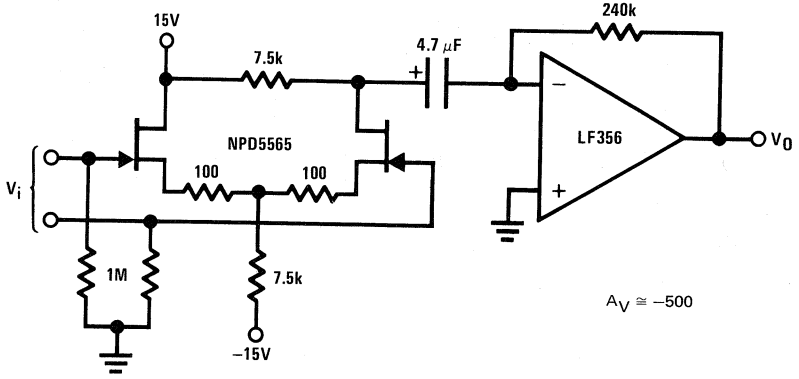
Amplifier noise performance is adequately described by modeling the noise sources as a series voltage generator and a shunt current generator with a series voltage generator for the source resistance thermal noise. The thermal noise of a resistor is given by Nyquist's relation and has a spectral density given by e_{nR}^2.

$$e_{nR}^2 = 4kTR \quad (1)$$

e_{nR}^2 = mean square noise voltage per unit bandwidth (nV^2/Hz)
k = Boltzmann constant ($1.38 \times 10^{-23} VAS/°K$)
T = absolute temperature (°K)
R = resistance (Ω)



a. Single-Ended



b. Differential Input

FIGURE 4. High Gain FET/Op Amp AC Amplifiers

The single ended and differential input amplifier input noise (FET noise current is negligible) is given by the RMS sum of the noise generators.

Single-Ended:

$$e_{nt}^2 = e_{nf}^2 + e_{ns}^2 + \left(\frac{1 + g_m R_s}{g_m R_d}\right)^2 (e_{nA}^2 + e_{nR}^2 + i_{nA}^2 R^2)$$

Differential Input:

$$e_{nt}^2 = 2\,(e_{nf}^2 + e_{ns}^2) + 4\left(\frac{1 + g_m R_s}{g_m R_d}\right)^2 (e_{nA}^2 + e_{nR}^2 + i_{nA}^2 R^2)$$

with

e_{nt} = total input noise voltage (nV/$\sqrt{Hz}$)
e_{nf} = FET noise voltage (nV/$\sqrt{Hz}$)
e_{nA} = op amp noise voltage (nV/$\sqrt{Hz}$)
i_{nA} = op amp noise current (pA/$\sqrt{Hz}$)
e_{ns} = source resistor thermal noise (nV/$\sqrt{Hz}$)
e_{nR} = drain and feedback (R_d//R_f) resistor thermal noise (nV/$\sqrt{Hz}$)
g_m = FET transconductance at the FET operating current (mmho)
R = parallel resistance of R_d and R_f (Ω)

The differential configuration has higher noise and lower gain than the single-ended version, but is useful when low distortion or balanced inputs are of paramount importance.

The noise of the op amp and the FET drain resistor is reduced by the gain of the FET portion of the amplifier $\frac{g_m R_d}{1 + g_m R_s}$. The noise of the feedback resistor has little effect on the noise but in conjunction with the drain resistor, it can have a dramatic effect on the total circuit noise. The drain resistor is the input leg of an inverting amplifier with the op amp and the feedback resistor. This amplifier has a gain of $-R_f/R_d$ which boosts the op amp noise, limiting the size of R_f to about 390k.

Practical low noise, high gain AC amplifiers can be built using a low noise JFET and just about any op amp. The op amp needs to meet the slew rate and bandwidth requirements of the circuit, eliminating selected low noise op amps or complex discrete amplifiers.

A note of caution is in order for the op amp noise. Virtually any JFET input or bipolar input op amp can be used without trouble, but MOSFET input op amps should be avoided. MOSFET 1/f noise is one or more orders of magnitude greater than discrete JFETs, JFET op amps or bipolar input op amps. MOSFETs have 1/f corner frequencies (where the noise power rises as 1/f) starting as high as 100 kHz. The other forms of amplifiers have 1/f corner frequencies of 1 kHz and less. Quite a difference.

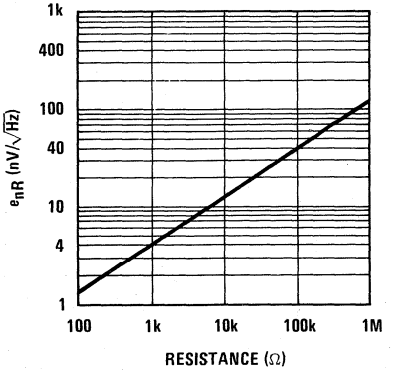


FIGURE 5. Thermal Noise vs Resistance

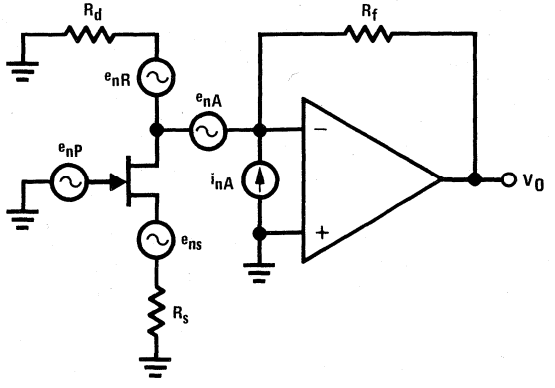


FIGURE 6. Single-Ended Noise Model

The Low Noise JFET—The Noise Problem Solver

National Semiconductor
Application Note 151
John Maxwell
January 1976

The most versatile low noise active device available to the designer today is the Junction Field-Effect Transistor (JFET). JFETs are virtually free of the problems which have plagued bipolar transistors—limited bandwidth, popcorn noise, a complex design procedure to optimize noise performance. In addition, JFETs offer low distortion and very high dynamic range.

Most designers think of JFETs for very high source impedances. However, modern devices offer the designer performance improvements over bipolar transistors in NF for all but lowest impedance (<500Ω) sources and even then may provide improved performance if popcorn noise, bandwidth or circuit component noise is a consideration (see *Figure 1).*

Therefore, the purpose of this article is to review low noise design procedures and indicate the simplicity of designing high performance low noise amplifiers with low cost JFETs.

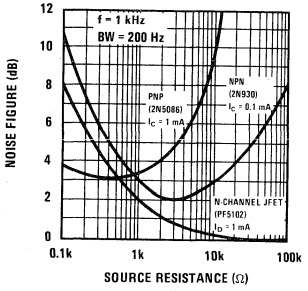
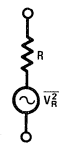


FIGURE 1. Bipolar and JFET Transistor Noise Comparison

REVIEW OF BASICS

Before guidelines are established for designing low noise JFET amplifiers, a method of noise characterization must be chosen. Designers are confronted with a multitude of different noise parameters such as Noise Figure (NF), noise voltage and current densities, noise temperature, noise resistance, etc. Designers are primarily concerned with signal to noise (S/N) ratios preferring noise voltage, (e_n) and current (i_n) density.

Noise generally manifests itself in three forms: thermal noise, shot noise and flicker or "1/f" noise. Thermal noise arises from thermal agitation of electrons in a conductor and is given by Nyquist's relation:



$$\overline{V_R^2} = 4k\,T\,R\,\Delta f \qquad (1)$$

$\overline{V_R^2}$ = mean square noise voltage
k = Boltzmann constant (1.38×10^{-23} VAS/°K)
T = Absolute temperature (°K)
R = Resistance in ohms
Δf = Noise bandwidth (Hz)

The noise of a resistor may be represented as a spectral density (V^2/Hz) or more commonly in $\mu V/\sqrt{Hz}$ or $nV/\sqrt{Hz}$ and is given by:

$$e_{nR} = (\overline{V_R^2}/\Delta f)^{1/2} \qquad (2)$$

It is sometimes more convenient to represent thermal noise as noise current instead of a noise voltage. One needs only to consider the Norton equivalent yielding a noise current density.

$$i_{nR} = \frac{e_{nR}}{R} = \left(\frac{4\,kT}{R}\right)^{1/2} \qquad (3)$$

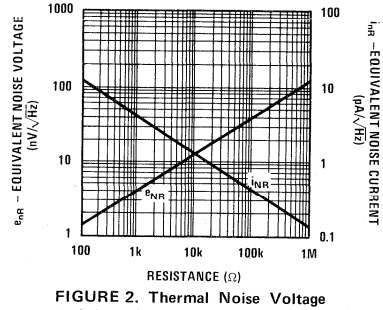


FIGURE 2. Thermal Noise Voltage and Current Densities vs Resistance.

The second basic form of noise, shot noise, is due to the randomness of current flow (discrete charge particles) in semiconductor P-N junctions.

$$\overline{i^2} = 2\,q\,I_{DC}\,\Delta f \qquad (4)$$

$\overline{i^2}$ = Mean square noise current
q = Charge of an electron (1.6×10^{-19} AS)
I_{DC} = dc current flowing through the junction (A)
Δf = Noise bandwidth (Hz)

As with thermal noise, shot noise may be represented as a current density (A^2/Hz) or $pA/\sqrt{Hz}$.

$$i_n = (\overline{i^2}/\Delta f)^{1/2} \qquad (5)$$

It should be noted that both thermal noise and shot noise are "white" noise sources, i.e., frequency independent.

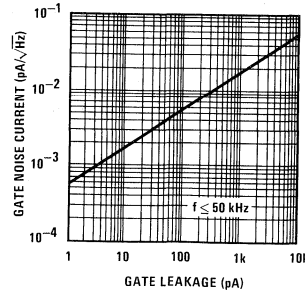


FIGURE 3. Current Noise vs Gate Leakage Current

The third basic noise source confronting designers is flicker or "1/f" noise whose density is roughly inversely proportional to frequency starting at about 1 kHz in both JFETs and bipolar transistors and increasing as frequency is decreased. Through careful processing, flicker noise in JFETs has been reduced to levels nearly insignificant to the designer. Flicker noise in JFETs is primarily a noise voltage and is source independent. Flicker noise in bipolar transistors is a function of base and leakage currents increasing with increased source impedance or operating currents.

A simple noise model of a JFET or any amplifying device may be constructed using a thermal and shot noise source which would adequately describe its noise performance allowing signal to noise ratios to be calculated directly.

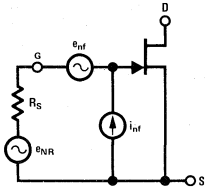


FIGURE 4. Simple JFET Noise Model

The input noise per unit bandwidth at some frequency may be calculated from the mean square sum of the noise sources (assuming the JFET noise sources are uncorrelated or independent of one another).

$$e_{nt}^2 = e_{nR}^2 + e_{nf}^2 + i_{nf}^2 R_s^2 \quad (6)$$

The total noise in the same bandwidth Δf, where the noise sources are independent of frequency, is simply:

$$V_{NOISE} = (e_{nt}^2 \Delta f)^{1/2} \quad (7)$$

Practically, noise sources are not frequency independent except resistor noise with no dc bias. The total input noise for the nonideal case may be calculated by breaking the spectrum up into several small bands and calculating the noise in each band where the noise sources are nearly frequency independent. The total input noise would then be the RMS sum of the noise in each of the bands N1 . . . Nn.

$$V_{NOISE} = (V_{N1}^2 + V_{N2}^2 + \ldots V_{Nn}^2)^{1/2} \quad (8)$$

THE DESIGN PROCESS

The final circuit configuration and suitable JFET will be determined by the external circuit constraints.

1) Minimum signal to noise ratio (maximum amplifier noise)
2) Type and magnitude of source impedance (resistive or reactive)
3) Amplifier input impedance requirements
4) Bandwidth and maximum frequency of interest
5) Maximum operating temperature
6) Stage gain
7) Power supply voltage and current limitations
8) Circuit configuration, single or dual device

The design procedure is dependent on the type of source and each case must be considered separately. Resistive sources will be considered first because they are the least restrictive for the preamplifier.

Resistive Sources

Preamplifiers for resistive sources are typically voltage amplifiers requiring a fixed input resistance and capacitance consistent with the maximum frequency of interest and source resistance. In most cases a resistor of the desired value connected between the gate and ground will satisfy the input resistance requirement leaving the maximum input capacitance as the major concern.

The maximum amplifier input capacitance is a function of the JFET source resistor, input resistance, source capacitance and maximum frequency. The maximum allowable input capacitance will be used in eliminating unsuitable JFET geometrics and optimizing the circuit configuration. Sometimes the JFET geometry (or type) with the lowest noise may also have an input capacitance that makes it unsuitable. The JFET input capacitance should be considered before noise in high source resistance, wideband amplifier designs.

$$C_{in} \cong C_{rs}\left(1 + \frac{gm\ R_D}{1 + gm\ R_s}\right) + \frac{C_{gs}^*}{1 + gm\ R_s} \quad (9)$$

$^*C_{gs} = C_{is} - C_{rs}$

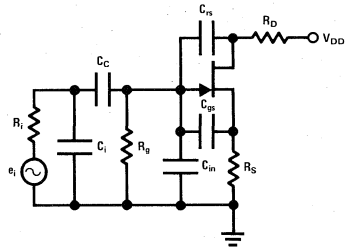


FIGURE 5. A Typical Resistive Source JFET Amplifier

If low input capacitance is required, a cascode configuration minimizes input capacitance and still allows high gain within a device type. The cascode configuration can also be used to reduce the voltage across a device, reducing device heating (for high current operation) and gate leakage currents when source impedances are very high.

Once the basic circuit configuration has been decided upon or dictated by gain, bandwidth and power supply limitations, the final JFET selection will be on noise. Redrawing the amplifier in *Figure 4* with all of the noise sources, the total amplifier noise per unit bandwidth can be found.

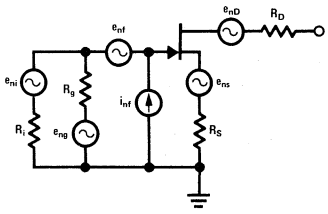


FIGURE 6. A Typical Resistive Source JFET Amplifier with Noise Sources

$$e_{nt} = \left[e_{nig}^2 + e_{nf}^2 + e_{ns}^2 + \frac{e_{nD}^2}{A_V^2} + i_n^2 \ (R_i // R_g)^2 \right]^{1/2} \quad (10)$$

where: e_{nig}^2 = The noise of the parallel connection of R_i and R_g

e_{nf}^2 = The noise voltage of the JFET

e_{ns}^2 = The noise of the source resistor R_s

$\frac{e_{nD}^2}{A_V^2}$ = The noise at the drain (thermal noise of the load plus the second stage noise)

$i_n^2 (R_i // R_g)^2$ = The current noise contribution of the JFET

When the amplifier is operated at room temperature and moderate drain voltages, the current noise term is usually negligible with source resistances as high as 10 MΩ. Depending on the voltage gain of the stage, the drain circuit noise may be negligible, simplifying the input noise expression.

$$e_{nt} = (e_{nig}^2 + e_{nf}^2 + e_{ns}^2)^{1/2} \quad (11)$$

The final JFET selection will be based on the noise requirements from the maximum allowable noise V_{MAX}.

$$V_{MAX} = (e_{nf}^2 + e_{ns}^2)^{1/2} \quad (12)$$

Depending on V_{MAX} and e_{nf}^2 the source resistor may have to be bypassed to ground to eliminate noise of the bias resistor.

Capacitive Sources

Preamplifiers for capacitive sources are primarily current amplifiers requiring very high input resistance and controlled input capacitance to match the source capacitance.

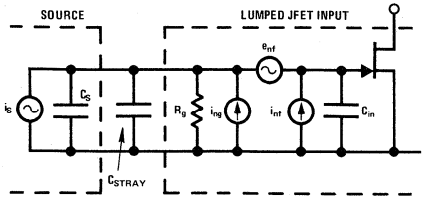


FIGURE 7. JFET Preamplifier with a Capacitive Source

The source capacitance should equal the sum of the preamplifier input capacitance and the stray capacitance for maximum frequency response and power transfer from the signal source. Assuming the gate resistor, R_g, is so large as to not load the capacitive source, the input noise voltage is:

$$e_{nt} \cong \left[e_{nf}^2 + (i_{nf}^2 + i^2{}_{ng}) \left(\frac{R_g{}^2}{(1 + \omega^2 R_g{}^2 C^2)} \right) \right]^{1/2} \quad (13)$$

where $C = C_S + C_{in}$

with an input signal of

$$e_s \cong i_s \left(\frac{R_g{}^2}{1 + \omega^2 R_g{}^2 C^2} \right)^{1/2} \quad (14)$$

When the source and input capacitance are matched, the final JFET geometry will be selected on two criteria: the noise voltage, e_n, and the current noise from the gate leakage, $I_{G(ON)}$, to optimize the signal to noise ratio. As in the resistive source case, the circuit configuration and JFET selection is an iterative process using all of the external circuit constraints and device parameters and limitations.

Inductive Sources

Amplifiers designed for inductive sources (including transformers) require fixed input resistances (as in the resistive source case) and controlled input capacitance (as in the capacitive source case). The input noise per unit bandwidth will rise with increasing frequency to a maximum value at resonance of the inductive source and the input capacitance or when the shunt resistance of the inductor is larger than the input resistance of the amplifier.

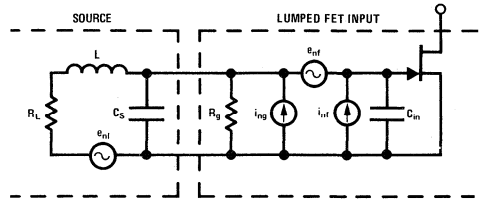


FIGURE 8. JFET Amplifier with an Inductive Source

The inductive source amplifier is the most difficult to analyze due to the complex input impedance. The input noise per unit bandwidth is given by:

$$e_{nt}^2 = e_{nf}^2 + (i_{nf}^2)(|Z_{in}|^2) + 4\,kT\,(Re\,(Z_{in})) \quad (15)$$

where $Z = X_{CIN} // R_g$

and $Z_{in} = Z // (Z_L + R_L)$

Usually the current noise of the JFET is negligible, simplifying the expression a little, but not much. The optimization process for inductive sources is very complex and it will require the spectrum to be broken up into several small bands to arrive at a final design. Generally, a JFET with a minimum noise voltage will be the proper choice.

Transformers may be used with JFET amplifiers to minimize noise with very low source impedances. Transformers have both drawbacks and advantages and both must be examined before a transformer design is chosen. Poor frequency response, susceptibility to mechanical and magnetic pickup and thermal noise head the list of disadvantages to be weighed against two very important advantages. First, the noise voltage is transformed by the turns ratio N; second, the resistance is transformed by N^2. These can be used to advantage by matching very low values of source resistance to a relatively noisy amplifier and still maintaining a good signal to noise ratio, i.e., the total noise at the source assuming an ideal transformer is

$$e_{nt}^2 = e_{nRs}^2 + \frac{e_{nAmp}^2}{N^2} \qquad (16)$$

SUMMARY

Low noise amplifier design concepts have been introduced for the three basic types of sources. Basic parameters (C_{in}, e_n, gm) were discussed that affect both circuit configuration and JFET type. There is no universal low noise JFET or circuit configuration that solves all problems. Each low noise amplifier design is different and must be considered within its own framework of performance requirements.

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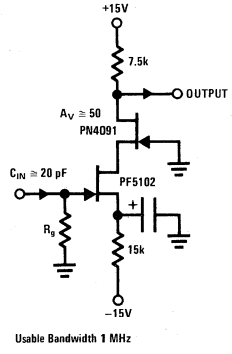
A. Van der Ziel, "Noise," Prentice-Hall, 1954.

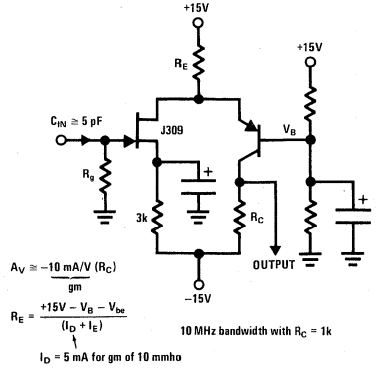
Richard S.C. Cobbold, "Theory and Applications of Field-Effect Transistors," John Wiley & Sons, 1970.

C.D. Motchenbacher and F.C. Fitchen, "Low Noise Electronic Design," John Wiley & Sons, 1973.

SOME PRACTICAL LOW NOISE JFET INPUT CIRCUITS



a) Wide Band, Low Input Capacitance, Very Low Noise Preamplifier



b) Low Noise, Very Low Input Capacitance Video Amplifier

APPENDIX A

Important National JFET Process Parameter Guide

Test Conditions V_{DS} = 15V, I_D = 1 mA (V_{GS} = 0V)*

PROCESS	e_n @ 10 Hz (nV/$\sqrt{Hz}$)	e_n @ 1 kHz (nV/$\sqrt{Hz}$)	e_n @ 100 kHz (nV/$\sqrt{Hz}$)	g_{fs} (mmho)	$I_{G(ON)}$ (pA)	C_{GD} (pF)	C_{GS} (pF)
50	15	5	2.5	3	5V 2 pA 10V 10 pA 15V 1 nA	0.7	2.5
51	5	3	1.3	7	30	3	9
55	10	4	2.5	2.4	5	2	4
92	10	4	1.5	4.5	10V 20 pA 15V 1 nA	2	4
83	10	5	2.5	2	5	1	2.5
84*	50	15	9	0.2	0.1	0.01	2
94	10	5	2.5	2	1–2	0.01	4
95	10	4	2.5	1.5	15	3.5	15
96	5	3	1.3	7	30	3	9
93	15	7	2	3.5	10V 20 pA 15V 1 nA	1	3.2

National JFET Process Low Noise Amplifier Guide

PROCESS	50	51	55	92	83	84	93	94	95	96
Low Noise Application	Single JFET				Dual JFET					
Resistive Ultra-Low $e_n < 5$ nV/$\sqrt{Hz}$ @ 10 Hz		X								X
Resistive Low Freq < 20 kHz		X	X		X			X	X	X
Resistive Wideband < 10 MHz	X	X		X	X		X	X	X	X
Resistive Wide Band > 10 MHz	X			X			X			
Resistive Very High $R_S > 10$ MΩ	X					X		X		
Capacitive Low C < 10 pF	X		X	X	X	X	X	X		
Capacitive High C > 20 pF		X	X						X	X
Inductive	X	X	X	X	X	X	X	X	X	X

APPENDIX B

NOISE PARAMETER CONVERSION

Noise Figure (NF) to an Effective e_n

It is more convenient to present noise data for bipolar transistors in the form of contours of constant noise figure at a fixed frequency or plots of noise figure versus frequency at a fixed source resistance due to large values of noise current (i_n). Noise figure must be converted to an effective noise voltage (e_{nE}) for comparisions to be made between a BJT and a JFET or for signal to raise ratio calculations.

By definition:

$$NF = 10 \log \frac{\text{Total Output Noise Power}}{\text{Output Noise Power of the Source}} \qquad \text{(B1)}$$

From equations 1 and 2, one finds the source noise power to be

$$\text{Source Noise Power} = \frac{e_{nR}^2 \, \Delta f}{R_S} \qquad \text{(B2)}$$

for some source resistance R_S.

Referring to *Figure 4*, the total output noise power at the input of the amplifier would be:

$$\text{Total Output Noise Power} = \frac{e_{nR}^2 \, \Delta f}{R_S} + \frac{e_{nf}^2 \, \Delta f}{R_S} + i_{nf}^2 \, R_S^2 \, \Delta f \qquad \text{(B3)}$$

The noise figure (NF) can now be expressed in terms of the noise source generators, e_{nR}, e_{nf} and i_{nf} allowing an expression to convert noise figure (NF) to an effective noise voltage (e_{nE}).

$$NF = 10 \log \left(1 + \frac{e_{nf}^2 + i_{nf}^2 \, R_S^2}{e_{nR}^2} \right) \qquad \text{(B4)}$$

yielding

$$e_{nf}^2 + i_{nf}^2 \, R_S^2 = e_{nE}^2 = (10^{NF/10} - 1) \; e_{nR}^2 \qquad \text{(B5)}$$

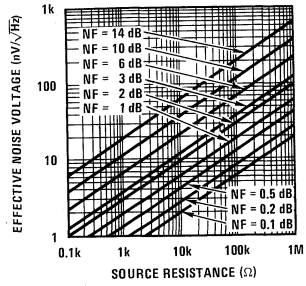


FIGURE B1. Effective Noise Voltage (e_{nE}) vs Noise Figure and Source Resistance (R_S)

Noise Resistance

The effective noise voltage density (e_n) and noise current density (i_n) are found directly by referring to *Figure 1*, and reading the values for the corresponding resistances.

$$e_{nR} = (4 \, KTR)^{1/2} \qquad (1)$$

$$i_{nR} = \left(\frac{4 \, KT}{R} \right)^{1/2} \qquad (3)$$

APPENDIX C

JFET Current Noise

At low frequencies the current noise and voltage noise sources are uncorrelated in JFETs with the current noise being pure shot noise due to gate leakage currents. As frequency is increased, the current noise also increases starting at frequencies as low as 50 kHz in some high capacitance device types.

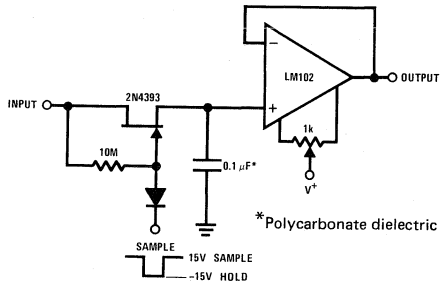
It has been suggested and experimentally verified that the noise current at high frequencies is due to increased gate input conductance.

$$i_n^2 = 4 \, KT \left[\text{Re} \, (Y_{11}) \right]^{-1} \qquad \text{(C1)}$$

Re (Y_{11}) is available on high frequency JFET data sheet as the real portion of the common source input admittance parameters. In effect the channel noise is coupling to the gate circuit through the source-gate and drain gate capacitances. Hence low capacitance devices exhibit lower values of noise current at high frequencies than do high capacitance devices.

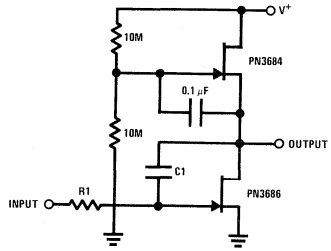
FET Circuit Applications

National Semiconductor
Application Note 32
April 1977



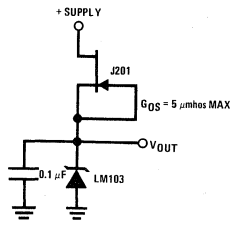
Sample and Hold With Offset Adjustment

The 2N4393 JFET was selected because of its low I_{GSS} (<100 pA), very low $I_{D(OFF)}$ (<100 pA) and low pinchoff voltage. Leakages of this level put the burden of circuit performance on clean, solder-resin free, low leakage circuit layout.



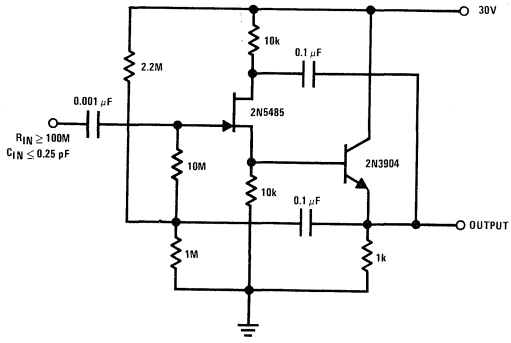
JFET AC Coupled Integrator

This circuit utilizes the "μ-amp" technique to achieve very high voltage gain. Using C1 in the circuit as a Miller integrator, or capacitance multiplier, allows this simple circuit to handle very long time constants.



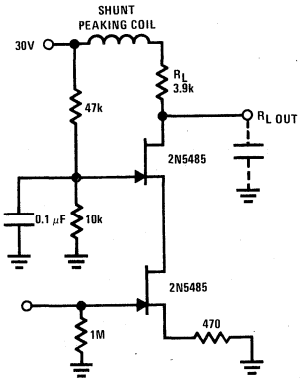
Low Power Regulator Reference

This simple reference circuit provides a stable voltage reference almost totally free of supply voltage hash. Typical power supply rejection exceeds 100 dB.



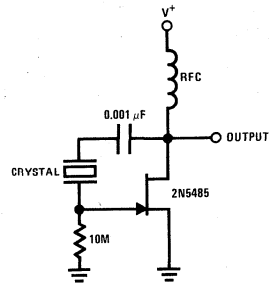
Ultra-High Z_{IN} AC Unity Gain Amplifier

Nothing is left to chance in reducing input capacitance. The 2N5485, which has low capacitance in the first place, is operated as a source follower with bootstrapped gate bias resistor and drain.



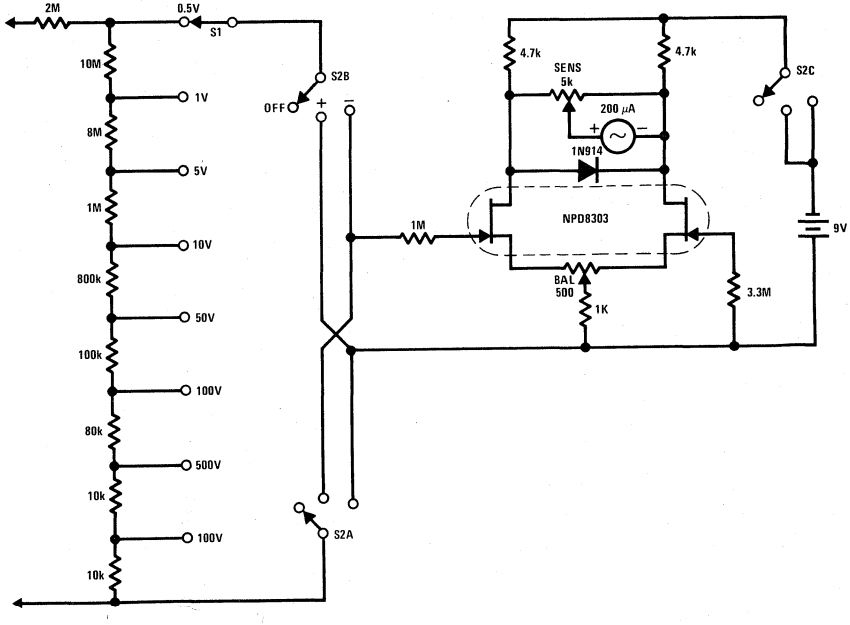
FET Cascode Video Amplifier

The FET cascode video amplifier features very low input loading and reduction of feedback to almost zero. The 2N5485 is used because of its low capacitance and high Y_{fs}. Bandwidth of this amplifier is limited by R_L and load capacitance.



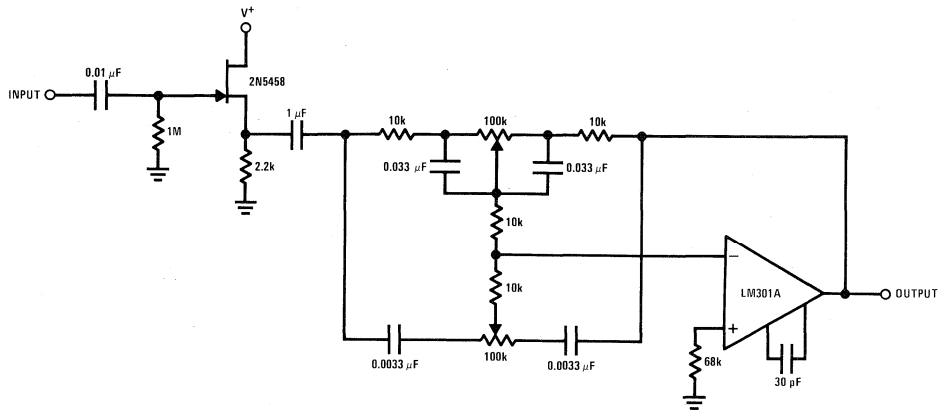
JFET Pierce Crystal Oscillator

The JFET Pierce crystal oscillator allows a wide frequency range of crystals to be used without circuit modification. Since the JFET gate does not load the crystal, good Q is maintained, thus insuring good frequency stability.



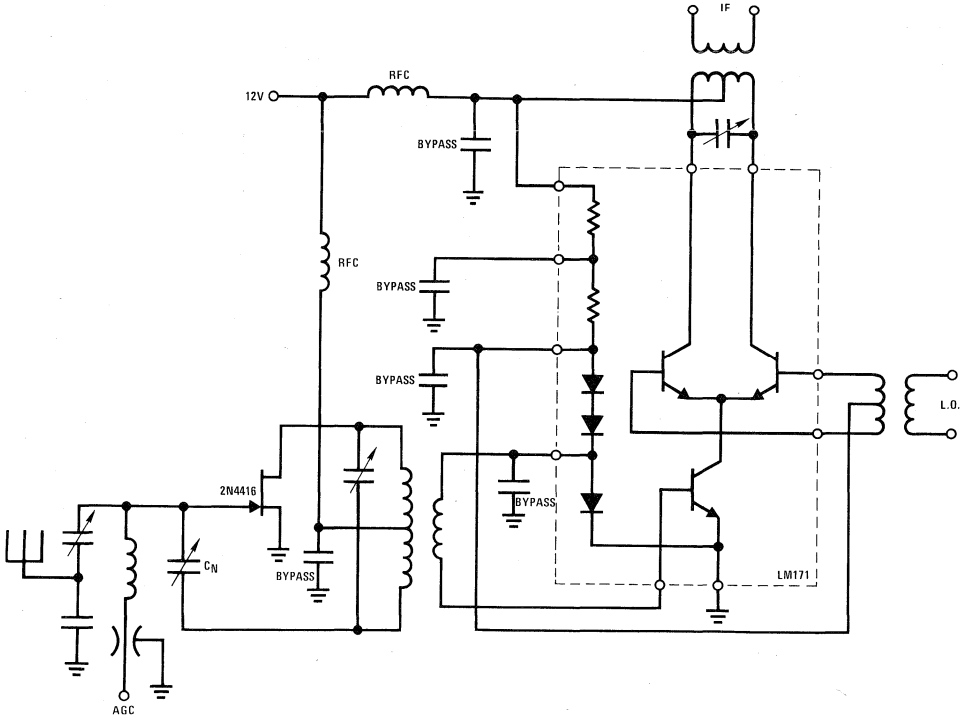
FETVM—FET Voltmeter

This FETVM replaces the function of the VTVM while at the same time ridding the instrument of the usual line cord. In addition, drift rates are far superior to vacuum tube circuits allowing a 0.5V full-scale range which is impractical with most vacuum tubes. The low leakage, low noise NPD8303 is an ideal device for this application.



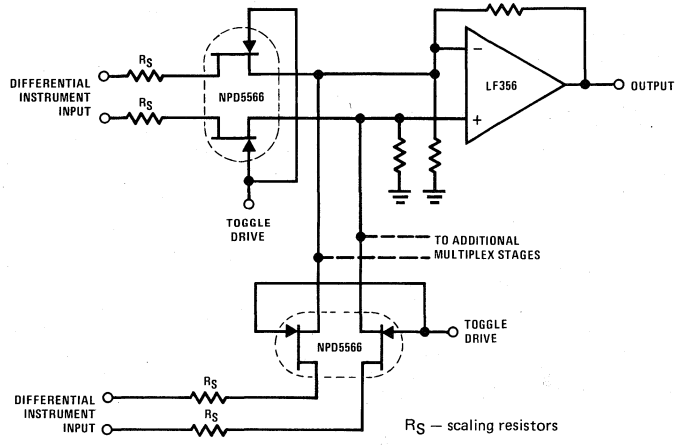
HI-FI Tone Control Circuit (High Z Input)

The 2N5458 JFET provides the function of a high input impedance and low noise characteristics to buffer an op amp-operated feedback type tone control circuit.



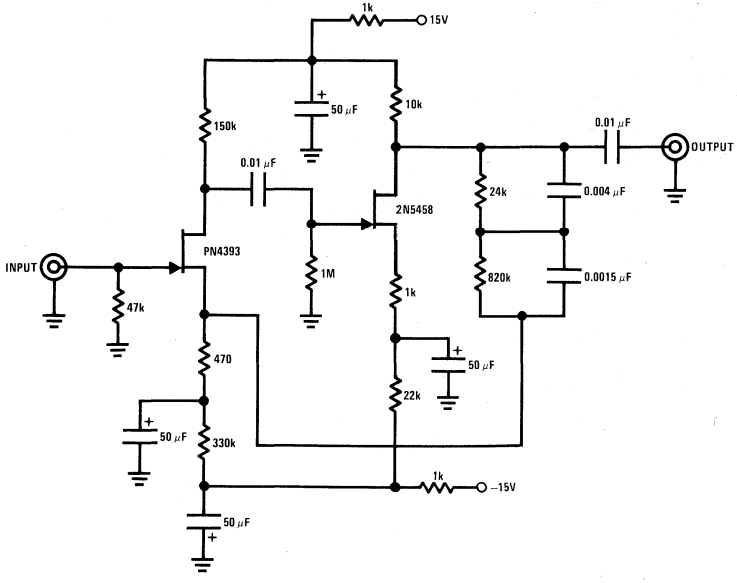
100 MHz Converter

The 2N4416 JFET will provide noise figures of less than 3 dB and power gain of greater than 20 dB. The JFET's outstanding low crossmodulation and low intermodulation distortion provides an ideal characteristic for an input stage. The output feeds into an LM171 used as a balanced mixer. This configuration greatly reduces L.O. radiation both into the antenna and into the IF strip and also reduces RF signal feedthrough.



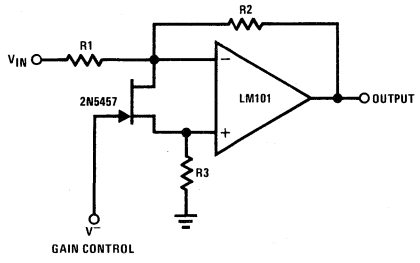
Differential Analog Switch

The NPD5566 monolithic dual is used in a differential multiplexer application where $R_{DS(ON)}$ should be closely matched. Since $R_{DS(ON)}$ for the monolithic dual tracks at better than ±1% over wide temperature ranges (−25°C to +125°C), this makes it an unusual but ideal choice for an accurate multiplexer. This close tracking greatly reduces errors due to common-mode signals.



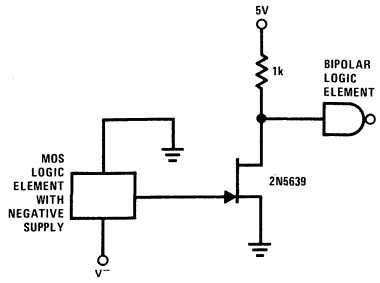
Magnetic Pickup Phono Preamplifier

This preamplifier provides proper loading to a reluctance phono cartridge. It provides approximately 35 dB of gain at 1 kHz (2.2 mV input for 100 mV output), it features S + N/N ratio of better than −70 dB (referenced to 10 mV input at 1 kHz) and has a dynamic range of 84 dB (referenced to 1 kHz). The feedback provides for RIAA equalization.



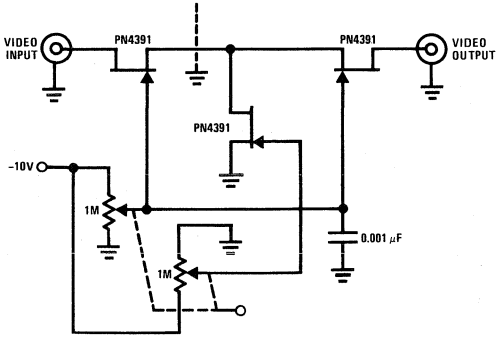
Voltage Controlled Variable Gain Amplifier

The 2N5457 acts as a voltage variable resistor with an $R_{DS(ON)}$ of 800Ω max. Since the differential voltage on the LM101 is in the low mV range, the 2N5457 JFET will have linear resistance over several decades of resistance providing an excellent electronic gain control.



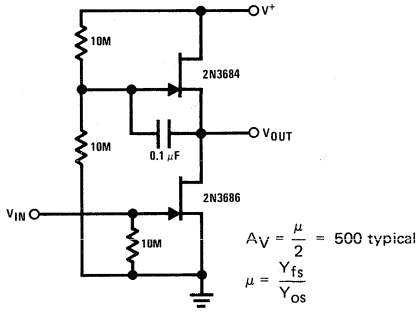
Negative to Positive Supply Logic Level Shifter

This simple circuit provides for level shifting from any logic function (such as MOS) operating from minus to ground supply to any logic level (such as TTL) operating from a plus to ground supply. The 2N5639 provides a low $r_{ds(ON)}$ and fast switching times.



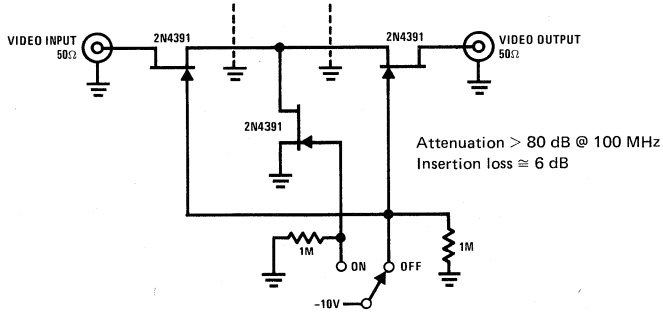
Variable Attenuator

The PN4391 provides a low $R_{DS(ON)}$ (less than 30Ω). The tee attenuator provides for optimum dynamic linear range for attenuation and if complete turn-off is desired, attenuation of greater than 100 dB can be obtained at 10 MHz providing proper RF construction techniques are employed.



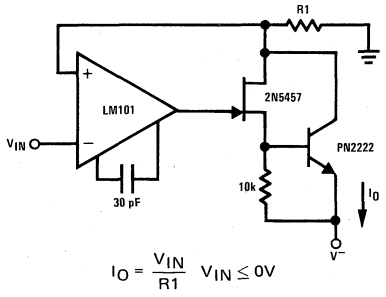
Ultra-High Gain Audio Amplifier

Sometimes called the "JFET μ-amp", this circuit provides a very low power, high gain amplifying function. Since μ of a JFET increases as drain current decreases, the lower drain current is, the more gain you get. You do sacrifice input dynamic range with increasing gain, however.



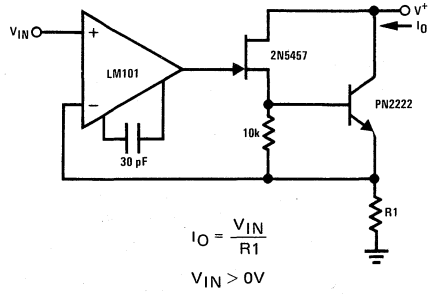
High Frequency Switch

The 2N4391 provides a low ON resistance of 30Ω and a high OFF impedance (<0.2 pF) when OFF. With proper layout and an "ideal" switch, the performance stated above can be readily achieved.



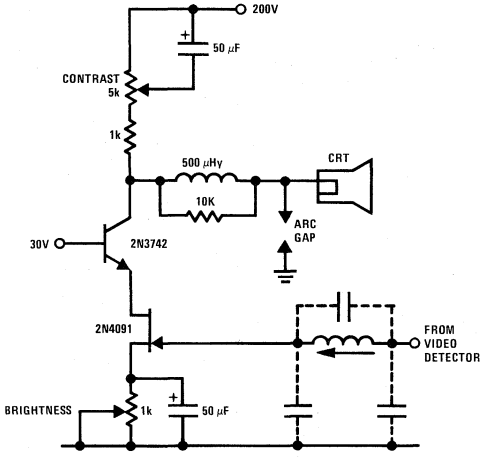
Precision Current Source

The 2N5457 and PN2222 bipolar serve as voltage isolation devices between the output and the current sensing resistor, R1. The LM101 provides a large amount of loop gain to assure that the circuit acts as a current source. For small values of current (<1 mA), the PN2222 and 10k resistor may be eliminated with the output appearing at the source of the 2N5457.



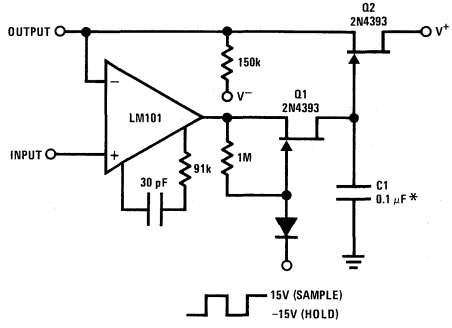
Precision Current Sink

The 2N5457 JFET and PN2222 bipolar have inherently high output impedance. Using R1 as a current sensing resistor to provide feedback to the LM101 op amp provides a large amount of loop gain for negative feedback to enhance the true current sink nature of this circuit. For small current values, the 10k resistor and PN2222 may be eliminated if the source of the JFET is connected to R1.



JFET–Bipolar Cascode Circuit

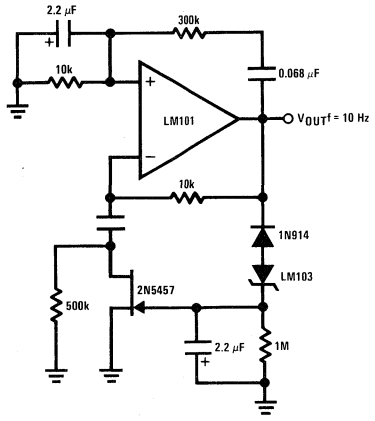
The JFET-bipolar cascode circuit will provide full video output for the CRT cathode drive. Gain is about 90. The cascode configuration eliminates Miller capacitance problems with the 2N4091 JFET, thus allowing direct drive from the video detector. An m derived filter using stray capacitance and a variable inductor prevents 4.5 MHz sound frequency from being amplified by the video amplifier.



*Polycarbonate dielectric capacitor

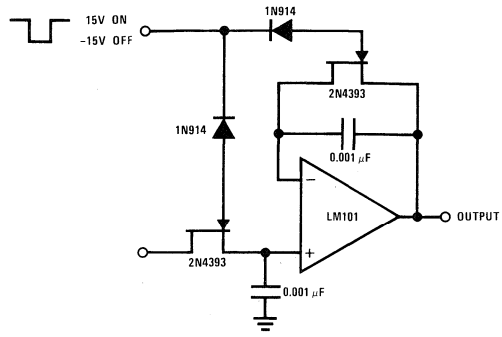
Low Drift Sample and Hold

The JFETs, Q1 and Q2, provide complete buffering to C1, the sample and hold capacitor. During sample, Q1 is turned ON and provides a path, $r_{ds(ON)}$, for charging C1. During hold, Q1 is turned OFF, thus leaving Q1 $I_{D(OFF)}$ (<100 pA) and Q2 I_{GSS} (<100 pA) as the only discharge paths. Q2 serves a buffering function so feedback to the LM101 and output current are supplied from its source.



Peak output voltage
$V_p \cong V_z + 1V$

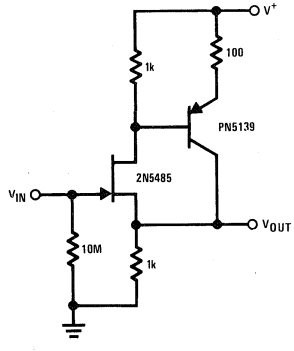
Wien Bridge Sine Wave Oscillator



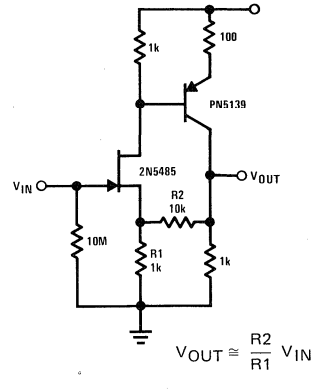
JFET Sample and Hold Circuit

The major problem in producing a low distortion, constant amplitude sine wave is getting the amplifier loop gain just right. By using the 2N5457 JFET as a voltage variable resistor in the amplifier feedback loop, this can be easily achieved. The LM103 zener diode provides the voltage reference for the peak sine wave amplitude; this is rectified and fed to the gate of the 2N5457, thus varying its channel resistance and, hence, loop gain.

The logic voltage is applied simultaneously to the sample and hold JFETs. By matching input impedance and feedback resistance and capacitance, errors due to $r_{ds(ON)}$ of the JFETs is minimized.



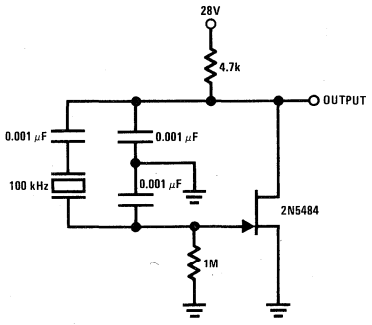
High Impedance Low Capacitance Wideband Buffer



High Impedance Low Capacitance Amplifier

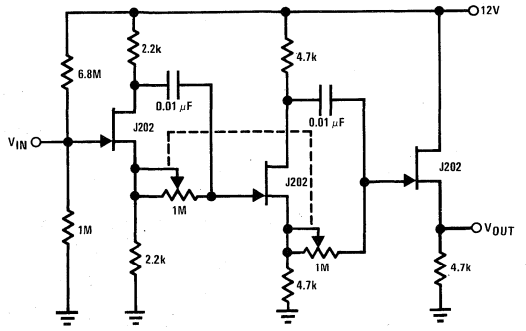
The 2N5485 features low input capacitance which makes this compound series-feedback buffer a wide-band unity gain amplifier.

This compound series-feedback circuit provides high input impedance and stable, wide-band gain for general purpose video amplifier applications.



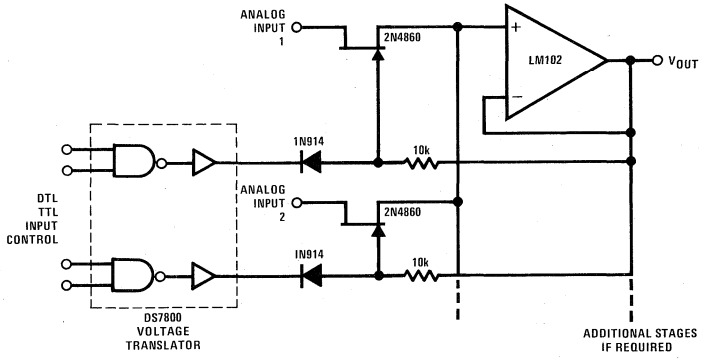
Stable Low Frequency Crystal Oscillator

This Colpitts-Crystal oscillator is ideal for low frequency crystal oscillator circuits. Excellent stability is assured because the 2N5484 JFET circuit loading does not vary with temperature.



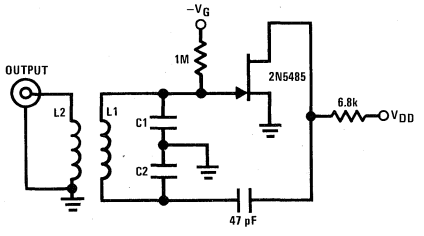
0 to 360° Phase Shifter

Each stage provides 0° to 180° phase shift. By ganging the 2 stages, 0° to 360° phase shift is achieved. The J202 JFETs are ideal since they do not load the phase shift networks.



DTL-TTL Controlled Buffered Analog Switch

This analog switch uses the 2N4860 JFET for its 25Ω r_{ON} and low leakage. The LM102 serves as a voltage buffer. This circuit can be adapted to a dual trace oscilloscope chopper. The DS7800 monolithic IC provides adequate switch drive controlled by DTL/TTL logic levels.



20 MHz oscillator values

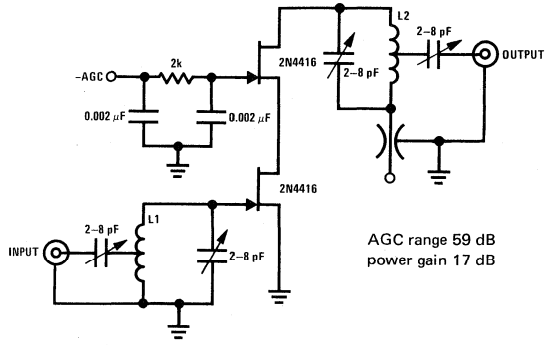
C1 ≅ 700 pF L1 = 1.3 μH
C2 = 75 pF L2 = 10T 3/8" dia 3/4" long
V_{DD} = 16V I_D = 1 mA

20 MHz oscillator performance

Low distortion 20 MHz osc
2nd harmonic — 60 dB
3rd harmonic > —70 dB

Low Distortion Oscillator

The 2N5485 JFET is capable of oscillating in a circuit where harmonic distortion is very low. The JFET local oscillator is excellent when a low harmonic content is required for a good mixer circuit.

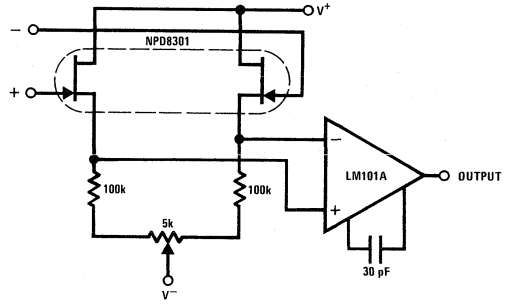


AGC range 59 dB
power gain 17 dB

L1 = 0.07 μHy center tap
L2 = 0.07 μHy tap 1/4 up from ground

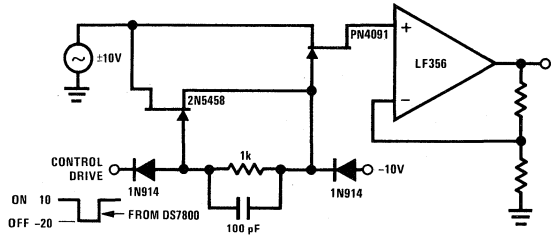
200 MHz Cascode Amplifier

This 200 MHz JFET cascode circuit features low cross-modulation, large signal handling ability, no neutralization, and AGC controlled by biasing the upper cascode JFET. The only special requirement of this circuit is that I_{DSS} of the upper unit must be greater than that of the lower unit.



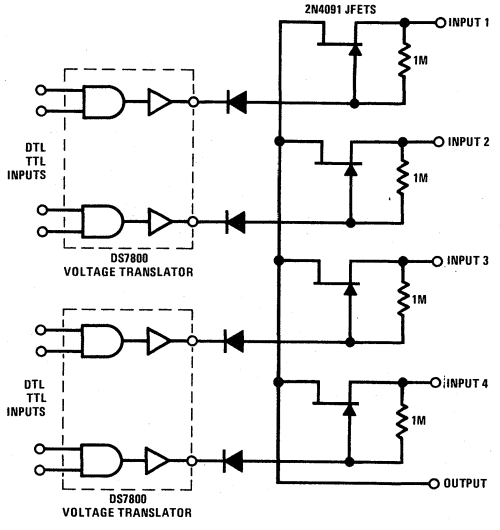
FET Op Amp

The NPD8301 monolithic-dual provides an ideal low offset, low drift buffer function for the LM101A op amp. The excellent matching characteristics of the NPD8301 track well over its bias current range, thus improving common-mode rejection.



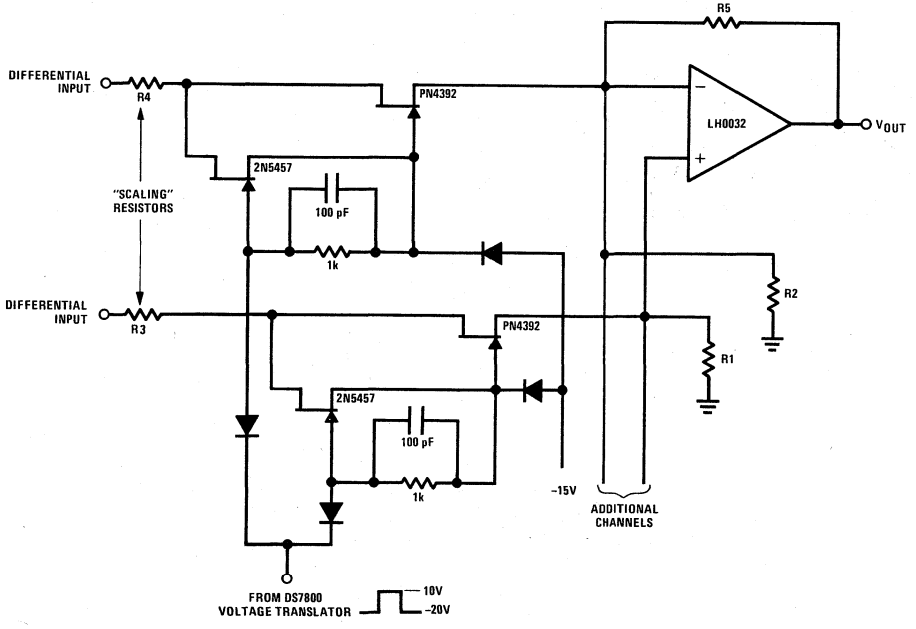
High Toggle Rate High Frequency Analog Switch

This commutator circuit provides low impedance gate drive to the PN4091 analog switch for both ON and OFF drive conditions. This circuit also approaches the ideal gate drive conditions for high frequency signal handling by providing a low AC impedance for OFF drive and high AC impedance for ON drive to the PN4091.



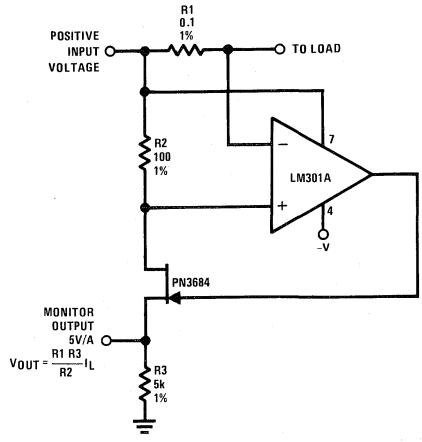
4-Channel Commutator

This 4-channel commutator uses the 2N4091 to achieve low channel ON resistance (<30Ω) and low OFF current leakage. The DS7800 voltage translator is a monolithic device which provides from 10V to −20V gate drive to the JFETs while at the same time providing DTL/TTL logic compatability.



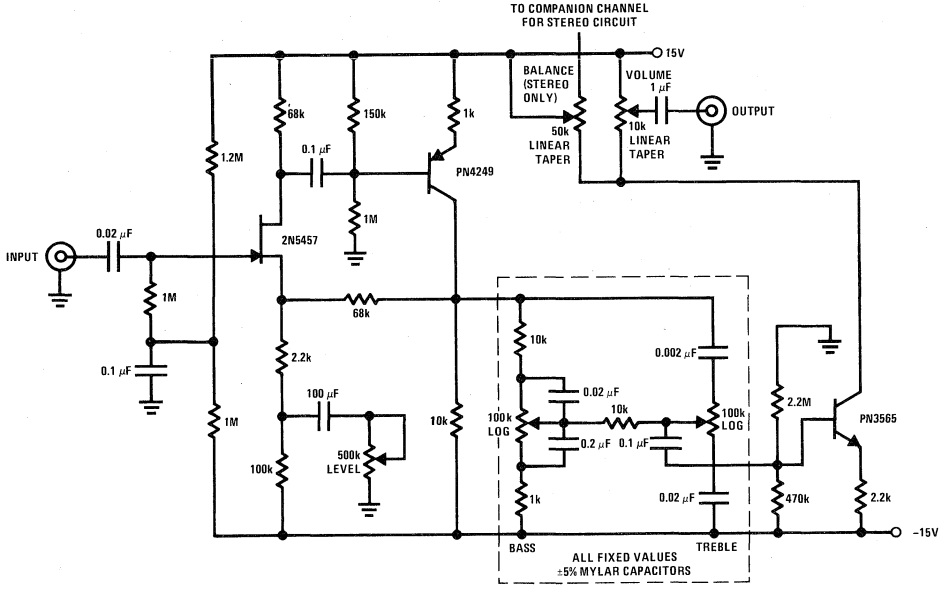
Wide Band Differential Multiplexer

This design allows high frequency signal handling and high toggle rates simultaneously. Toggle rates up to 1 MHz and MHz signals are possible with this circuit.



Current Monitor

R1 senses current flow of a power supply. The JFET is used as a buffer because $I_D = I_S$, therefore the output monitor voltage accurately reflects the power supply current flow.



Low Cost High Level Preamp and Tone Control Circuit

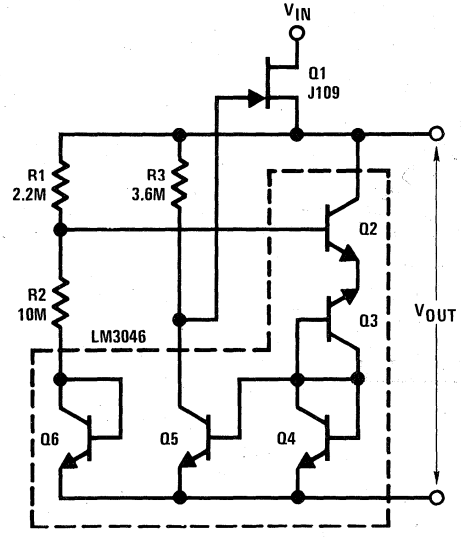
This preamp and tone control uses the JFET to its best advantage; as a low noise high input impedance device. All device parameters are non-critical, yet the circuit achieves harmonic distortion levels of less than 0.05% with an S/N ratio of over 85 dB. The tone controls allow 18 dB of cut and boost; the amplifier has a 1V output for 100 mV input at maximum level.

A Novel FET Micropower Voltage Regulator

National Semiconductor
John Maxwell
February 1977

Many systems require a stable voltage supply to maintain constant performance. When these systems are battery-operated, a regulator is needed to stabilize the system voltage as the battery decays with time. Unfortunately, IC voltage regulators require several milliamps of quiescent current, making them impractical for micropower applications. Zener diodes may also be impractical because of short term peak current requirements of the system. This could require additional buffering or high standby currents, but both increase the battery drain. An inexpensive micropower voltage regulator is needed to fill the gap between IC regulators (high quiescent current) and zener diodes (high standby current).

Instead of the tranditional bipolar approach, the regulator shown in *Figure 1* uses a JFET as the series pass element. This offers several advantages: first, no pre-regulation is needed for the pass element as with an NPN because the drive comes from the regulated output. Next, the gate-source is isolated from the line via the drain, thus offering excellent line regulation. This is not the case with PNP pass elements, where the emitter is the input. Finally, and possibly the most important feature for micropower regulators, is FETs require no current drive.



Output Voltage

$$V_{OUT} = V_{BE}\left(2 + \frac{R1}{R2}\right) + BV_{EB}\left(1 + \frac{R1}{R2}\right)$$

Drift

$$\frac{\partial V_{OUT}}{\partial T} = \frac{\partial V_{BE}}{\partial T}\left(2 + \frac{R1}{R2}\right) + \frac{\partial BV_{EB}}{\partial T}\left(1 + \frac{R1}{R2}\right)$$

Quiescent Current $\simeq 4\ \mu A$

FIGURE 1. Micropower Regulator

The emitter-base breakdown voltage of Q3 is used as a reference (~7.2V) in conjunction with Q2 to form a shunt regulator. The shunt current drives a current mirror, Q4–Q5, which creates the gate drive voltage of the pass FET. The value of the shunt current is determined by R3 and the V_{GS} of the pass FET ($I_{R3} \simeq I_{SHUNT}$). High load currents will reduce the shunt current because the FET V_{GS} is lower. Temperature stability is achieved by cancelling the drift of Q2 and Q3's V_{BE} (~–2 mV/°C/transistor) with the BV_{EB} drift of Q3 (~ 3 mV/°C) resulting in a negative drift at the base of Q2, and the output, of 1 mV/°C.

Selection of the FET requires some care. Ideally, the FET I_{DSS} needs to be greater than the load current at all temperatures (I_{DSS} has a temperature coefficient of ~–0.7%/°C) and the breakdown voltage should be greater than the maximum input voltage. Practically, the FET I_{DSS} needs to be much larger than the maximum load current. Linear operation requires the FET's drain to gate voltage (V_{DG}) to be greater than the pinchoff voltage V_P. By operating the FET at currents much less than I_{DSS}, the gate to source voltage (V_{GS}) will be close to V_P ($V_{GS} = V_P\ (1-(I_D/I_{DSS})^{1/2})$) allowing small drain to source voltages (V_{DS}). For linear operation:

$$|V_{DG}| > |V_P|$$

$$V_{DG} = V_{DS} - V_{GS}$$

It should be noted that N FET's can be paralleled for higher load current requirements without matching the devices.

Actual performance of the regulator is quite good. With a 10V typical output, the line regulation is within ±0.05% for a range of V_{IN}–V_{OUT} of 0.3V to 10V. The load regulation is 0.2% with a load range of 10 μA to 10 mA ($Z_o \simeq 10\Omega$) and the temperature stability is –0.01%/°C (–1 mV/°C). The output voltage can be easily trimmed by adding a pot at the R1R2Q2$_{BASE}$ junction to eliminate BV_{EB} variations or to make the output adjustable over a limited range. Also, the temperature stability can be improved by replacing Q3 with an 8.2V zener diode, because its temperature drift (~ 4 mV/°C) would nearly match the combined V_{BE} drift of Q2 and Q4. The regulator is good enough to be used as a reference in low accuracy (6–7-bit) or limited temperature range applications if current drain is important.

REFERENCES

1. "Voltage Regulator Handbook", National Semiconductor Corporation, May 1975.
2. "Zener Diode Handbook", Motorola, Inc., May 1967.
3. Williams, P., "D.C. Voltage-Reference Circuits with Minimum Input-Output Differentials", Proc. IEEE pp. 1280–1281, December, 1969.

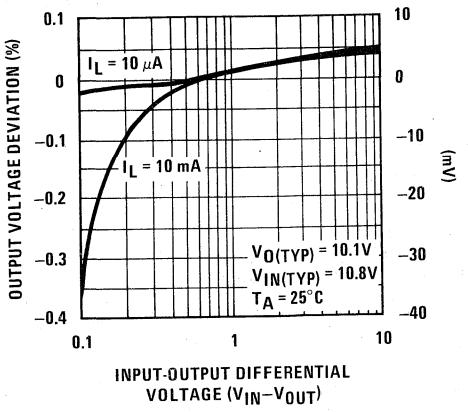


FIGURE 2. Line Regulation vs Input-Output Differential

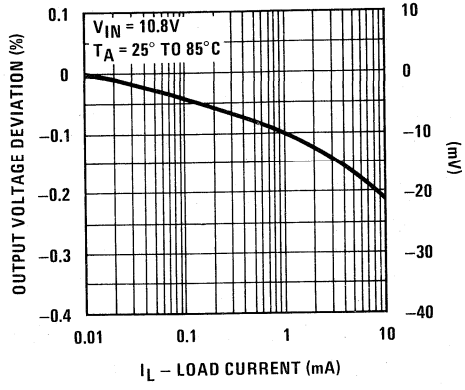


FIGURE 3. Load Regulation

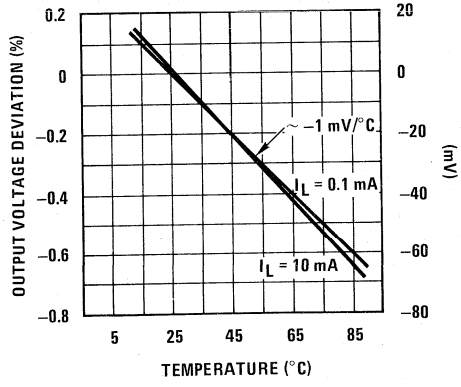


FIGURE 4. Temperature Stability

A Linear Multiple Gain Controlled Amplifier

National Semiconductor
Application Note 129
Jim Sherwin
August 1975

INTRODUCTION

A linear control function over three decades of gain can be achieved with a FET in the feedback path of a non-inverting amplifier. Besides the ultimate simplicity of the circuit, multiple tracking gain control circuits can be constructed with dual op amps and monolithic dual FET's or quad op amps and monolithic quad FET's. Such circuits could even be integrated with ion-implanted FET's on single or multiple monolithic op amp chips. The gain control range may be designed for less than 2 to 1 or higher than 1000:1, but input voltage levels are limited by acceptable levels of distortion. Bandwidth is dependent on maximum gain and unity gain bandwidth of the op amp used. The gain control circuit is especially suitable for volume expansion applications.

GAIN CONTROL WITH FETS

The FET has long been used as a voltage controlled resistor (VCR), often as the shunt arm in the series-shunt attenuator of *Figure 1.* Advantages of the FET as a VCR are that:

1. The control signal is almost perfectly isolated from the controlled signal path, and
2. The resistance can be made to vary over an almost infinite max/min ratio.

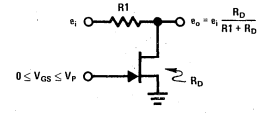


FIGURE 1. Voltage Controlled FET Attenuator

Disadvantages are that:

1. The FET behaves as a linear resistance only for small values of source-drain voltage V_{DS},
2. Non-linearity (of resistance) increases as the control voltage V_{GS} approaches cut-off voltage V_P when the resistance is maximum,
3. The relationship of resistance r_d to V_{GS} is reciprocal rather than direct linear,
4. VCR multiples with matched resistance characteristics over their full control range have been extremely difficult to obtain at any kind of reasonable price, and
5. Production spread in V_P requires separate bias set and gain set on each circuit.

Examination of the FET drain characteristics in *Figure 2* will reveal the essential non-linearity of r_d at high signal levels, especially as V_{GS} approaches V_P. This non-linear region must be avoided in order to achieve tolerable distortion levels. One obvious way is to limit V_{DS} to small values when r_d is high as suggested by *Figures 2c and 2d,* another is to utilize FET's with high V_P as suggested by reference to *Figures 2b and 2d.*

The reciprocal relationship of r_d and V_{GS} is an advantage, as it is precisely that which allows the linear control of gain in the circuit to be described. The availability of matched monolithic dual FET's such as the NSC 2N3958 (watch out for the matched pairs as their resistance match close to V_P may not be as good as that of the monolithic versions) make available low cost duals with very closely matched resistance characteristics over the full control range. There are even some monolithic quads available (such as the AM9709 series). The final problem of the production range of V_P can be much improved with ion-implant diffusion techniques whereby lot variation in V_P may be held to within a few tenths of one volt.

The gain control circuit is that of an ordinary non-inverting op amp with feedback. The usual circuit is modified in *Figure 3a* to include a FET as controlled resistor. The gain function is normal except that r_d replaces R2 in the usual form.

$$A_V = 1 + \frac{R1}{r_d} \tag{1}$$

Now r_d can be equated to a control voltage V_C as follows:

$$r_d = r_o \frac{V_P}{V_P - V_{GS}} \tag{2}$$

Where:

$$r_o = r_d \Big|_{V_{GS} = 0}$$

$$r_d = r_o \frac{V_P}{V_C} \tag{3}$$

Where:

$$V_C = V_P - V_{GS}$$

The gain function is thus seen to be linear with V_C.

$$A_V = 1 + \frac{R1}{r_o} \frac{V_C}{V_P} \tag{4}$$

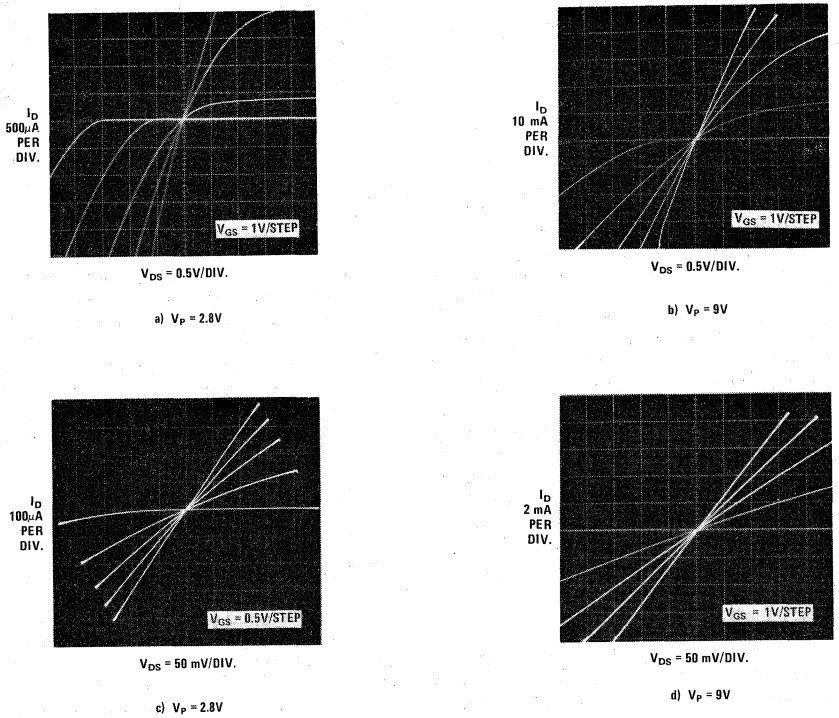


FIGURE 2. AC Output Characteristics of FET

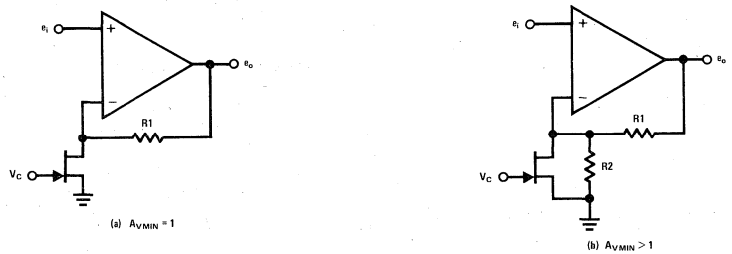


FIGURE 3. FET/Op Amp Gain Control Circuit

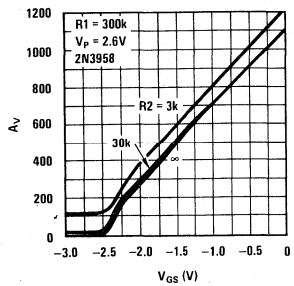


FIGURE 4. Gain vs Control Voltage For Short Channel FET

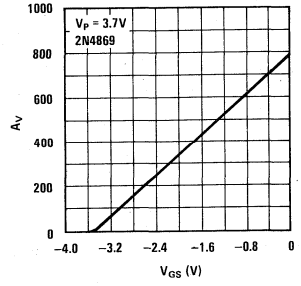


FIGURE 5. Gain vs Control Voltage For Long Channel FET

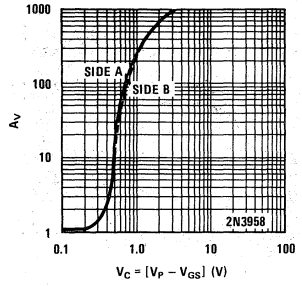


FIGURE 6. Control-Gain Match For Dual FET

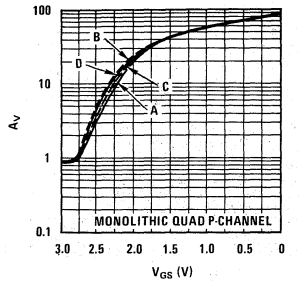


FIGURE 7. Monolithic Quad Gain Control Tracking

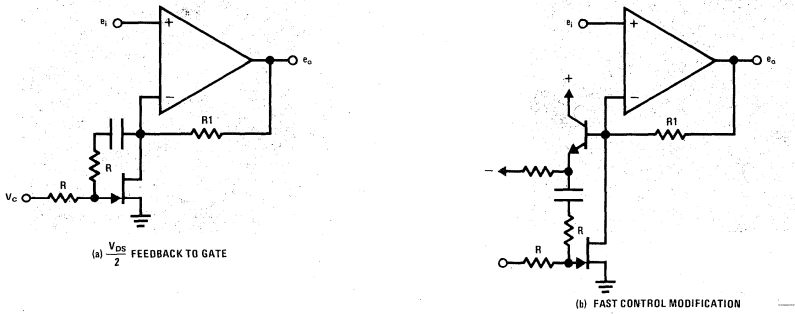


FIGURE 8. Circuit to Reduce Distortion

At $V_C = 0$, the gain reduces to unity; and at $V_C = V_P$, the gain increases to $1 + R1/r_o$ which may be as high as 1000 or so. If it is desired to limit the minimum gain to some value greater than unity, another resistor R2 may be added as in *Figure 3b.* Then the gain equation becomes:

$$A_V = 1 + \frac{R1}{\dfrac{R2\, r_o\, (V_P/V_C)}{R2 + r_o\, (V_P/V_C)}}$$

$$= 1 + \frac{R1\,[R2 + r_o\, (V_P/V_C)]}{R2\, r_o (V_P/V_C)}$$

$$A_V = 1 + \frac{R1}{R2} + \frac{R1\, V_C}{r_o\, V_P} \qquad (5)$$

In either case, the gain function is linear with V_C.

The circuits of *Figure 3* do indeed show a linear gain versus control voltage as plotted in *Figure 4* for several values of minimum gain. There is some non-linearity near minimum gain which appears in all curves. This is certainly due to a non-ideal characteristic of the FET caused by finite contact and bulk resistance at source and drain. *Figure 5* shows a similar control curve for a FET with longer channel in which the controlled channel resistance is a greater part of the total resistance than that of the short channel device of *Figure 4*. For those applications requiring a more precisely linear control of gain, the long channel devices will be preferable.

Several variable-gain circuits can be made to track when monolithic multiple FET's are used as the control elements with matched feedback resistors. A monolithic FET dual (NSC 2N3958) used in two identical control circuits shows remarkable tracking over the entire control range, even when V_{GS} is near V_P where variations would be expected to be most apparent. The plots appear in *Figure 6.* Similar performance for a quad gain control using a monolithic P-channel quad FET (AM97C09 or AM9709) is shown in *Figure 7.*

DISTORTION

Reference to *Figure 2* will show that the FET acts as a linear resistance only for relatively small values of drain-source voltage, in either polarity. This is particularly apparent for positive V_{DS} (for N-channel FET) and V_{GS} approaching V_P. The difference between *Figures 2c and 2d* indicates that the maximum allowed applied signal will be greater for high V_P as compared with low V_P.

It is possible to improve the linearity characteristics somewhat by applying a part of the V_{DS} in series with the control voltage applied as V_{GS}. The circuit to accomplish this is that shown in *Figure 8.* It happens that about half of V_{DS} applied to the gate provides the greatest improvement for small signals. The addition of two resistors and one capacitor as in *Figure 8a* is all that is required. The capacitor simply blocks the control voltage from the FET drain and the op amp input. *Figure 8b* shows the addition of an emitter follower to

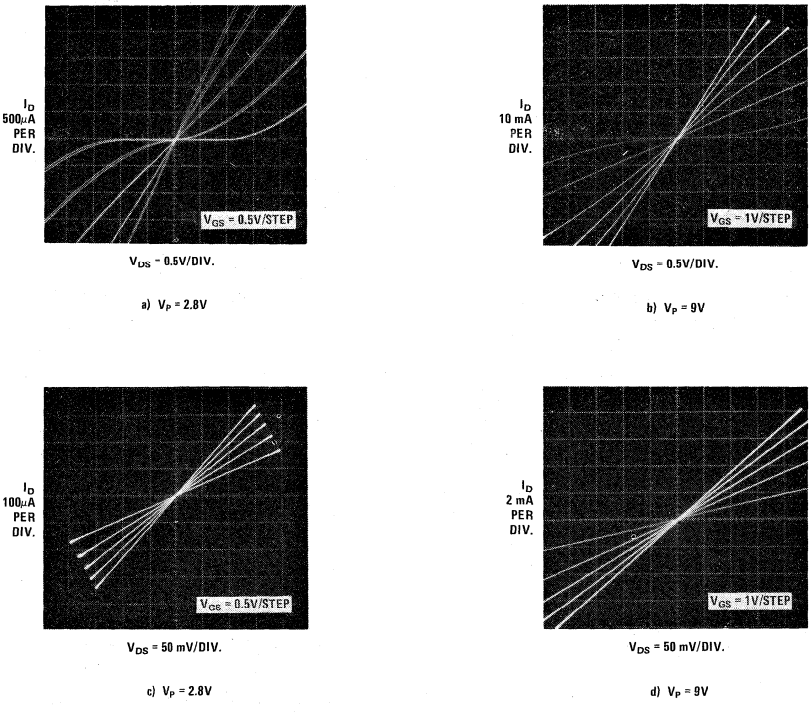


FIGURE 9. AC Output Characteristics of FET with Feedback Linearization

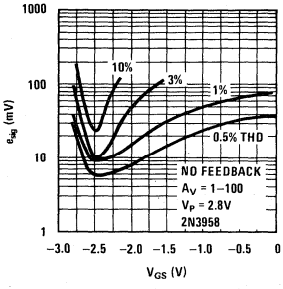


FIGURE 10. Distortion With V_P = 2.8V

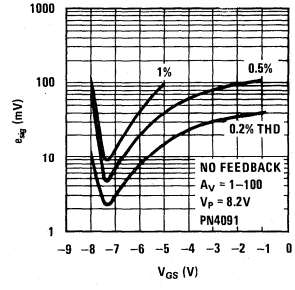


FIGURE 11. Distortion With V_P = 8.2V

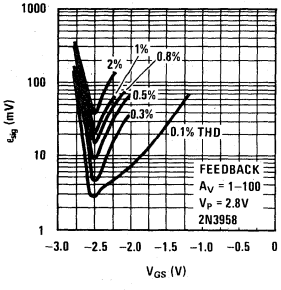


FIGURE 12. Distortion With V_P = 2.8V, With Linearization

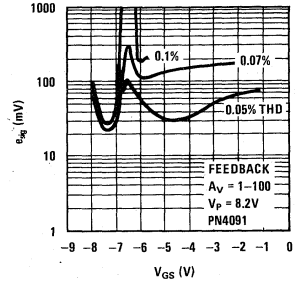


FIGURE 13. Distortion With V_P = 8.2V, Linearized

prevent abrupt changes in V_C from coupling to the op amp. *Figure 9* shows the improved linearity of the drain characteristics as compared to *Figure 2.* The improvement is also seen in the distortion versus input signal plots of *Figures 10–13.* Note particularly that the distortion at any value of V_C is primarily a function of input signal (which equals the feedback signal applied to the FET drain at the inverting input). Some modification is made to this direct relationship if an R2 is shunted across the FET as in *Figure 3b.* Measured distortion at low signal level is the result of noise rather than of signal distortion. Maximum gain is limited to about 100 in these plots so as to avoid the region of lower S/N. The noise is that of the op amp input stage and the signal source resistance plus the contribution of the FET which is essentially the thermal noise of r_d.

BANDWIDTH AND CONTROL TIME CONSTANT

The circuit bandwidth is the closed loop bandwidth of the op amp used at the (instantaneous) set gain. The gain control time constant is that of the input circuit to the FET (dependent on the value of R in *Figure 8*) limited by the slew rate of the op amp. The FET itself reacts practically instantly, producing a step change in feedback ratio. Control time constant is thus a few microseconds at most.

APPLICATIONS

Three obvious applications present themselves; they are:

1. Remote or multichannel gain control

2. Volume expansion

3. Volume compression/limiting

To this short list might be added a number of others, including applications in noise reduction and quad sound techniques.

The gain-controlled amplifier of *Figure 14* has a gain range of 1–1000, a maximum output level of 8.5 Vrms, and a bandwidth of better than 20 kHz at maximum gain. The FET used has high V_P for maximum freedom from distortion. *Figures 15 and 16* show the gain function and constant distortion contour lines. Note that the gain control curve is non-linear near unity gain because the PN4091 is a short channel FET. Distortion is quite low except as limited by maximum output voltage. Note that the maximum e_{in} is restricted by output saturation. The LM318 is used in the example only to achieve wideband response at maximum gain. The amplifier input voltage must be restricted to about 8 mVrms at maximum gain when the S/N will be about 60 dB over a 10 kHz bandwidth.

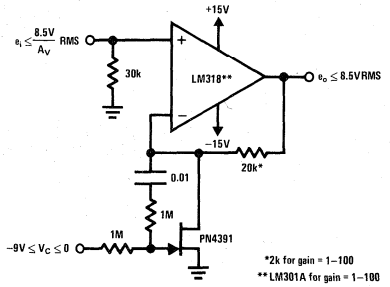


FIGURE 14. Amplifier With Gain Range = 1–1000

A more practical circuit might employ a gain range of 1–100. Then the amplifier could be a LM301A and still achieve a 10 kHz bandpass at maximum gain. The input signal could, accordingly, be increased to 80 mVrms for a S/N of 80 dB. This performance can be extended to dual and quad control circuits with tracking gain functions, but watch the bandwidth as required at maximum gain. Any of the several dual op amps could be used with the 2N3958 (monolithic dual from NSC), or the LM324 quad op amp can be used in limited gain times bandwidth applications with a quad monolithic FET. *Figure 17* shows all details of an ac coupled tracking quad gain control with 40 dB range. Gain varies over 1–100 range, bandwidth is 10 kHz minimum, S/N is better than 70 dB with 4.3 Vrms maximum output. *Figure 7* shows the gain curve and matching characteristics.

Noise considerations could be important in this method of gain control, as the signal is amplified rather than attenuated. To realize the function of a 40 dB variable attenuator, it is necessary to install a fixed attenuator at the amplifier input and perhaps also at the output. This will reduce the minimum signal level to millivolts, thus a low noise amplifier is desirable. The LM381 dual low-noise ac coupled amplifier could be used in a 40 dB

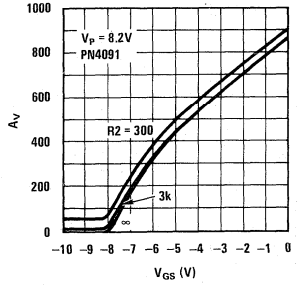


FIGURE 15. Gain For Circuit of Figure 14

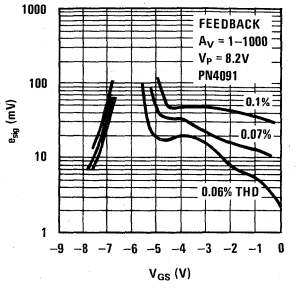


FIGURE 16. Distortion For Circuit of Figure 14

A Linear Multiple Gain Controlled Amplifier

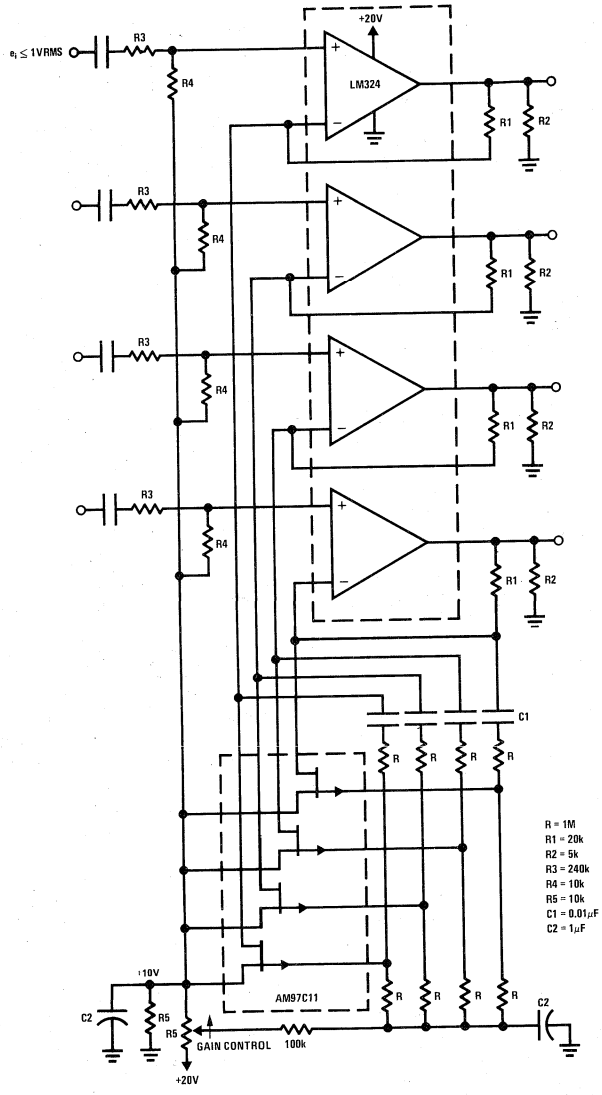


FIGURE 17. Quad Gain Control

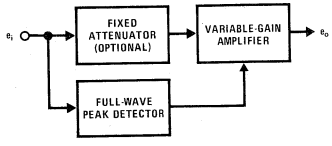


FIGURE 18. Volume Expander/Compressor Block Diagram

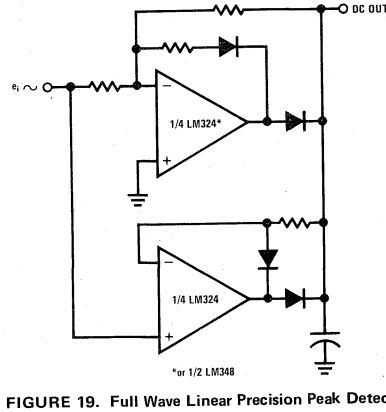


FIGURE 19. Full Wave Linear Precision Peak Detector

audio attenuator to realize S/N about 100 dB or in a 60 dB attenuator to realize 80 dB S/N. Improvements in S/N can be made by reducing system bandwidth in fixed or low frequency operation. Minimum noise is also achieved by using the minimum practical amplifier source resistance. Values as low as 1 kΩ are advantageous.

The effect of temperature will be to change the gain according to the temperature sensitivity of the FET. This effect can be reduced by using a silicon resistor for the feedback resistor, R1. If the FET were to be integrated onto the op amp chip, an attempt should be made to include R1 on the chip as well.

The application to a volume expander circuit is of interest as the control is linear, the required control range is only about 1:4, and the input signal is small for the low gain condition when distortion would otherwise be most apparent. The elements of a volume expander are indicated in *Figure 18.* The gain controlled amplifier need only exhibit a 12 dB variation in gain, being lowest for small signals. The slope of gain versus control should be linear, more specifically the slope of (log) gain in dB versus (log) signal in dB should be linear. A practical range is 12 dB gain change over a 30 dB input signal range. The peak detector should be linear down to very small signals, exhibit a fast attack or charge time of a millisecond or less, a discharge time constant of about 2 seconds, and operate on the first half cycle (full-wave detector). The detector should, therefore, be a full-wave precision linear peak detector with low internal impedance; the requirements can be met with the circuit of *Figure 19.*

The expander circuit shown in *Figure 20* will perform as desired. The gain control function is plotted in *Figure 21;* distortion is below 0.1% at all levels. Resistors R3 and R4 are added in order to modify the linear control curve to the desired log curve. Note that the input signal is attenuated prior to amplification in order to reduce distortion and maintain an overall gain of approximately 0 dB at midrange of expansion. The noise with the LM124 over a 20 kHz bandwidth is, of course, a function of signal; but the maximum signal to noise ratio is 80 dB. The circuit could be adapted to stereo or quad sound as in *Figures 22–23.* Questions for individual design concern the method of control. Whether to expand all channels together, and whether to derive the control signals individually from each channel, a summation from 2 to 4 channels, or from a single channel (assuming that high level from any channel indicates high levels from all channels). Note that the FET is biased OFF (minimum gain) for low signals, and increasing signals progressively bias the FET ON (maximum gain).

The volume compression circuit is a logical mate to the expander. The only difference would be that the FET is initially biased ON (maximum gain) for low signals, and

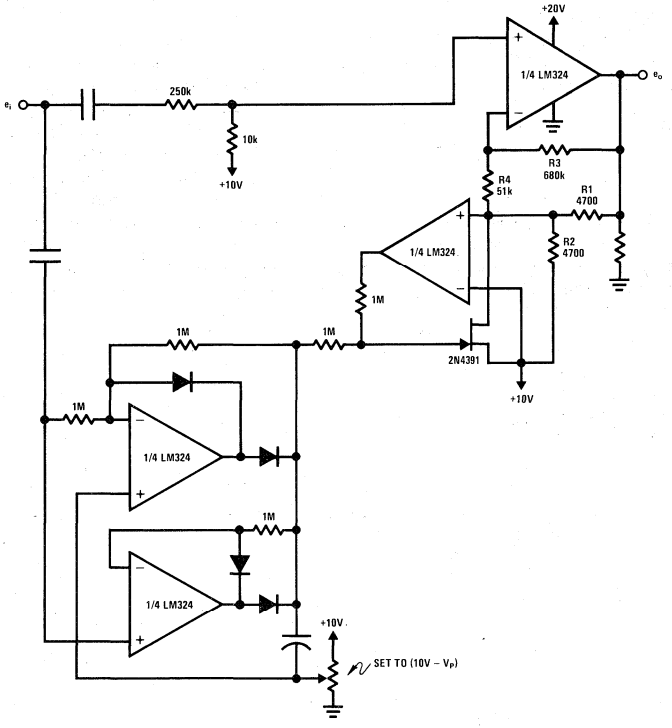


FIGURE 20. Volume Expander Circuit

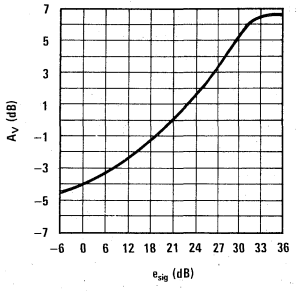


FIGURE 21. Expander Gain Characteristic

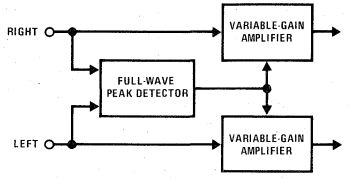
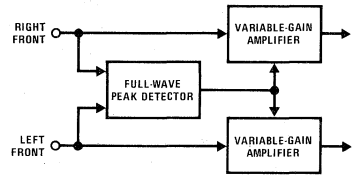


FIGURE 22. Stereo Expander Block



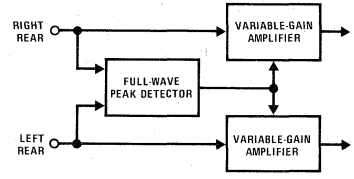


FIGURE 23. Four-Channel Expander Block

increasing signals progressively bias the FET OFF (minimum gain). A disadvantage is that the circuit produces greatest distortion in the low gain condition when signals are highest. Maximum S/N is degraded by 24 dB over that of the expander, minimum S/N is the same.

CONCLUSION

The combination of FET and op amp provides a linear dc (voltage) control of gain over a range to 60 dB. As the circuit realizes positive gain, rather than being a controlled attenuator, the input signal is limited. Input signal is further limited to several hundred millivolts by the non-linearity of the FET (which sees the full input signal). Because input signals will generally be in the 10—300 mV range, noise performance of the selected op amp will be important. Even so, S/N of 60—100 dB is obtainable with standard amplifiers. Tracking pair or quad gain-control amplifiers are realizable with existing monolithic dual or quad FET's, and the combination of FET and op amp lends itself to simple integration. The circuit is well-suited to remote and multiple linear gain control and to volume expander/compressors. The volume expander is especially interesting as the signal level and gain conditions result in extremely low distortion and more than adequate signal-to-noise ratio.

Binary/BCD Gain Programmed Amplifiers

National Semiconductor
John Maxwell
February 1977

Many systems require logic controlled gain programmable amplifiers (GPA) for signal preconditioning, level control and dynamic range expansion. The system sets GPA requirements for accuracy, speed and signal handling capability, limiting the type used. Conventional CMOS analog switches limit signal handling to ±7.5V and accuracy to 1%. High voltage CMOS or JFET analog switches increase both accuracy and signal handling (±10V to ±15V) but at a greater cost. Programmable amplifiers using current mode analog switches have the highest signal handling capability (±25V) with high accuracy, speed and low cost.

In reality, the logic controlled GPA is a multiplying digital-to-analog converter (multiplying D/A). The D/A input is the reference node which is multiplied by the digital input. Multiplying D/A converters have been available for some time in module, hybrid and monolithic form but suffer from high cost and poor signal handling capability (±10V maximum).

Large signal handling (±25V), moderate cost multiplying D/A converters can be built using monolithic current mode analog switches, an op amp and a few resistors.

Unlike conventional analog switches, only signal current is switched at the virtual ground of an op amp with current mode analog switches. Limiting the voltage across the switch to a few hundred millivolts, power supplies, logic interface and level translator circuits are eliminated allowing the JFET switches to be driven directly by standard logic.

A logic "0" turns the switch ON with a logic "1" shutting the switch OFF by pinching the FET OFF. The diode is used to clamp the source to drain voltage to about 0.7V in the switch OFF state. The series FET in the feedback path is used to compensate for the ON resistance of the switch FET.

Current through the switch is determined by the input resistor, R1, the switch ON resistance and the input voltage, V_{IN}. Scaling of the output voltage is accomplished with the feedback resistor, setting the gain of the amplifier.

$$A_V = -\frac{R2 + R_{ON2}}{R1 + R_{ON1}} \qquad (1)$$

A 4-bit multiplying D/A converter can be built using a quad current mode switch, 4 binary weighted resistors (R, 2R, 4R, 8R) and an op amp. The output voltage will be a function of the feedback resistor, input resistors and the logic state of the FET gates, G_N.

The number of bits is expanded by cascading another quad current switch and resistor array to the first. Instead of continuing the binary progression of the input resistors, (16R, 32R, etc), current splitting resistors are used such that the same resistor array (R, 2R, 4R, 8R) is used for the additional bits, minimizing the number of resistor values required for higher order converters.

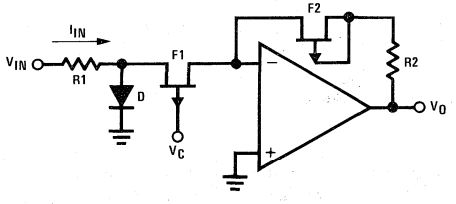
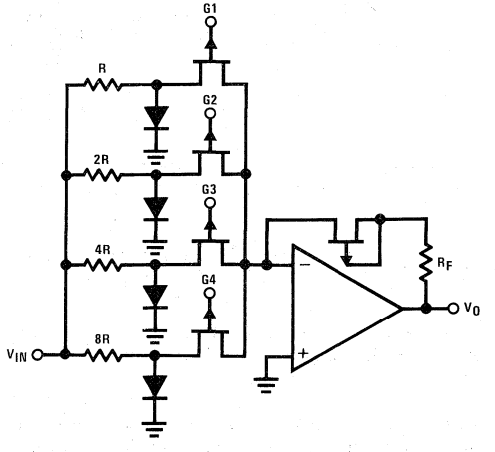
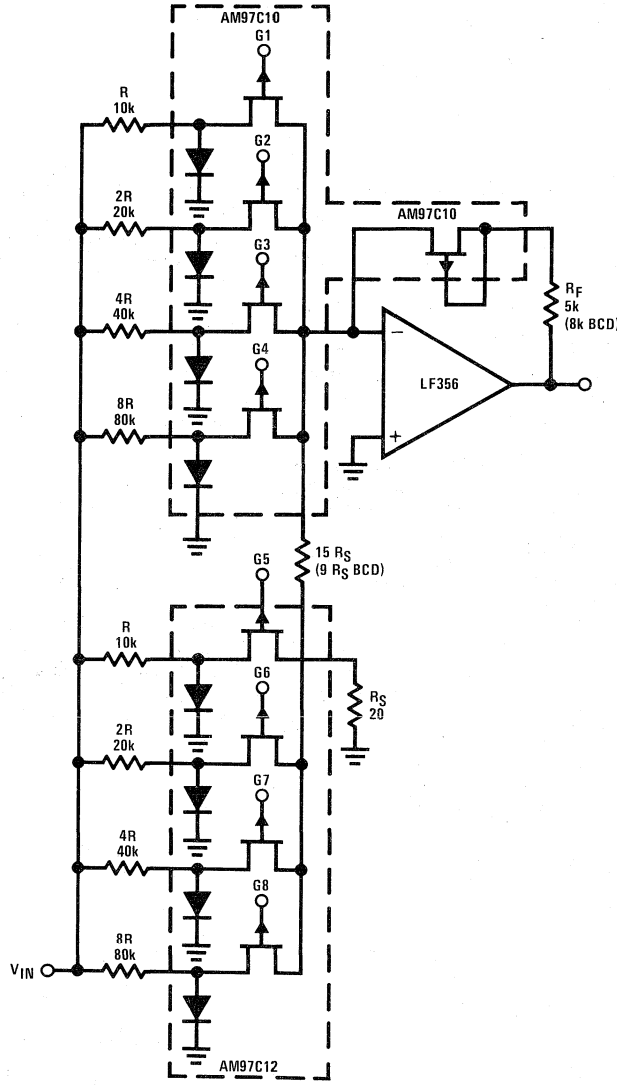


FIGURE 1. Current Mode Analog Switch



$$V_O = -V_{IN}\frac{R_F}{R}(\bar{G}1\,2^0 + \bar{G}2\,2^{-1} + \bar{G}3\,2^{-2} + \bar{G}4\,2^{-3})$$

FIGURE 2. 4-Bit Multiplying D/A Converter



$$V_O = -V_{IN}\frac{R_F}{R}\left[\bar{G}1\,2^0 + \bar{G}2\,2^{-1} + \bar{G}3\,2^{-2} + \bar{G}4\,2^{-3} + 1/16\,(\bar{G}5\,2^0 + \bar{G}6\,2^{-1} + \bar{G}7\,2^{-2} + \bar{G}8\,2^{-3})\right]$$
(1/10 for BCD)

FIGURE 3. 8-Bit Multiplying D/A Using Cascaded 4-Bit Sections

Binary weighting requires a 1/16 current split for the second switch quad while BCD weighting requires a 1/10 split.

There are 2 basic switch configurations available that are optimized for a variety of logic drives: TTL or CMOS Multiple independent switches (4 by SPST) and a 4-channel multiplex version with a series compensation FET.

Practical limitations in using monolithic current mode analog switches need consideration. Resistor values and tolerance impacted by switch resistance is minimized by increasing resistor values without regard, but limits bandwidth and creates leakage errors at elevated temperatures. Using resistors that are too small, increase switch resistance errors. Current saturation (increased switch resistance) occurs when the switch current approaches the FET saturation current, I_{DSS}. High currents also

cause $I_{G(ON)}$, current lost through the gate, as the diode and FET source to gate diode become forward biased. An input resistor value of 10k limits the switch current to less than 2 mA minimizing both leakage and switch resistance problems. For example, the gain accuracy at unity gain using the compensation FET is less than 0.05% with $R = R_F = 10k$.

The current shunt resistor used in cascading switches should be kept small to minimize the voltage drop, keeping the FET drains near ground. Values of R_S should be less than 100Ω (20 typ).

Resistor tolerance will be determined by converter resolution, i.e., the number if bits (N). For example, an 8-bit binary D/A converter will have 2^N-1 or 255 steps (99 for BCD) or different gains. The resolution or smallest step is (least significant bit) $1/2^N$ of the full-scale value (0.0039). Typical accuracy specifications for D/A converters are stated as 1 LSB or ±1/2 LSB. This works out to be ±0.2% for the 8-bit binary unit. Errors in the feedback resistor directly affect the output of the converter. The most significant resistor, R, contributes 1/2 full-scale, reducing its error contribution by a factor of 2. The same is true for the rest of the resistors with contributions of 1/4, 1/8, etc. Using a resistor tolerance of 0.1% for the feedback resistor, 0.2% for the 2 most significant resistors (R, 2R), 0.5% for the 3rd and 1% for the 4th and 5th switches allows 5% resistors to be used in the 6th, 7th and 8th switch positions.

Using the above information, 4-bit or more binary/BCD gain programmable amplifiers can be built with large signal handling capability, few parts and easily adjustable gain or attenuation. *Figure 3* shows a practical 8-bit binary/BCD GPA with gains of 0.996 (binary) with R_F = 5k and 0.99 (BCD) with R_F = 8k. For other gains, only the feedback resistor need be changed.

$$\% \text{ error} = \left[\epsilon_f^2 + \left(\frac{\epsilon_R}{2}\right)^2 + \left(\frac{\epsilon_{2R}}{2^2}\right)^2 + - - - + \left(\frac{\epsilon_{nR}}{2^n}\right)^2\right]^{1/2}$$

or (2)

$$\% \text{ error} = \left[(0.1)^2 + \left(\frac{0.2}{2}\right)^2 + \left(\frac{0.2}{4}\right)^2 + - - - + \left(\frac{5}{256}\right)^2\right]^{1/2} = \pm 0.198\%$$

ϵ_f = tolerance of feedback resistor
ϵ_R = tolerance of most significant resistor
ϵ_{nR} = tolerance of Nth resistor

FET Curve Tracer

National Semiconductor
John Maxwell
February 1977

Junction field-effect transistors (JFETs), unlike bipolar transistors, do not easily lend themselves to analytic solutions of bias networks. By their very nature, JFETs are voltage controlled devices. Gate to source voltage (control voltage V_{GS}) variations of several volts can exist within a given part type at the same operating conditions, causing the problem. Multiple suppliers and inadequate or non-existent data sheet curves compound the problem further, requiring data from the suppliers or the use of a curve tracer.

A simple curve tracer, used with any oscilloscope, can be built using a quad op amp and a handful of parts. The circuit displays drain current versus gate voltage for both P and N-channel JFETs at a constant drain voltage.

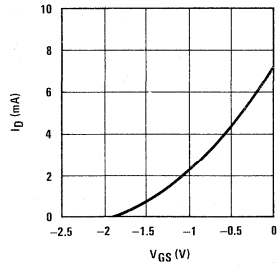


FIGURE 1. Typical N-Channel FET Transfer Curve

The circuit consists of an op amp current to voltage (I/V) amplifier with a positive or negative gate sweep

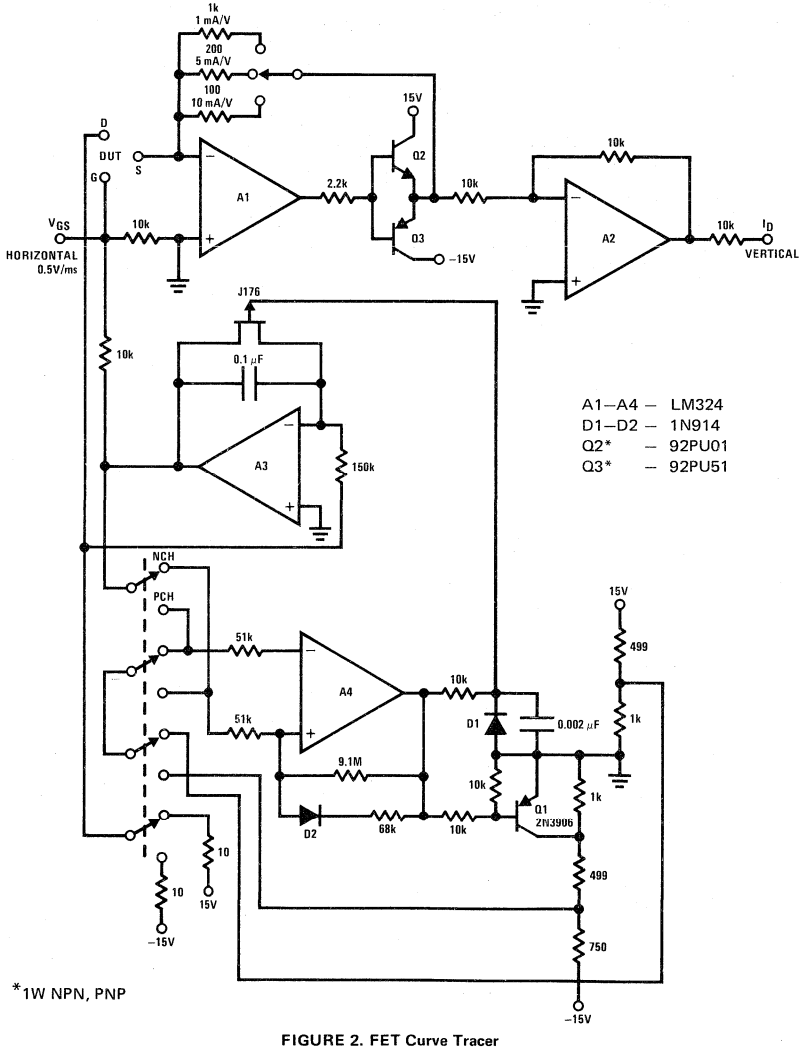


FIGURE 2. FET Curve Tracer

voltage. The I/V amplifier uses 1/4 of the quad op amp and 3 switchable feedback resistors for drain current scaling: 1k for 1 mA/V, 200Ω for 5 mA/V and 100Ω for 10 mA/V. An NPN-PNP emitter-follower buffer is used with the I/V amplifier to handle high FET currents (to 100 mA). A unity gain inverting amplifier is used for proper drain current polarity.

The gate sweep generator consists of 2 parts, a linear ramp generator with a reset and a window comparator. The ramp generator is an op amp with a capacitor in its feedback loop. The sweep rate is set by a constant current supplied to the capacitor through a resistor tied to either the plus or minus voltage supply.

The positive (P-channel) ramp mode uses the positive reference on the plus input of the comparator with the ramp connected to the minus input. The comparator output stays high (15V) pinching the FET OFF until the input exceeds the reference (10V). At that point, the output snaps to the negative supply, turning the FET switch ON, discharging the capacitor. The reference voltage at the plus input is set near ground using the 51k input resistor, D2 and 68k feedback resistor when the comparator output is in the low state. When the capacitor is discharged, the comparator resets, restarting the ramp.

A negative sweep is more difficult to generate using the same comparator. The reference (−10V) is on the minus input with the ramp connected to the plus input. As with the positive sweep, the comparator output is high until the negative sweep exceeds the reference. The difference is that the reference cannot be set to ground for the reset sweep but to a negative voltage such that when the ramp is at 0V the comparator resets. The function of Q2 is to short R1, changing the reference voltage from −10V to −6V.

In both cases, the sweep time is 10 ms. The resistor attenuator on the FET gate terminal divides the voltage in half, yielding a sweep rate of 0.5V/ms with a maximum gate voltage of ±5V. This should be adequate for most FETs used as amplifiers but if additional gate voltage is required, the attenuator can be switched out.

The circuit is limited to displaying only the FET transfer characteristic I_D vs V_{GS}, but this is the curve most needed by designers. It gives insight into parameter variations of bias circuits and it can be used to observe temperature effects on the FET. The oscilloscope vertical input is used for the drain current and the horizontal input is used for the gate voltage. The horizontal sweep can be used if no horizontal input is available where a sweep rate of 0.5 ms/cm corresponds to 0.5V/ms, allowing the curve tracer to be used with any oscilloscope.

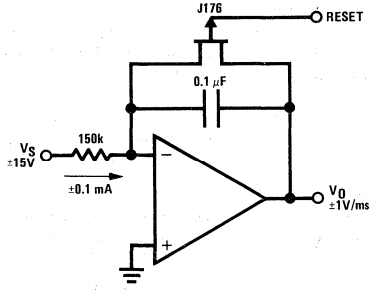


FIGURE 3. Linear Ramp Generator

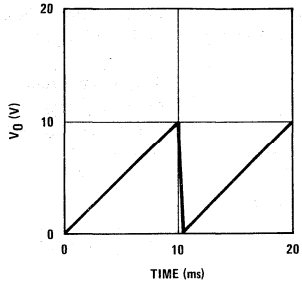


FIGURE 4. Positive Sweep

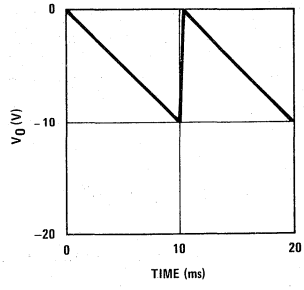
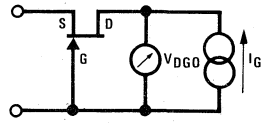
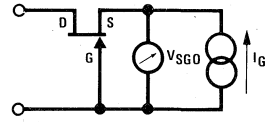
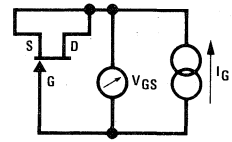
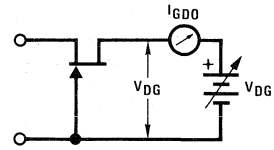
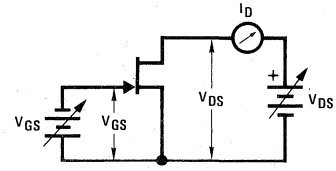
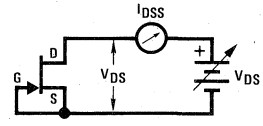
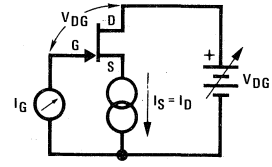
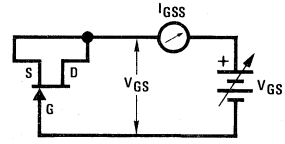
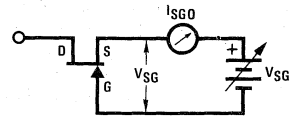
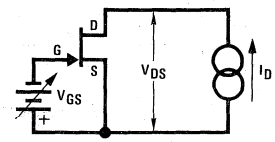
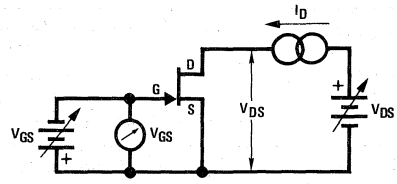
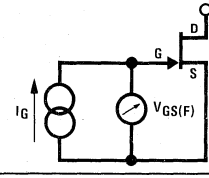
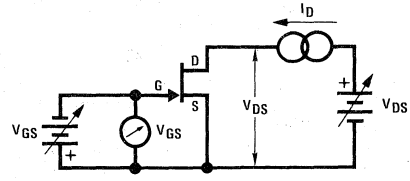
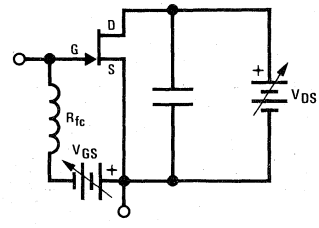
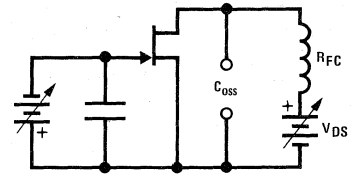


FIGURE 5. Negative Sweep

JFET Glossary of Symbols

DC PARAMETERS

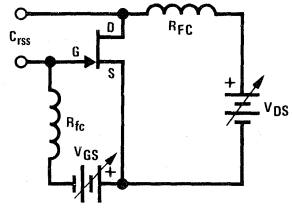
BV_{DGO} (V) or BV_{GDO}	**Drain-Gate Breakdown Voltage with Source Open-Circuited** The breakdown voltage of the drain-gate junction, measured at a specified current with the source open-circuited.	
BV_{SGO} (V) or BV_{GSO}	**Source-Gate Breakdown Voltage with Drain Open-Circuited** The breakdown voltage of the source-gate junction, measured at a specified current, with the drain open-circuited.	
BV_{GSS} (V) or BV, $V_{(BR)GSS}$	**Source-Gate Breakdown Voltage with Drain-Source Shorted** The breakdown voltage of the source-gate and drain-gate junctions, measured at a specified current with the drain-source shorted.	
I_{DGO} (pA) or I_{GDO}	**Drain-Gate Leakage Current, Source Open-Circuited** The leakage current of the drain-gate junction, measured at a specified voltage, with the source open-circuited.	
I_D (μA) or $I_{D(ON)}$	**Drain ON Current** The drain current, measured at a specified drain-source voltage and gate-source voltage.	
$I_{D(OFF)}$ (pA)	**Drain Cutoff Current** The drain cutoff current, measured at a specified drain-source voltage and gate-source voltage.	
I_{DSS} (mA)	**Drain Saturation Current** The drain current, measured at a specified drain-source voltage with the source shorted to the gate (V_{GS} = 0)	
I_G (pA) or $I_{G(ON)}$	**Gate Leakage Current with Drain Current Flowing** The gate leakage current, measured at a specified drain current and drain-gate voltage.	
I_{GSS} (pA)	**Gate-Source Reverse Leakage Current with Drain-Source Shorted** The gate-source reverse leakage current measured at a specified gate-source voltage.	

I_{SGO} (pA) or I_{GSO}	**Source-Gate Reverse Leakage Current with Drain Open-Circuited** The leakage current of the source-gate junction, measured at a specified voltage, with the drain open-circuited.	
r_{DS} (Ω) or r_{ds}, R_{DS}, $r_{DS(ON)}$	**Drain-Source ON Resistance** The drain-source ON resistance, measured at a specified gate-source voltage and drain current.	 $r_{DS} = \frac{V_{DS}}{I_D}$
$V_{DS(ON)}$ (mV)	**Drain-Source ON Voltage** The drain-source ON voltage, measured at a specified gate-source voltage and drain current.	
V_{GS} (V) or $V_{GS(ON)}$, V_G	**Operating Gate-Source Voltage** The gate-source voltage, measured at a specified drain current and drain-source voltage.	
$V_{GS(F)}$ (V)	**Forward Gate-Source Voltage** The forward gate-source voltage, measured at specified current.	
$V_{GS(OFF)}$ (V) or V_P	**Gate-Source Cutoff (Pinch-Off) Voltage** The gate-source cutoff voltage, measured at a specified drain current and drain-source voltage.	
SMALL SIGNAL PARAMETERS		
C_{iss} (pF) or C_{iss}, C_{gss}	**Common-Source Input Capacitance** The common-source input capacitance measured between the gate and source with the drain A–C shorted to the source at specified drain-source and gate-source voltages.	
C_{oss} (pF) or C_{os}, C_{dss}	**Common-Source Output Capacitance** The common-source output capacitance, measured between the drain and source with the source A–C shorted to the gate at specified drain-source and gate-source voltages.	

C_{rss} (pF) or C_{rs}, C_{dg}

Common-Source Reverse Transfer Capacitance

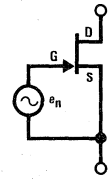
The common-source reverse transfer capacitance, measured between the drain and gate at specified drain-source and gate source voltages.



e_n (nV/$\sqrt{Hz}$) or e_n, V_n, E_n

Equivalent Input Noise Voltage

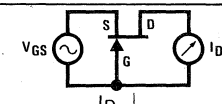
The equivalent input noise voltage per unit bandwidth, measured with the input A–C shorted to the source at a specified operating condition.



g_{fg} (mV) or y_{fg}

Common- Gate Forward Transconductance

The common-gate forward transconductance with the output A–C shorted. This is a complex quantity ($g_{fg} + jb_{fg}$).



$$Y_{fg} = \frac{I_D}{V_{GS}}\Bigg|_{V_{DS}=0}$$

g_{fs} (mV) or g_m, Y_{fs}, $Re|Y_{fs}|$

Common-Source Forward Transconductance

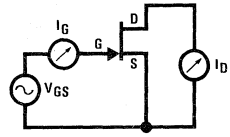
The common source forward transconductance with the output A–C shorted. This is a complex quantity ($g_{fs} + jb_{fs}$).

$$Y_{fs} = \frac{I_D}{V_{GS}}\Bigg|_{V_{DS}=0}$$

g_{iss} (μV) or Y_{is}

Common-Source Input Conductance

The common-source input conductance with the output A–C shorted. This is a complex quantity ($g_{is} + jb_{is}$).

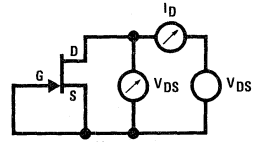


$$Y_{is} = \frac{I_G}{V_{GS}}\Bigg|_{V_{DS}=0}$$

g_{oss} (μV) or Y_{os}

Common-Source Output Conductance

The common source output conductance with the input A–C shorted. This is a complex quantity ($g_{os} + jb_{os}$).



$$Y_{os} = \frac{I_D}{V_{DS}}\Bigg|_{V_{GS}=0}$$

G_{pg} (dB)

Common-Gate Power Gain

The common-gate power gain is the ratio of output power to input power.

G_{PS} (dB)

Common-Source Power Gain

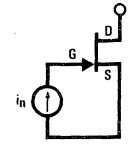
The common-source power gain is the ratio of output power to input power.

$$G_p = 10 \log_{10} \frac{P_o}{P_i}$$

i_n (pA/$\sqrt{Hz}$)

Equivalent Input Noise Current

The equivalent input noise current measured with the input open-circuited under specified operating conditions.



NF (dB)

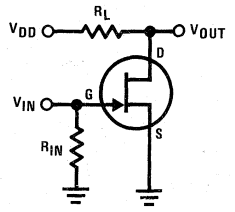
Spot Noise Figure

Noise figure = 10 $\log_{10}$ F were F is noise factor which is the ratio of the total output noise power to the output noise power of the source. Measured at specified operating conditions and source resistance.

$$F = \frac{\text{Total Output Noise Power}}{\text{Source Output Noise Power}}$$

COMMON-SOURCE SWITCHING PARAMETERS

In the following, drive circuit conditions and drain circuit conditions must be specified. The transition times of the input must be negligible compared to the measured times.



$t_{d(ON)}$ **Turn-On Delay Time**

The time interval during turn-on from the point when the input pulse at the gate reaches 10% of its full amplitude to the point when the drain pulse changes from 0 to 10% of its maximum amplitude.

t_r **Rise Time**

The time interval during turn-on in which the drain current pulse changes from 10% to 90% of its maximum amplitude.

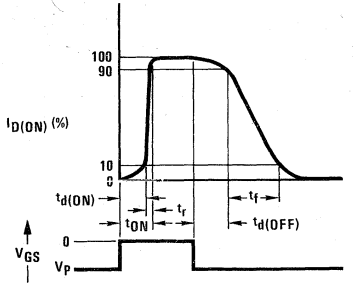
$$I_{D(ON)} = \frac{V_{DD} - V_{DS(ON)}}{R_L}$$

$t_{d(OFF)}$ **Turn-Off Delay Time**

The time interval during turn-off from the point when the turn-off pulse at the gate changes from 100% to 90% of its full amplitude to the time when the drain current has changed from 100% to 90% of its maximum amplitude.

t_f **Fall Time**

The time interval during turn-off in which the drain current pulse decreases from 90% to 10% of its maximum amplitude.

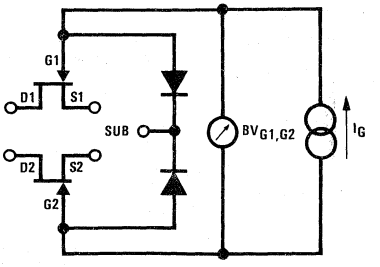


DUAL FET PARAMETERS

$BV_{G1, G2}$ (V) or BV_{G1-2}

Gate to Gate Breakdown Voltage

The breakdown voltage of the gate to gate junctions, measured at a specified current.

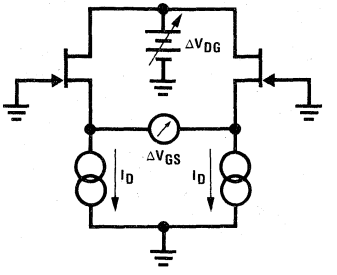


CMRR (dB) or CMR

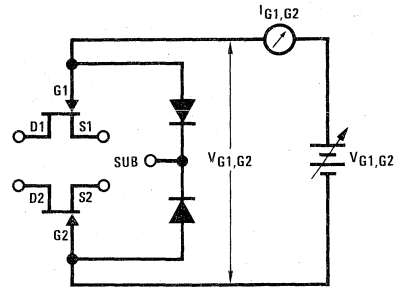
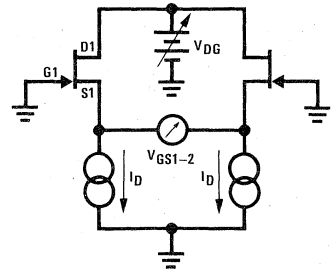
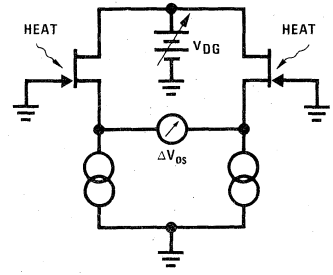
Common-Mode Rejection Ratio

The common-mode rejection ratio is the ratio of the change in differential gate voltage with a change in the drain to gate voltage.

$$CMRR = 20 \log_{10} \frac{\Delta V_{DG}}{\Delta V_{os}}$$



6

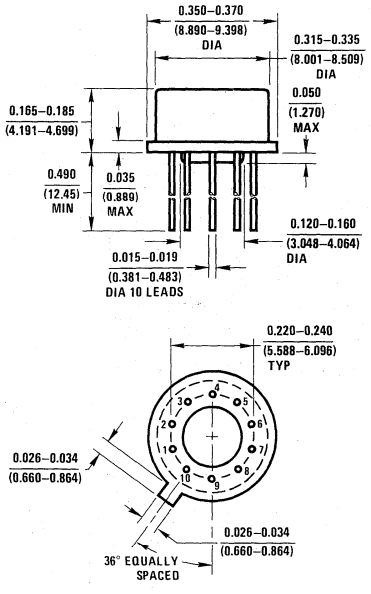
g_{fs1-2} (%) or g_{fs1}/g_{fs2}	**Common-Source Forward Transconductance Ratio (Match)** The transconductance ratio = g_{fs1}/g_{fs2} x 100 (%) measured at specified drain-gate voltage and drain current.	
g_{oss} 1-2 (μV) or g_{os1-2}	**Common-Source Output Conductance (Match)** Output conductance match = $\lvert g_{os1}-g_{os2}\rvert$ measured at specified drain-gate voltage and drain current.	
I_{DSS1-2} (%) or I_{DS1-2}, I_{DSS1}/I_{DSS2}	**Drain Saturation Current Ratio (Match)** The drain saturation current ratio = I_{DSS1}/I_{DSS2} x 100% measured at specified drain-source voltages.	
I_{G1-2} (pA)	**Differential Gate Leakage Current** Differential gate leakage current = $\lvert I_{G1}-I_{G2}\rvert$ measured at specified drain-gate voltage and drain current.	
$I_{G1, G2}$ (pA)	**Gate to Gate Reverse Leakage Current** The gate to gate reverse leakage measured at a specified voltage monolithic dual with diode isolation shown.	
V_{GS1-2} (mV) or ΔV_{GS}, V_{os}, $\lvert V_{GS1}-V_{GS2}\rvert$	**Differential Gate-Source Voltage** The differential gate-source voltage, measured at a specified drain-gate voltage and drain current.	
ΔV_{GS1-2} (μV/°C) or $\Delta\lvert V_{GS1}-V_{GS2}\rvert/\Delta T$ $\Delta V_{os}/\Delta T$	**Differential Gate-Source Voltage Drift** The differential gate-source voltage drift is the change in the differential gate-source voltage with a change in device temperature at a specified operating condition. $\frac{\Delta V_{os}}{\Delta T} = \left\lvert \frac{(V_{GS1}-V_{GS2})\lvert T_1 - (V_{GS1}-V_{GS2})\lvert T_2}{T_1-T_2} \right\rvert$	

Section 7

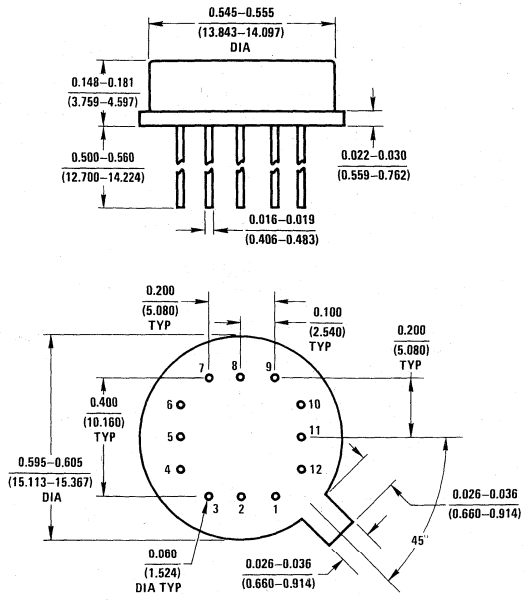
Physical Dimensions

7

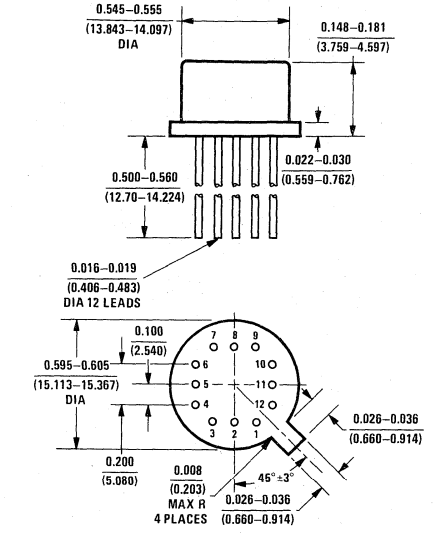
Physical Dimensions All dimensions expressed as inches (millimeters)



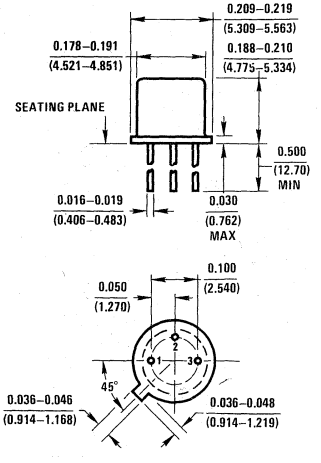
Package 1
10-Lead TO-5 Metal Can Package (H) (Low Profile)
NS Package Number H10A



Package 2
12-Lead TO-8 Metal Can Package (G)
NS Package Number H12B

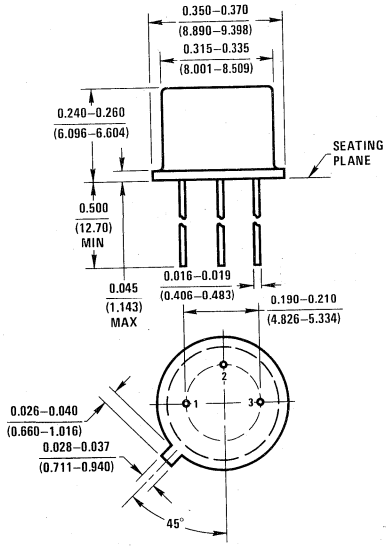


Package 3
12-Lead TO-8 Metal Can Package (G)
(AH2114/AH2114C Only)
NS Package Number H12C



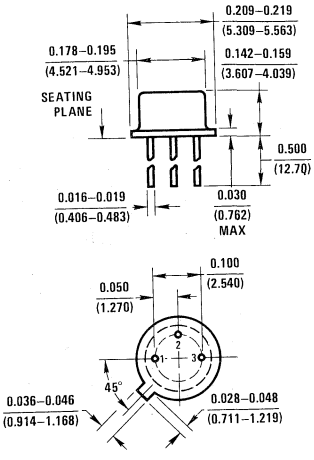
PIN	FET N(02)	FET P (11)
1	S	S
2	D	G
3	G	D

Package 4
3-Lead TO-18 (02, 11) Metal Can Package
NS Package Number H03D



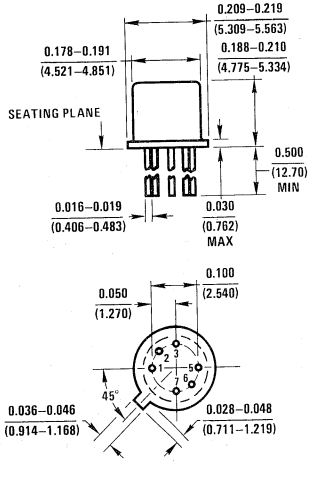
PIN	FET
1	S
2	D
3	G

Package 5
3-Lead TO-39 (09) Metal Can Package (H) (High Profile)
NS Package Number H03G



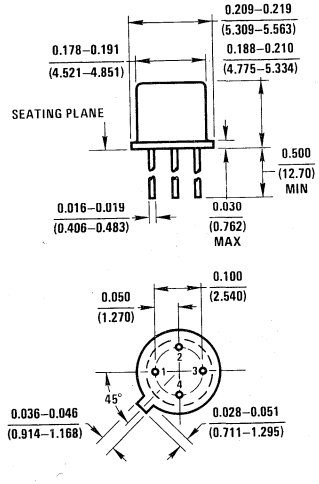
PIN	FET(07)
1	S
2	D
3	G

Package 6
3-Lead TO-52 (07) Metal Can Package
NS Package Number H03J



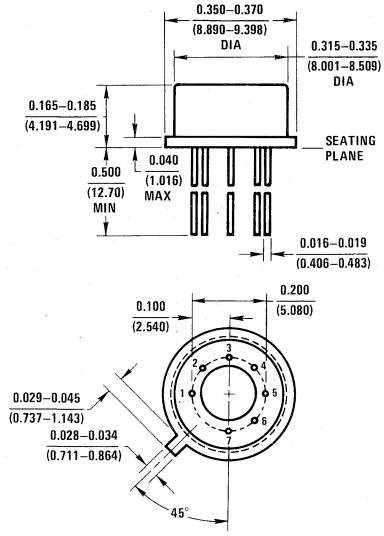
PIN	FET
1	S1
2	D1
3	G1
5	S2
6	D2
7	G2

Package 7
6-Lead TO-71 (12) Metal Can Package
NS Package Number H06A



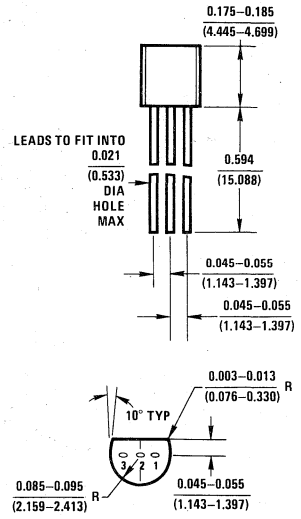
PIN	FET P(23)	FET N(25)
1	S	S
2	G	D
3	D	G

Package 8
4-Lead TO-72 (23, 25) Metal Can Package (H)
NS Package Number H04C



PIN	FET
1	S1
2	D1
3	G1
4	Case
5	S2
6	D2
7	G2

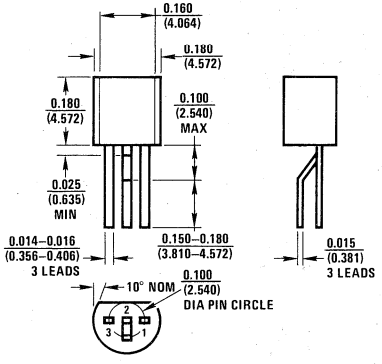
Package 9
6-Lead TO-78 (24) Metal Can Package (H)
NS Package Number H06B



PIN	71	72	74
1	G	G	S
2	D	S	G
3	S	D	D

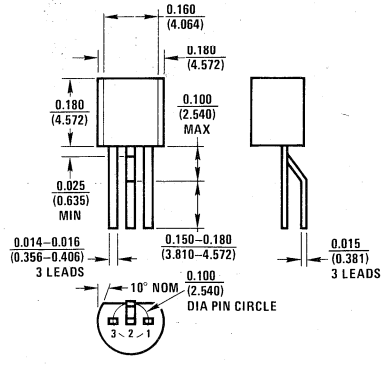
FET case 71 and 72 are interchangeable without compromise in performance except some RF application at VHF

Package 10
3-Lead TO-92 (71, 72, 74) Plastic Package
NS Package Number Z03A



PIN	FET
1	D
2	S
3	G

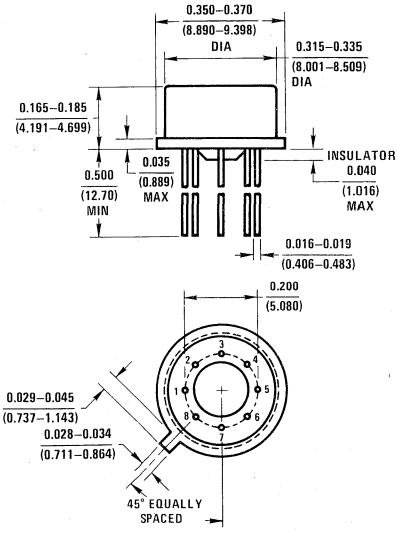
Package 11
3-Lead TO-92 (77) Plastic Package
NS Package Number Z03D



PIN	71	72	74
1	G	G	S
2	D	S	G
3	S	D	D

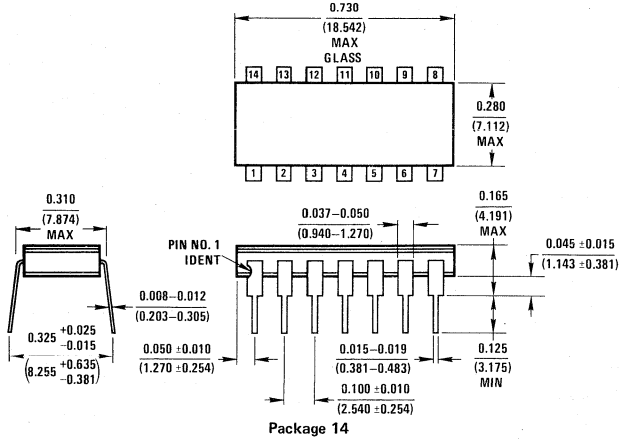
TO-18 lead form available on special order or standard on some products converted from TO-106 package.

Package 12
3-Lead TO-92 (TO-18 Lead Form) Plastic Package
NS Package Number Z03E

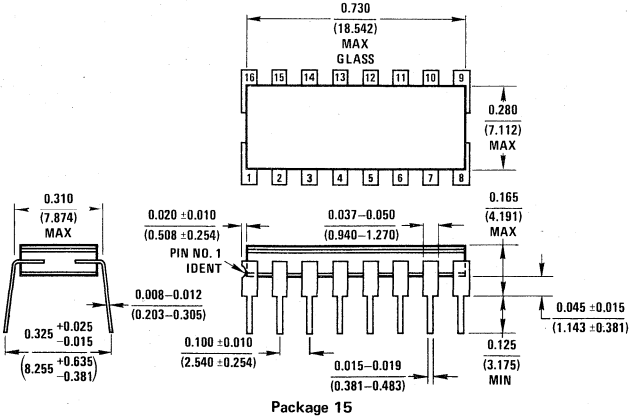


PIN	FET
1	S1
2	D1
3	G1
4	Case
5	S2
6	D2
7	G2
8	Sub

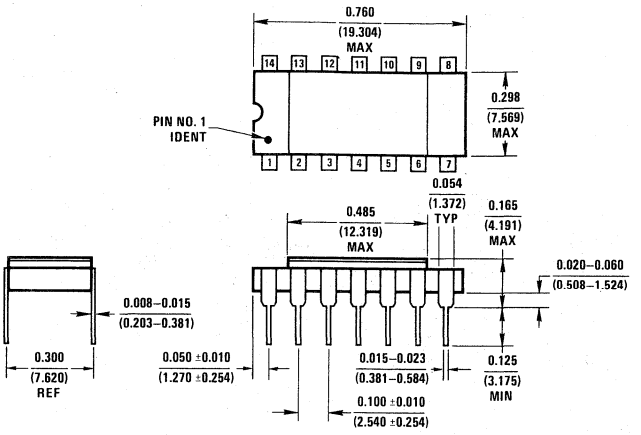
Package 13
8-Lead TO-99 (24 Alternate) Metal Can Package (H)
NS Package Number H08B



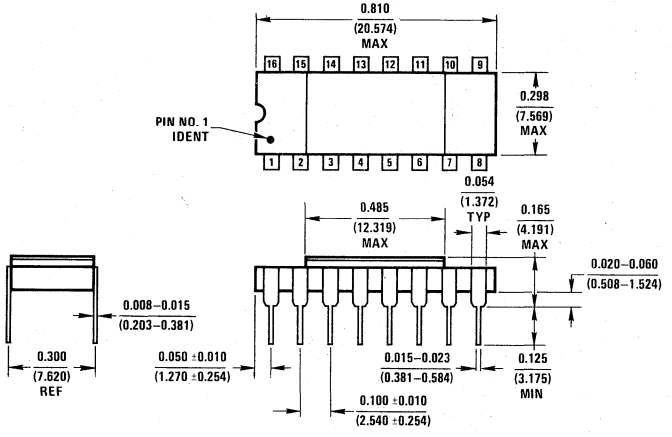
Package 14
14-Lead Cavity DIP (D)
NS Package Number D14A



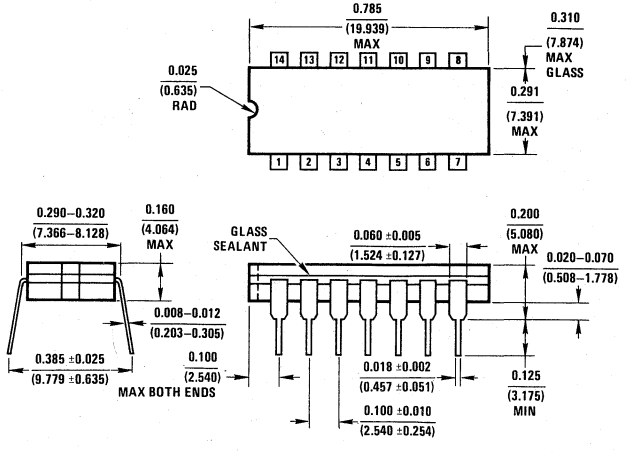
Package 15
16-Lead Cavity DIP (D)
NS Package Number D16A



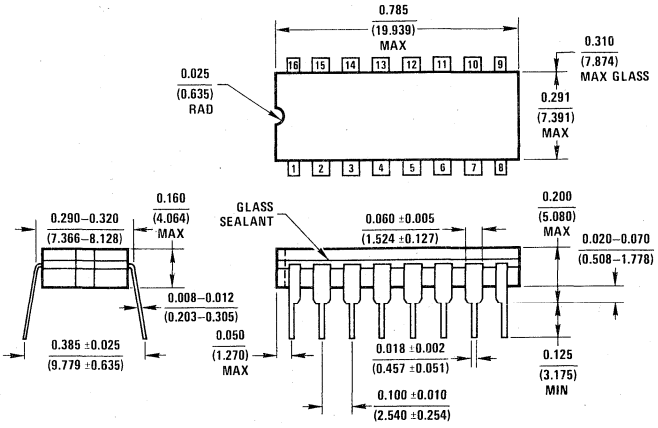
Package 16
14-Lead Side-Brazed Cavity DIP (D)
NS Package Number D14E



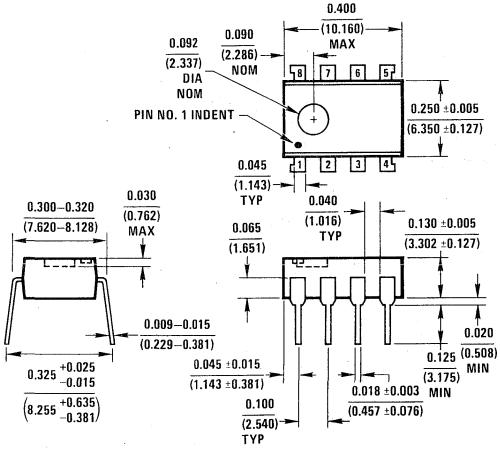
Package 17
16-Lead Side-Brazed Cavity DIP (D)
NS Package Number D16C



Package 18
14-Lead Cavity DIP (J)
NS Package Number J14A

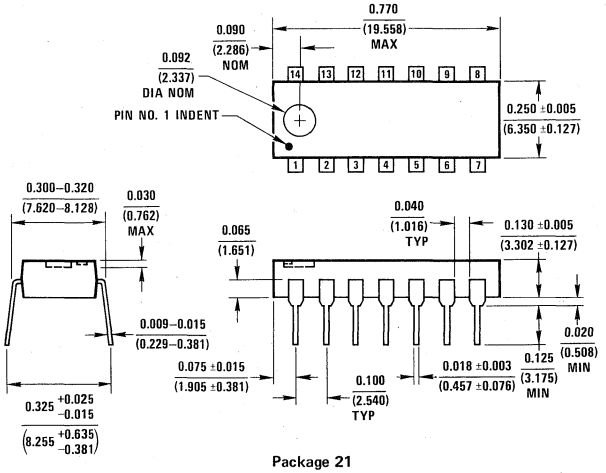


Package 19
16-Lead Cavity DIP (J)
NS Package Number J16A

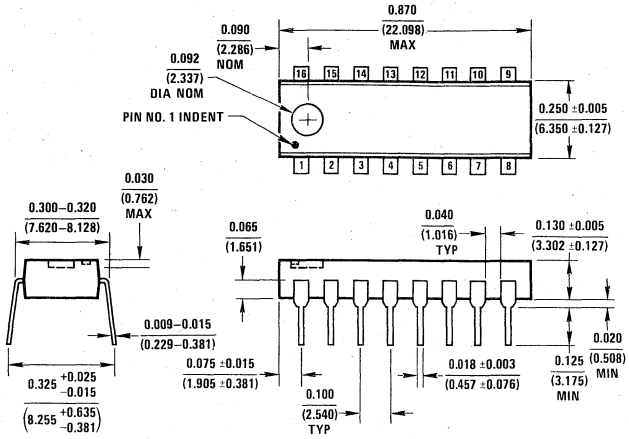


PIN	60	67
1	NC	S1
2	S1	D1
3	D1	NC
4	G1	G1
5	S2	S2
6	D2	D2
7	G2	NC
8	NC	G2

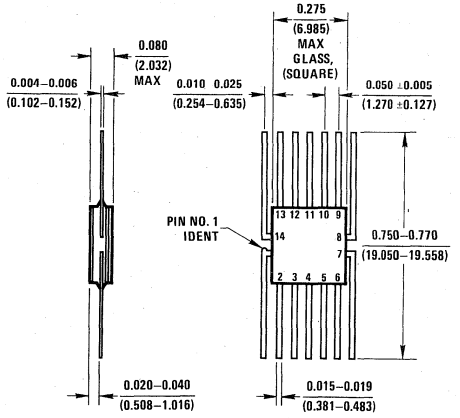
Package 20
8-Lead Molded Mini-DIP (60, 67) (N)
NS Package Number N08A



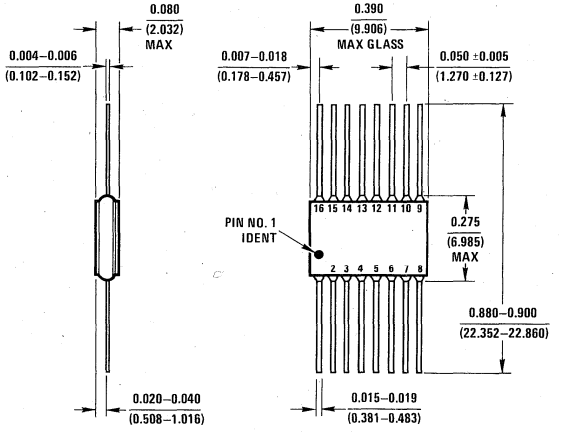
Package 21
14-Lead Molded DIP (N)
NS Package Number N14A



Package 22
16-Lead Molded DIP (N)
NS Package Number N16A



Package 23
14-Lead Flat Package (F)
NS Package Number F14A



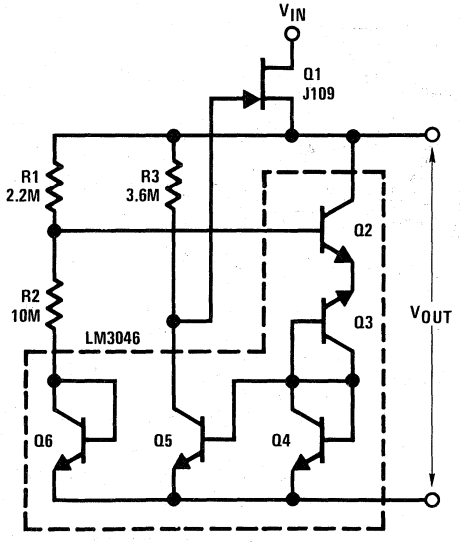
Package 24
16-Lead Flat Package (F)
NS Package Number F16A

A Novel FET Micropower Voltage Regulator

National Semiconductor
John Maxwell
February 1977

Many systems require a stable voltage supply to maintain constant performance. When these systems are battery-operated, a regulator is needed to stabilize the system voltage as the battery decays with time. Unfortunately, IC voltage regulators require several milliamps of quiescent current, making them impractical for micropower applications. Zener diodes may also be impractical because of short term peak current requirements of the system. This could require additional buffering or high standby currents, but both increase the battery drain. An inexpensive micropower voltage regulator is needed to fill the gap between IC regulators (high quiescent current) and zener diodes (high standby current).

Instead of the tranditional bipolar approach, the regulator shown in *Figure 1* uses a JFET as the series pass element. This offers several advantages: first, no pre-regulation is needed for the pass element as with an NPN because the drive comes from the regulated output. Next, the gate-source is isolated from the line via the drain, thus offering excellent line regulation. This is not the case with PNP pass elements, where the emitter is the input. Finally, and possibly the most important feature for micropower regulators, is FETs require no current drive.



Output Voltage

$$V_{OUT} = V_{BE}\left(2 + \frac{R1}{R2}\right) + BV_{EB}\left(1 + \frac{R1}{R2}\right)$$

Drift

$$\frac{\partial V_{OUT}}{\partial T} = \frac{\partial V_{BE}}{\partial T}\left(2 + \frac{R1}{R2}\right) + \frac{\partial BV_{EB}}{\partial T}\left(1 + \frac{R1}{R2}\right)$$

Quiescent Current $\simeq 4\ \mu A$

FIGURE 1. Micropower Regulator

The emitter-base breakdown voltage of Q3 is used as a reference (~7.2V) in conjunction with Q2 to form a shunt regulator. The shunt current drives a current mirror, Q4–Q5, which creates the gate drive voltage of the pass FET. The value of the shunt current is determined by R3 and the V_{GS} of the pass FET ($I_{R3} \simeq I_{SHUNT}$). High load currents will reduce the shunt current because the FET V_{GS} is lower. Temperature stability is achieved by cancelling the drift of Q2 and Q3's V_{BE} (~–2 mV/°C/transistor) with the BV_{EB} drift of Q3 (~ 3 mV/°C) resulting in a negative drift at the base of Q2, and the output, of 1 mV/°C.

Selection of the FET requires some care. Ideally, the FET I_{DSS} needs to be greater than the load current at all temperatures (I_{DSS} has a temperature coefficient of ~–0.7%/°C) and the breakdown voltage should be greater than the maximum input voltage. Practically, the FET I_{DSS} needs to be much larger than the maximum load current. Linear operation requires the FET's drain to gate voltage (V_{DG}) to be greater than the pinchoff voltage V_P. By operating the FET at currents much less than I_{DSS}, the gate to source voltage (V_{GS}) will be close to V_P ($V_{GS} = V_P\ (1-(I_D/I_{DSS})^{1/2})$) allowing small drain to source voltages (V_{DS}). For linear operation:

$$|V_{DG}| > |V_P|$$

$$V_{DG} = V_{DS} - V_{GS}$$

It should be noted that N FET's can be paralleled for higher load current requirements without matching the devices.

Actual performance of the regulator is quite good. With a 10V typical output, the line regulation is within ±0.05% for a range of V_{IN}–V_{OUT} of 0.3V to 10V. The load regulation is 0.2% with a load range of 10 μA to 10 mA ($Z_o \simeq 10\Omega$) and the temperature stability is –0.01%/°C (–1 mV/°C). The output voltage can be easily trimmed by adding a pot at the R1R2Q2$_{BASE}$ junction to eliminate BV_{EB} variations or to make the output adjustable over a limited range. Also, the temperature stability can be improved by replacing Q3 with an 8.2V zener diode, because its temperature drift (~ 4 mV/°C) would nearly match the combined V_{BE} drift of Q2 and Q4. The regulator is good enough to be used as a reference in low accuracy (6–7-bit) or limited temperature range applications if current drain is important.

REFERENCES

1. "Voltage Regulator Handbook", National Semiconductor Corporation, May 1975.
2. "Zener Diode Handbook", Motorola, Inc., May 1967.
3. Williams, P., "D.C. Voltage-Reference Circuits with Minimum Input-Output Differentials", Proc. IEEE pp. 1280–1281, December, 1969.

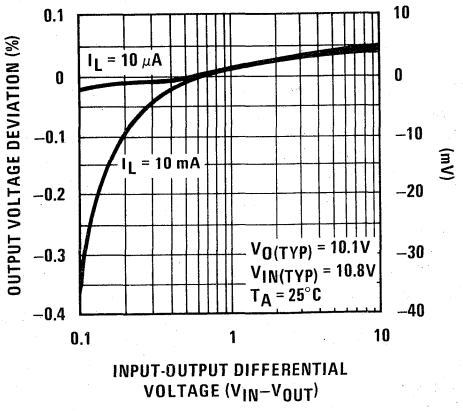


FIGURE 2. Line Regulation vs Input-Output Differential

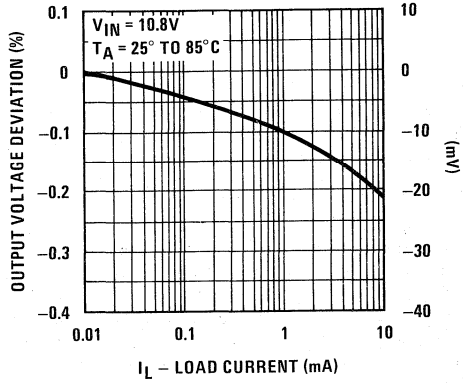


FIGURE 3. Load Regulation

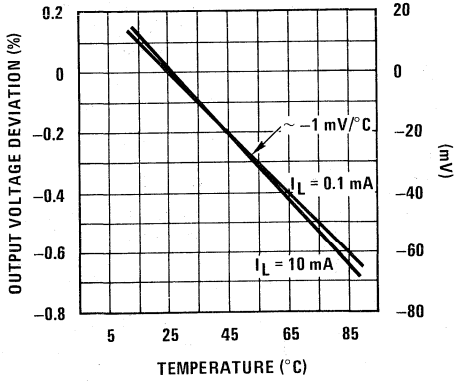


FIGURE 4. Temperature Stability

A Linear Multiple Gain Controlled Amplifier

National Semiconductor
Application Note 129
Jim Sherwin
August 1975

INTRODUCTION

A linear control function over three decades of gain can be achieved with a FET in the feedback path of a non-inverting amplifier. Besides the ultimate simplicity of the circuit, multiple tracking gain control circuits can be constructed with dual op amps and monolithic dual FET's or quad op amps and monolithic quad FET's. Such circuits could even be integrated with ion-implanted FET's on single or multiple monolithic op amp chips. The gain control range may be designed for less than 2 to 1 or higher than 1000:1, but input voltage levels are limited by acceptable levels of distortion. Bandwidth is dependent on maximum gain and unity gain bandwidth of the op amp used. The gain control circuit is especially suitable for volume expansion applications.

GAIN CONTROL WITH FETS

The FET has long been used as a voltage controlled resistor (VCR), often as the shunt arm in the series-shunt attenuator of *Figure 1.* Advantages of the FET as a VCR are that:

1. The control signal is almost perfectly isolated from the controlled signal path, and
2. The resistance can be made to vary over an almost infinite max/min ratio.

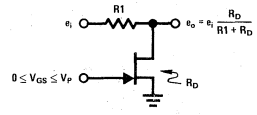


FIGURE 1. Voltage Controlled FET Attenuator

Disadvantages are that:

1. The FET behaves as a linear resistance only for small values of source-drain voltage V_{DS},
2. Non-linearity (of resistance) increases as the control voltage V_{GS} approaches cut-off voltage V_P when the resistance is maximum,
3. The relationship of resistance r_d to V_{GS} is reciprocal rather than direct linear,
4. VCR multiples with matched resistance characteristics over their full control range have been extremely difficult to obtain at any kind of reasonable price, and
5. Production spread in V_P requires separate bias set and gain set on each circuit.

Examination of the FET drain characteristics in *Figure 2* will reveal the essential non-linearity of r_d at high signal levels, especially as V_{GS} approaches V_P. This non-linear region must be avoided in order to achieve tolerable distortion levels. One obvious way is to limit V_{DS} to small values when r_d is high as suggested by *Figures 2c and 2d,* another is to utilize FET's with high V_P as suggested by reference to *Figures 2b and 2d.*

The reciprocal relationship of r_d and V_{GS} is an advantage, as it is precisely that which allows the linear control of gain in the circuit to be described. The availability of matched monolithic dual FET's such as the NSC 2N3958 (watch out for the matched pairs as their resistance match close to V_P may not be as good as that of the monolithic versions) make available low cost duals with very closely matched resistance characteristics over the full control range. There are even some monolithic quads available (such as the AM9709 series). The final problem of the production range of V_P can be much improved with ion-implant diffusion techniques whereby lot variation in V_P may be held to within a few tenths of one volt.

The gain control circuit is that of an ordinary non-inverting op amp with feedback. The usual circuit is modified in *Figure 3a* to include a FET as controlled resistor. The gain function is normal except that r_d replaces R2 in the usual form.

$$A_V = 1 + \frac{R1}{r_d} \tag{1}$$

Now r_d can be equated to a control voltage V_C as follows:

$$r_d = r_o \frac{V_P}{V_P - V_{GS}} \tag{2}$$

Where:

$$r_o = r_d \Big|_{V_{GS} = 0}$$

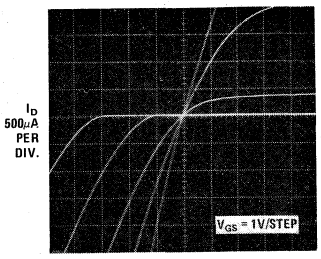
$$r_d = r_o \frac{V_P}{V_C} \tag{3}$$

Where:

$$V_C = V_P - V_{GS}$$

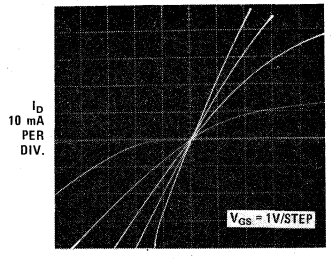
The gain function is thus seen to be linear with V_C.

$$A_V = 1 + \frac{R1}{r_o} \frac{V_C}{V_P} \tag{4}$$



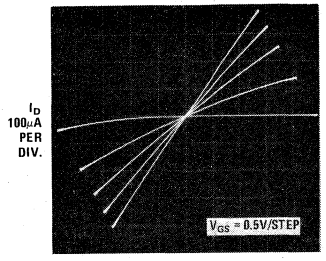
V_{DS} = 0.5V/DIV.

a) V_P = 2.8V



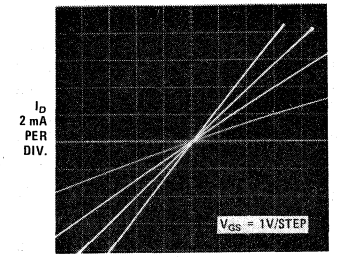
V_{DS} = 0.5V/DIV.

b) V_P = 9V



V_{DS} = 50 mV/DIV.

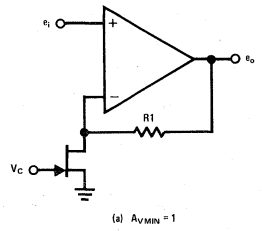
c) V_P = 2.8V



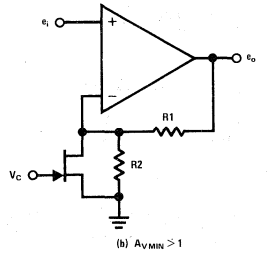
V_{DS} = 50 mV/DIV.

d) V_P = 9V

FIGURE 2. AC Output Characteristics of FET



(a) $A_{V_{MIN}} = 1$



(b) $A_{V_{MIN}} > 1$

FIGURE 3. FET/Op Amp Gain Control Circuit

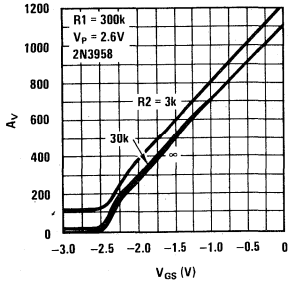


FIGURE 4. Gain vs Control Voltage For Short Channel FET

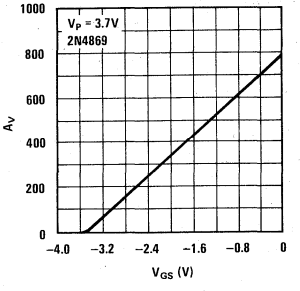


FIGURE 5. Gain vs Control Voltage For Long Channel FET

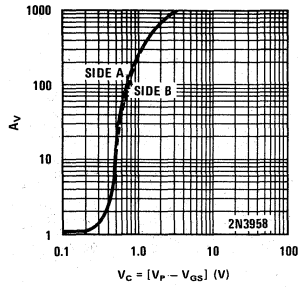


FIGURE 6. Control-Gain Match For Dual FET

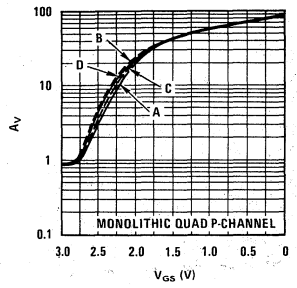
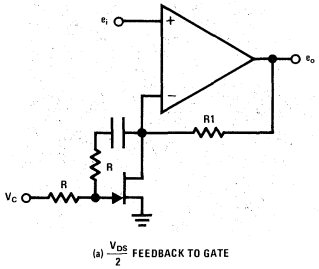


FIGURE 7. Monolithic Quad Gain Control Tracking



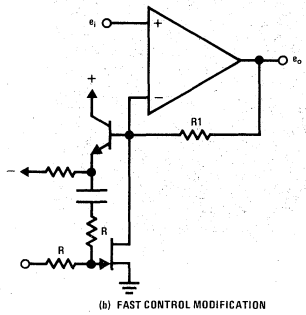


FIGURE 8. Circuit to Reduce Distortion

At $V_C = 0$, the gain reduces to unity; and at $V_C = V_P$, the gain increases to $1 + R1/r_o$ which may be as high as 1000 or so. If it is desired to limit the minimum gain to some value greater than unity, another resistor R2 may be added as in *Figure 3b.* Then the gain equation becomes:

$$A_V = 1 + \frac{R1}{\frac{R2\, r_o\, (V_P/V_C)}{R2 + r_o\, (V_P/V_C)}}$$

$$= 1 + \frac{R1\, [R2 + r_o\, (V_P/V_C)]}{R2\, r_o (V_P/V_C)}$$

$$A_V = 1 + \frac{R1}{R2} + \frac{R1\, V_C}{r_o\, V_P} \qquad (5)$$

In either case, the gain function is linear with V_C.

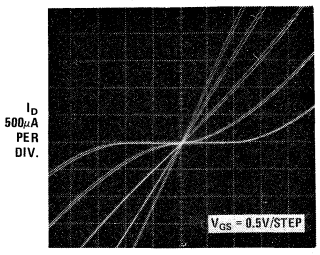
The circuits of *Figure 3* do indeed show a linear gain versus control voltage as plotted in *Figure 4* for several values of minimum gain. There is some non-linearity near minimum gain which appears in all curves. This is certainly due to a non-ideal characteristic of the FET caused by finite contact and bulk resistance at source and drain. *Figure 5* shows a similar control curve for a FET with longer channel in which the controlled channel resistance is a greater part of the total resistance than that of the short channel device of *Figure 4*. For those applications requiring a more precisely linear control of gain, the long channel devices will be preferable.

Several variable-gain circuits can be made to track when monolithic multiple FET's are used as the control elements with matched feedback resistors. A monolithic FET dual (NSC 2N3958) used in two identical control circuits shows remarkable tracking over the entire control range, even when V_{GS} is near V_P where variations would be expected to be most apparent. The plots appear in *Figure 6.* Similar performance for a quad gain control using a monolithic P-channel quad FET (AM97C09 or AM9709) is shown in *Figure 7.*

DISTORTION

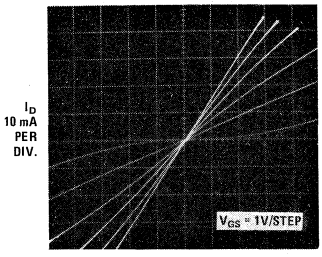
Reference to *Figure 2* will show that the FET acts as a linear resistance only for relatively small values of drain-source voltage, in either polarity. This is particularly apparent for positive V_{DS} (for N-channel FET) and V_{GS} approaching V_P. The difference between *Figures 2c and 2d* indicates that the maximum allowed applied signal will be greater for high V_P as compared with low V_P.

It is possible to improve the linearity characteristics somewhat by applying a part of the V_{DS} in series with the control voltage applied as V_{GS}. The circuit to accomplish this is that shown in *Figure 8.* It happens that about half of V_{DS} applied to the gate provides the greatest improvement for small signals. The addition of two resistors and one capacitor as in *Figure 8a* is all that is required. The capacitor simply blocks the control voltage from the FET drain and the op amp input. *Figure 8b* shows the addition of an emitter follower to



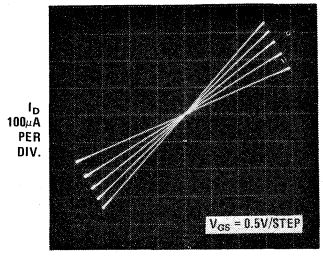
V_{DS} = 0.5V/DIV.

a) V_P = 2.8V



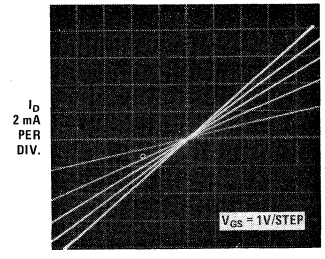
V_{DS} = 0.5V/DIV.

b) V_P = 9V



V_{DS} = 50 mV/DIV.

c) V_P = 2.8V



V_{DS} = 50 mV/DIV.

d) V_P = 9V

FIGURE 9. AC Output Characteristics of FET with Feedback Linearization

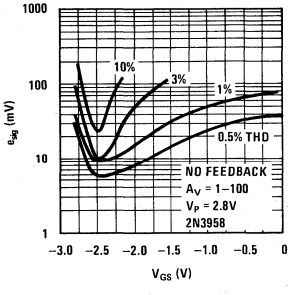


FIGURE 10. Distortion With V_P = 2.8V

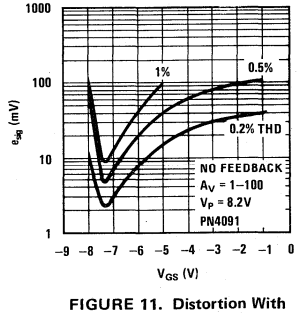


FIGURE 11. Distortion With V_P = 8.2V

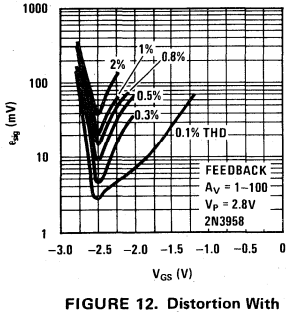


FIGURE 12. Distortion With V_P = 2.8V, With Linearization

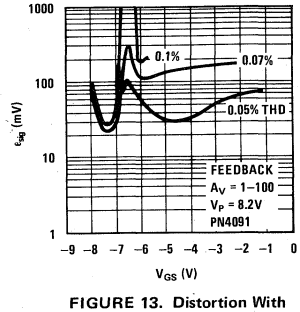


FIGURE 13. Distortion With V_P = 8.2V, Linearized

prevent abrupt changes in V_C from coupling to the op amp. *Figure 9* shows the improved linearity of the drain characteristics as compared to *Figure 2.* The improvement is also seen in the distortion versus input signal plots of *Figures 10–13.* Note particularly that the distortion at any value of V_C is primarily a function of input signal (which equals the feedback signal applied to the FET drain at the inverting input). Some modification is made to this direct relationship if an R2 is shunted across the FET as in *Figure 3b.* Measured distortion at low signal level is the result of noise rather than of signal distortion. Maximum gain is limited to about 100 in these plots so as to avoid the region of lower S/N. The noise is that of the op amp input stage and the signal source resistance plus the contribution of the FET which is essentially the thermal noise of r_d.

BANDWIDTH AND CONTROL TIME CONSTANT

The circuit bandwidth is the closed loop bandwidth of the op amp used at the (instantaneous) set gain. The gain control time constant is that of the input circuit to the FET (dependent on the value of R in *Figure 8*) limited by the slew rate of the op amp. The FET itself reacts practically instantly, producing a step change in feedback ratio. Control time constant is thus a few microseconds at most.

APPLICATIONS

Three obvious applications present themselves; they are:

1. Remote or multichannel gain control

2. Volume expansion

3. Volume compression/limiting

To this short list might be added a number of others, including applications in noise reduction and quad sound techniques.

The gain-controlled amplifier of *Figure 14* has a gain range of 1–1000, a maximum output level of 8.5 Vrms, and a bandwidth of better than 20 kHz at maximum gain. The FET used has high V_P for maximum freedom from distortion. *Figures 15 and 16* show the gain function and constant distortion contour lines. Note that the gain control curve is non-linear near unity gain because the PN4091 is a short channel FET. Distortion is quite low except as limited by maximum output voltage. Note that the maximum e_{in} is restricted by output saturation. The LM318 is used in the example only to achieve wideband response at maximum gain. The amplifier input voltage must be restricted to about 8 mVrms at maximum gain when the S/N will be about 60 dB over a 10 kHz bandwidth.

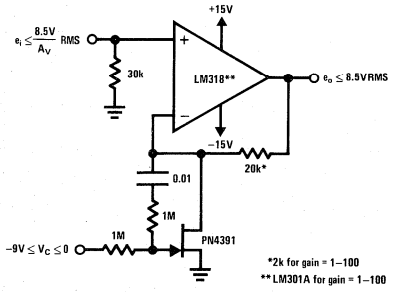


FIGURE 14. Amplifier With Gain Range = 1–1000

A more practical circuit might employ a gain range of 1–100. Then the amplifier could be a LM301A and still achieve a 10 kHz bandpass at maximum gain. The input signal could, accordingly, be increased to 80 mVrms for a S/N of 80 dB. This performance can be extended to dual and quad control circuits with tracking gain functions, but watch the bandwidth as required at maximum gain. Any of the several dual op amps could be used with the 2N3958 (monolithic dual from NSC), or the LM324 quad op amp can be used in limited gain times bandwidth applications with a quad monolithic FET. *Figure 17* shows all details of an ac coupled tracking quad gain control with 40 dB range. Gain varies over 1–100 range, bandwidth is 10 kHz minimum, S/N is better than 70 dB with 4.3 Vrms maximum output. *Figure 7* shows the gain curve and matching characteristics.

Noise considerations could be important in this method of gain control, as the signal is amplified rather than attenuated. To realize the function of a 40 dB variable attenuator, it is necessary to install a fixed attenuator at the amplifier input and perhaps also at the output. This will reduce the minimum signal level to millivolts, thus a low noise amplifier is desirable. The LM381 dual low-noise ac coupled amplifier could be used in a 40 dB

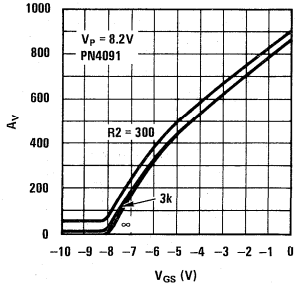


FIGURE 15. Gain For Circuit of Figure 14

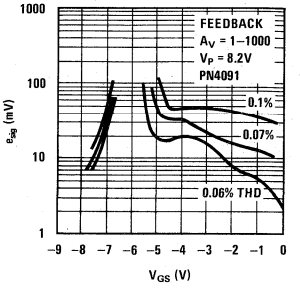


FIGURE 16. Distortion For Circuit of Figure 14

A Linear Multiple Gain Controlled Amplifier

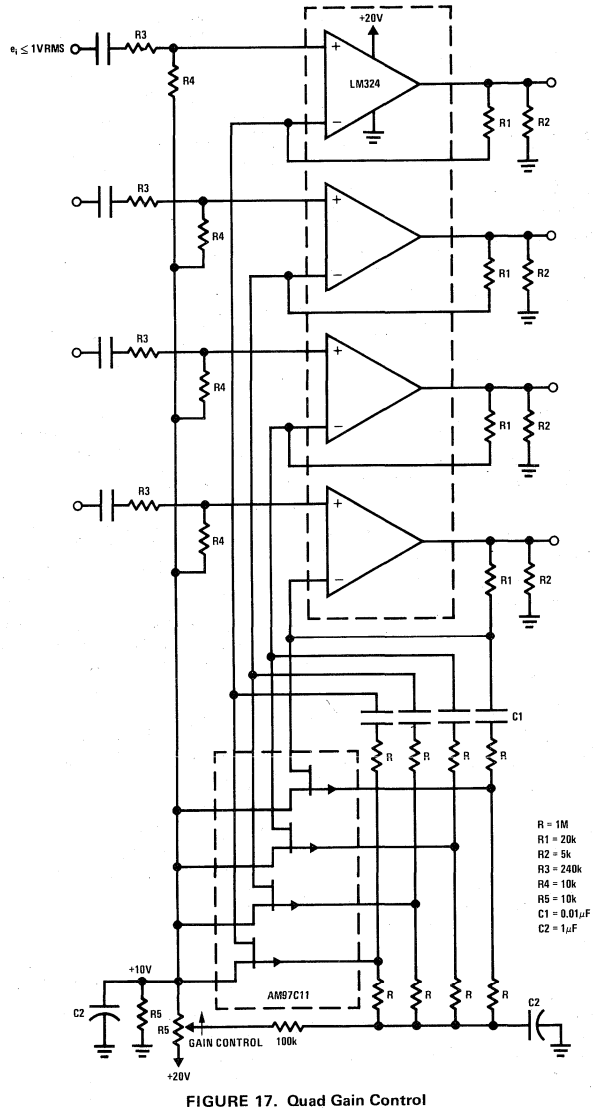


FIGURE 17. Quad Gain Control

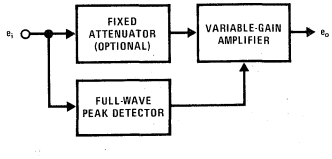


FIGURE 18. Volume Expander/Compressor Block Diagram

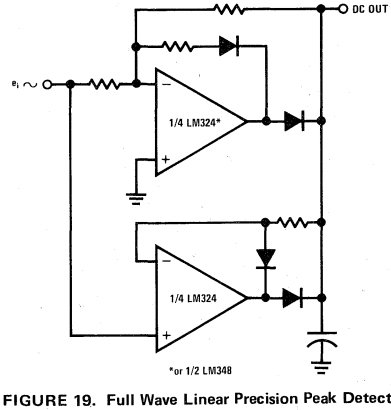


FIGURE 19. Full Wave Linear Precision Peak Detector

audio attenuator to realize S/N about 100 dB or in a 60 dB attenuator to realize 80 dB S/N. Improvements in S/N can be made by reducing system bandwidth in fixed or low frequency operation. Minimum noise is also achieved by using the minimum practical amplifier source resistance. Values as low as 1 kΩ are advantageous.

The effect of temperature will be to change the gain according to the temperature sensitivity of the FET. This effect can be reduced by using a silicon resistor for the feedback resistor, R1. If the FET were to be integrated onto the op amp chip, an attempt should be made to include R1 on the chip as well.

The application to a volume expander circuit is of interest as the control is linear, the required control range is only about 1:4, and the input signal is small for the low gain condition when distortion would otherwise be most apparent. The elements of a volume expander are indicated in *Figure 18.* The gain controlled amplifier need only exhibit a 12 dB variation in gain, being lowest for small signals. The slope of gain versus control should be linear, more specifically the slope of (log) gain in dB versus (log) signal in dB should be linear. A practical range is 12 dB gain change over a 30 dB input signal range. The peak detector should be linear down to very small signals, exhibit a fast attack or charge time of a millisecond or less, a discharge time constant of about 2 seconds, and operate on the first half cycle (full-wave detector). The detector should, therefore, be a full-wave precision linear peak detector with low internal impedance; the requirements can be met with the circuit of *Figure 19.*

The expander circuit shown in *Figure 20* will perform as desired. The gain control function is plotted in *Figure 21;* distortion is below 0.1% at all levels. Resistors R3 and R4 are added in order to modify the linear control curve to the desired log curve. Note that the input signal is attenuated prior to amplification in order to reduce distortion and maintain an overall gain of approximately 0 dB at midrange of expansion. The noise with the LM124 over a 20 kHz bandwidth is, of course, a function of signal; but the maximum signal to noise ratio is 80 dB. The circuit could be adapted to stereo or quad sound as in *Figures 22–23.* Questions for individual design concern the method of control. Whether to expand all channels together, and whether to derive the control signals individually from each channel, a summation from 2 to 4 channels, or from a single channel (assuming that high level from any channel indicates high levels from all channels). Note that the FET is biased OFF (minimum gain) for low signals, and increasing signals progressively bias the FET ON (maximum gain).

The volume compression circuit is a logical mate to the expander. The only difference would be that the FET is initially biased ON (maximum gain) for low signals, and

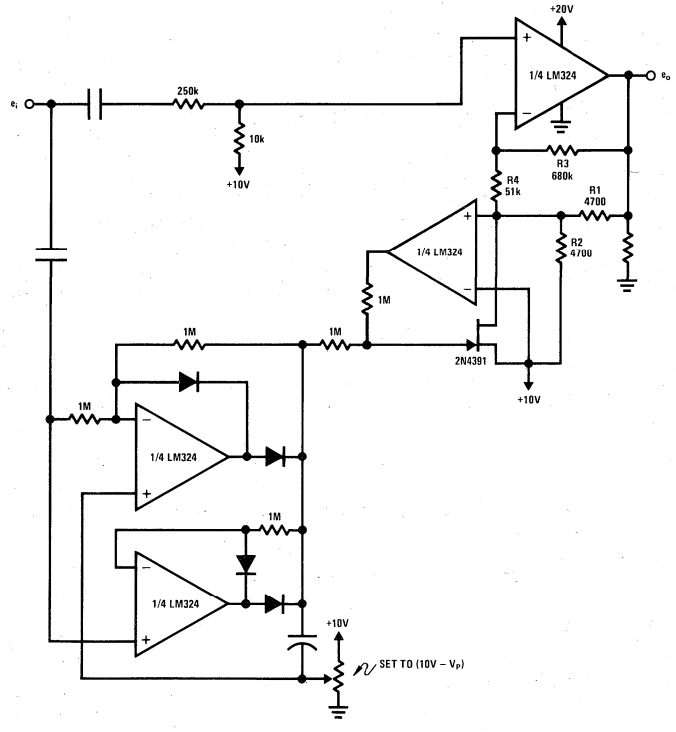


FIGURE 20. Volume Expander Circuit

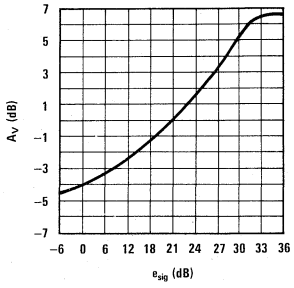


FIGURE 21. Expander Gain Characteristic

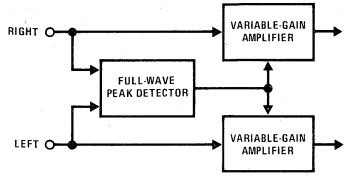
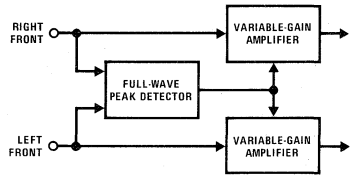


FIGURE 22. Stereo Expander Block



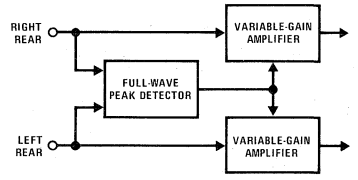


FIGURE 23. Four-Channel Expander Block

increasing signals progressively bias the FET OFF (minimum gain). A disadvantage is that the circuit produces greatest distortion in the low gain condition when signals are highest. Maximum S/N is degraded by 24 dB over that of the expander, minimum S/N is the same.

CONCLUSION

The combination of FET and op amp provides a linear dc (voltage) control of gain over a range to 60 dB. As the circuit realizes positive gain, rather than being a controlled attenuator, the input signal is limited. Input signal is further limited to several hundred millivolts by the non-linearity of the FET (which sees the full input signal). Because input signals will generally be in the 10–300 mV range, noise performance of the selected op amp will be important. Even so, S/N of 60–100 dB is obtainable with standard amplifiers. Tracking pair or quad gain-control amplifiers are realizable with existing monolithic dual or quad FET's, and the combination of FET and op amp lends itself to simple integration. The circuit is well-suited to remote and multiple linear gain control and to volume expander/compressors. The volume expander is especially interesting as the signal level and gain conditions result in extremely low distortion and more than adequate signal-to-noise ratio.

Binary/BCD Gain Programmed Amplifiers

National Semiconductor
John Maxwell
February 1977

Many systems require logic controlled gain programmable amplifiers (GPA) for signal preconditioning, level control and dynamic range expansion. The system sets GPA requirements for accuracy, speed and signal handling capability, limiting the type used. Conventional CMOS analog switches limit signal handling to ±7.5V and accuracy to 1%. High voltage CMOS or JFET analog switches increase both accuracy and signal handling (±10V to ±15V) but at a greater cost. Programmable amplifiers using current mode analog switches have the highest signal handling capability (±25V) with high accuracy, speed and low cost.

In reality, the logic controlled GPA is a multiplying digital-to-analog converter (multiplying D/A). The D/A input is the reference node which is multiplied by the digital input. Multiplying D/A converters have been available for some time in module, hybrid and monolithic form but suffer from high cost and poor signal handling capability (±10V maximum).

Large signal handling (±25V), moderate cost multiplying D/A converters can be built using monolithic current mode analog switches, an op amp and a few resistors.

Unlike conventional analog switches, only signal current is switched at the virtual ground of an op amp with current mode analog switches. Limiting the voltage across the switch to a few hundred millivolts, power supplies, logic interface and level translator circuits are eliminated allowing the JFET switches to be driven directly by standard logic.

A logic "0" turns the switch ON with a logic "1" shutting the switch OFF by pinching the FET OFF. The diode is used to clamp the source to drain voltage to about 0.7V in the switch OFF state. The series FET in the feedback path is used to compensate for the ON resistance of the switch FET.

Current through the switch is determined by the input resistor, R1, the switch ON resistance and the input voltage, V_{IN}. Scaling of the output voltage is accomplished with the feedback resistor, setting the gain of the amplifier.

$$A_V = -\frac{R2 + R_{ON2}}{R1 + R_{ON1}} \qquad (1)$$

A 4-bit multiplying D/A converter can be built using a quad current mode switch, 4 binary weighted resistors (R, 2R, 4R, 8R) and an op amp. The output voltage will be a function of the feedback resistor, input resistors and the logic state of the FET gates, G_N.

The number of bits is expanded by cascading another quad current switch and resistor array to the first. Instead of continuing the binary progression of the input resistors, (16R, 32R, etc), current splitting resistors are used such that the same resistor array (R, 2R, 4R, 8R) is used for the additional bits, minimizing the number of resistor values required for higher order converters.

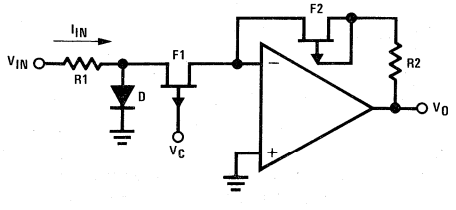
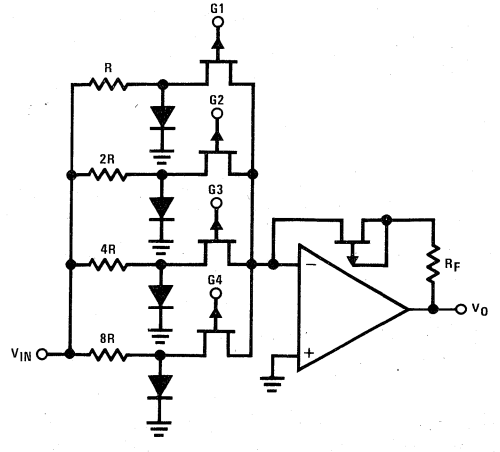
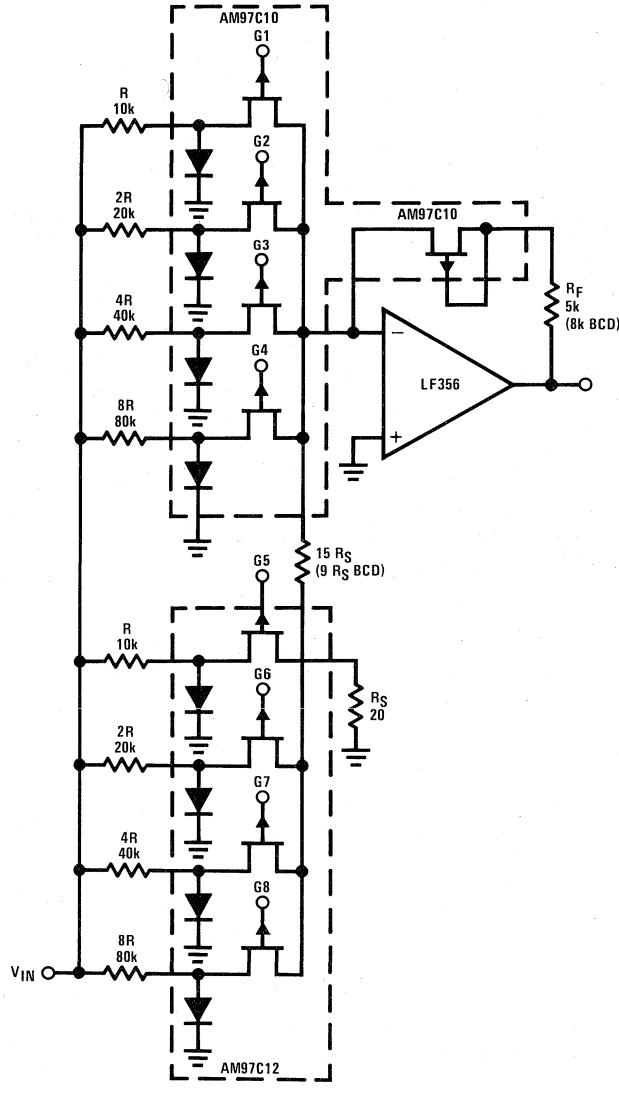


FIGURE 1. Current Mode Analog Switch



$$V_O = -V_{IN}\frac{R_F}{R}\left(\overline{G}1\,2^0 + \overline{G}2\,2^{-1} + \overline{G}3\,2^{-2} + \overline{G}4\,2^{-3}\right)$$

FIGURE 2. 4-Bit Multiplying D/A Converter



$$V_O = -V_{IN}\frac{R_F}{R}\left[\overline{G}1\,2^0 + \overline{G}2\,2^{-1} + \overline{G}3\,2^{-2} + \overline{G}4\,2^{-3} + 1/16\,(\overline{G}5\,2^0 + \overline{G}6\,2^{-1} + \overline{G}7\,2^{-2} + \overline{G}8\,2^{-3})\right]$$

(1/10 for BCD)

FIGURE 3. 8-Bit Multiplying D/A Using Cascaded 4-Bit Sections

Binary weighting requires a 1/16 current split for the second switch quad while BCD weighting requires a 1/10 split.

There are 2 basic switch configurations available that are optimized for a variety of logic drives: TTL or CMOS Multiple independent switches (4 by SPST) and a 4-channel multiplex version with a series compensation FET.

Practical limitations in using monolithic current mode analog switches need consideration. Resistor values and tolerance impacted by switch resistance is minimized by increasing resistor values without regard, but limits bandwidth and creates leakage errors at elevated temperatures. Using resistors that are too small, increase switch resistance errors. Current saturation (increased switch resistance) occurs when the switch current approaches the FET saturation current, I_{DSS}. High currents also

cause $I_{G(ON)}$, current lost through the gate, as the diode and FET source to gate diode become forward biased. An input resistor value of 10k limits the switch current to less than 2 mA minimizing both leakage and switch resistance problems. For example, the gain accuracy at unity gain using the compensation FET is less than 0.05% with $R = R_F = 10k$.

The current shunt resistor used in cascading switches should be kept small to minimize the voltage drop, keeping the FET drains near ground. Values of R_S should be less than 100Ω (20 typ).

Resistor tolerance will be determined by converter resolution, i.e., the number if bits (N). For example, an 8-bit binary D/A converter will have 2^N-1 or 255 steps (99 for BCD) or different gains. The resolution or smallest step is (least significant bit) $1/2^N$ of the full-scale value (0.0039). Typical accuracy specifications for D/A converters are stated as 1 LSB or ±1/2 LSB.

This works out to be ±0.2% for the 8-bit binary unit. Errors in the feedback resistor directly affect the output of the converter. The most significant resistor, R, contributes 1/2 full-scale, reducing its error contribution by a factor of 2. The same is true for the rest of the resistors with contributions of 1/4, 1/8, etc. Using a resistor tolerance of 0.1% for the feedback resistor, 0.2% for the 2 most significant resistors (R, 2R), 0.5% for the 3rd and 1% for the 4th and 5th switches allows 5% resistors to be used in the 6th, 7th and 8th switch positions.

Using the above information, 4-bit or more binary/BCD gain programmable amplifiers can be built with large signal handling capability, few parts and easily adjustable gain or attenuation. *Figure 3* shows a practical 8-bit binary/BCD GPA with gains of 0.996 (binary) with R_F = 5k and 0.99 (BCD) with R_F = 8k. For other gains, only the feedback resistor need be changed.

$$\% \text{ error} = \left[\epsilon_f^2 + \left(\frac{\epsilon_R}{2}\right)^2 + \left(\frac{\epsilon_{2R}}{2^2}\right)^2 + \cdots + \left(\frac{\epsilon_{nR}}{2^n}\right)^2 \right]^{1/2}$$

or

$$\% \text{ error} = \left[(0.1)^2 + \left(\frac{0.2}{2}\right)^2 + \left(\frac{0.2}{4}\right)^2 + \cdots + \left(\frac{5}{256}\right)^2 \right]^{1/2} = \pm 0.198\% \qquad (2)$$

ϵ_f = tolerance of feedback resistor
ϵ_R = tolerance of most significant resistor
ϵ_{nR} = tolerance of Nth resistor

FET Curve Tracer

National Semiconductor
John Maxwell
February 1977

Junction field-effect transistors (JFETs), unlike bipolar transistors, do not easily lend themselves to analytic solutions of bias networks. By their very nature, JFETs are voltage controlled devices. Gate to source voltage (control voltage V_{GS}) variations of several volts can exist within a given part type at the same operating conditions, causing the problem. Multiple suppliers and inadequate or non-existent data sheet curves compound the problem further, requiring data from the suppliers or the use of a curve tracer.

A simple curve tracer, used with any oscilloscope, can be built using a quad op amp and a handful of parts. The circuit displays drain current versus gate voltage for both P and N-channel JFETs at a constant drain voltage.

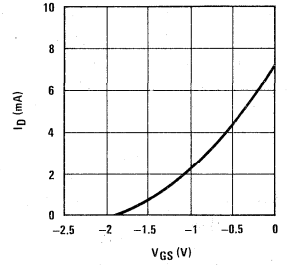


FIGURE 1. Typical N-Channel FET Transfer Curve

The circuit consists of an op amp current to voltage (I/V) amplifier with a positive or negative gate sweep

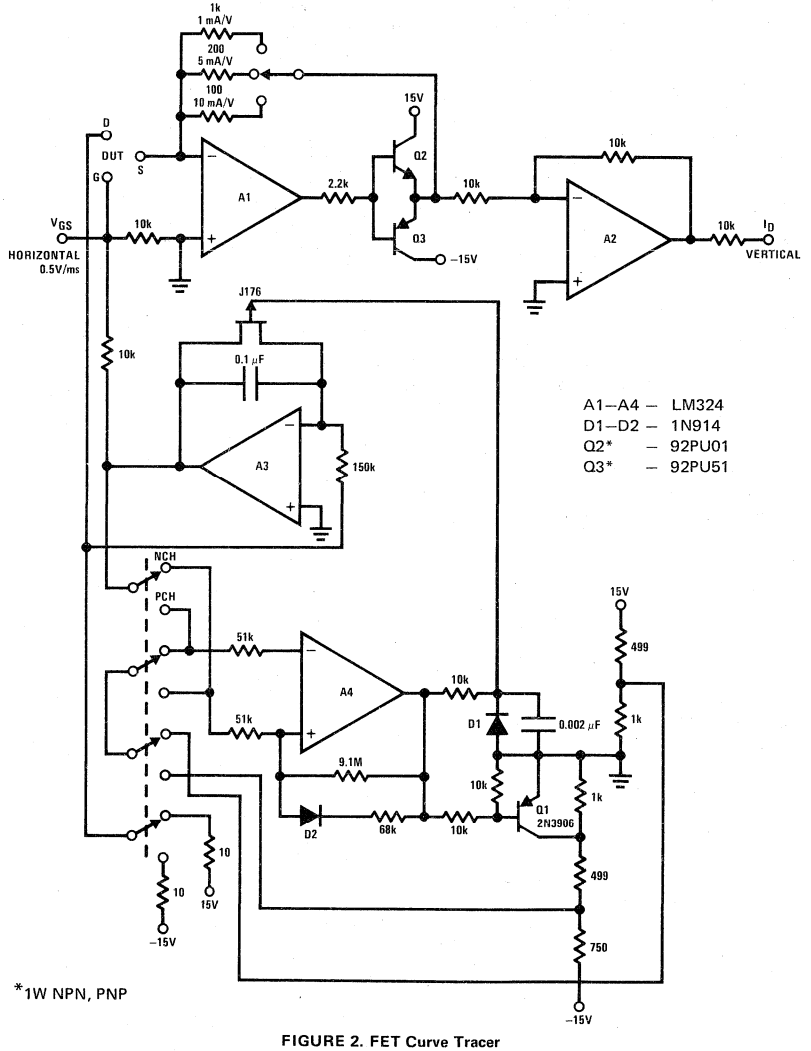


FIGURE 2. FET Curve Tracer

voltage. The I/V amplifier uses 1/4 of the quad op amp and 3 switchable feedback resistors for drain current scaling: 1k for 1 mA/V, 200Ω for 5 mA/V and 100Ω for 10 mA/V. An NPN-PNP emitter-follower buffer is used with the I/V amplifier to handle high FET currents (to 100 mA). A unity gain inverting amplifier is used for proper drain current polarity.

The gate sweep generator consists of 2 parts, a linear ramp generator with a reset and a window comparator. The ramp generator is an op amp with a capacitor in its feedback loop. The sweep rate is set by a constant current supplied to the capacitor through a resistor tied to either the plus or minus voltage supply.

The positive (P-channel) ramp mode uses the positive reference on the plus input of the comparator with the ramp connected to the minus input. The comparator output stays high (15V) pinching the FET OFF until the input exceeds the reference (10V). At that point, the output snaps to the negative supply, turning the FET switch ON, discharging the capacitor. The reference voltage at the plus input is set near ground using the 51k input resistor, D2 and 68k feedback resistor when the comparator output is in the low state. When the capacitor is discharged, the comparator resets, restarting the ramp.

A negative sweep is more difficult to generate using the same comparator. The reference (−10V) is on the minus input with the ramp connected to the plus input. As with the positive sweep, the comparator output is high until the negative sweep exceeds the reference. The difference is that the reference cannot be set to ground for the reset sweep but to a negative voltage such that when the ramp is at 0V the comparator resets. The function of Q2 is to short R1, changing the reference voltage from −10V to −6V.

In both cases, the sweep time is 10 ms. The resistor attenuator on the FET gate terminal divides the voltage in half, yielding a sweep rate of 0.5V/ms with a maximum gate voltage of ±5V. This should be adequate for most FETs used as amplifiers but if additional gate voltage is required, the attenuator can be switched out.

The circuit is limited to displaying only the FET transfer characteristic I_D vs V_{GS}, but this is the curve most needed by designers. It gives insight into parameter variations of bias circuits and it can be used to observe temperature effects on the FET. The oscilloscope vertical input is used for the drain current and the horizontal input is used for the gate voltage. The horizontal sweep can be used if no horizontal input is available where a sweep rate of 0.5 ms/cm corresponds to 0.5V/ms, allowing the curve tracer to be used with any oscilloscope.

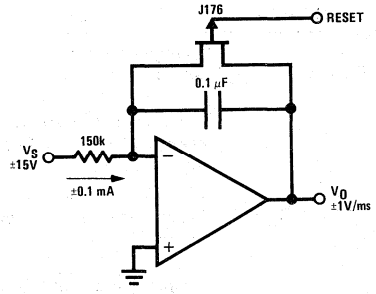


FIGURE 3. Linear Ramp Generator

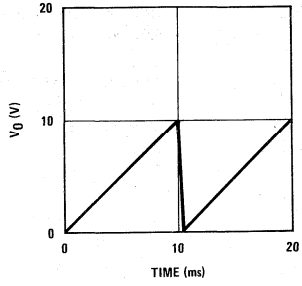


FIGURE 4. Positive Sweep

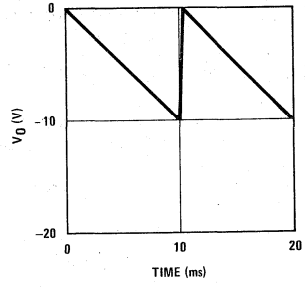


FIGURE 5. Negative Sweep

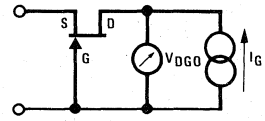
JFET Glossary of Symbols

DC PARAMETERS

BV_{DGO} (V) or BV_{GDO}

Drain-Gate Breakdown Voltage with Source Open-Circuited

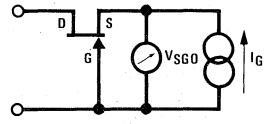
The breakdown voltage of the drain-gate junction, measured at a specified current with the source open-circuited.



BV_{SGO} (V) or BV_{GSO}

Source-Gate Breakdown Voltage with Drain Open-Circuited

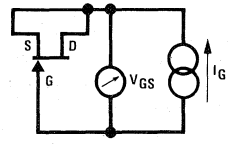
The breakdown voltage of the source-gate junction, measured at a specified current, with the drain open-circuited.



BV_{GSS} (V) or BV, $V_{(BR)GSS}$

Source-Gate Breakdown Voltage with Drain-Source Shorted

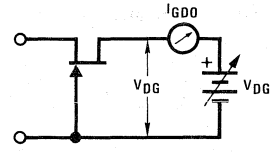
The breakdown voltage of the source-gate and drain-gate junctions, measured at a specified current with the drain-source shorted.



I_{DGO} (pA) or I_{GDO}

Drain-Gate Leakage Current, Source Open-Circuited

The leakage current of the drain-gate junction, measured at a specified voltage, with the source open-circuited.



I_D (μA) or $I_{D(ON)}$

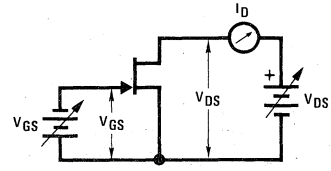
Drain ON Current

The drain current, measured at a specified drain-source voltage and gate-source voltage.

$I_{D(OFF)}$ (pA)

Drain Cutoff Current

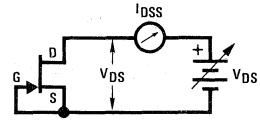
The drain cutoff current, measured at a specified drain-source voltage and gate-source voltage.



I_{DSS} (mA)

Drain Saturation Current

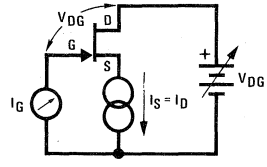
The drain current, measured at a specified drain-source voltage with the source shorted to the gate ($V_{GS} = 0$)



I_G (pA) or $I_{G(ON)}$

Gate Leakage Current with Drain Current Flowing

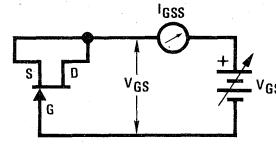
The gate leakage current, measured at a specified drain current and drain-gate voltage.



I_{GSS} (pA)

Gate-Source Reverse Leakage Current with Drain-Source Shorted

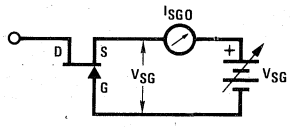
The gate-source reverse leakage current measured at a specified gate-source voltage.



I_{SGO} (pA) or I_{GSO}

Source-Gate Reverse Leakage Current with Drain Open-Circuited

The leakage current of the source-gate junction, measured at a specified voltage, with the drain open-circuited.



r_{DS} (Ω) or r_{ds}, R_{DS}, $r_{DS(ON)}$

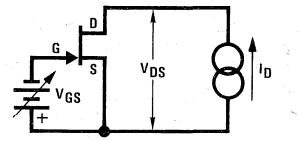
Drain-Source ON Resistance

The drain-source ON resistance, measured at a specified gate-source voltage and drain current.

$V_{DS(ON)}$ (mV)

Drain-Source ON Voltage

The drain-source ON voltage, measured at a specified gate-source voltage and drain current.

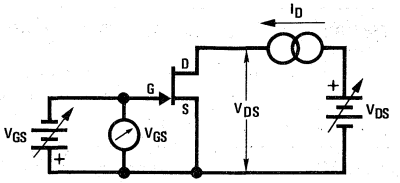


$$r_{DS} = \frac{V_{DS}}{I_D}$$

V_{GS} (V) or $V_{GS(ON)}$, V_G

Operating Gate-Source Voltage

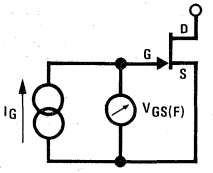
The gate-source voltage, measured at a specified drain current and drain-source voltage.



$V_{GS(F)}$ (V)

Forward Gate-Source Voltage

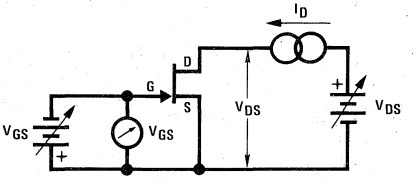
The forward gate-source voltage, measured at specified current.



$V_{GS(OFF)}$ (V) or V_P

Gate-Source Cutoff (Pinch-Off) Voltage

The gate-source cutoff voltage, measured at a specified drain current and drain-source voltage.

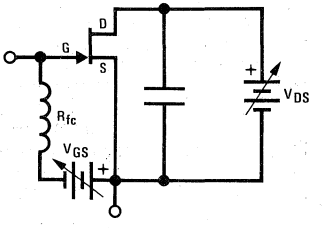


SMALL SIGNAL PARAMETERS

C_{iss} (pF) or C_{iss}, C_{gss}

Common-Source Input Capacitance

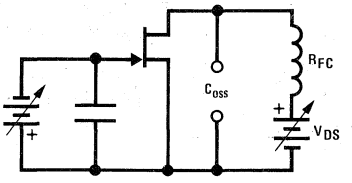
The common-source input capacitance measured between the gate and source with the drain A–C shorted to the source at specified drain-source and gate-source voltages.



C_{oss} (pF) or C_{os}, C_{dss}

Common-Source Output Capacitance

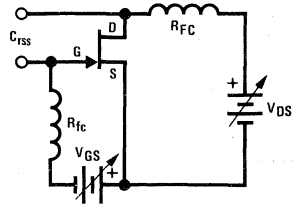
The common-source output capacitance, measured between the drain and source with the source A–C shorted to the gate at specified drain-source and gate-source voltages.



C_{rss} (pF) or C_{rs}, C_{dg}

Common-Source Reverse Transfer Capacitance

The common-source reverse transfer capacitance, measured between the drain and gate at specified drain-source and gate source voltages.

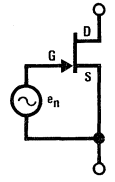


---

e_n (nV/$\sqrt{Hz}$) or e_n, V_n, E_n

Equivalent Input Noise Voltage

The equivalent input noise voltage per unit bandwidth, measured with the input A–C shorted to the source at a specified operating condition.

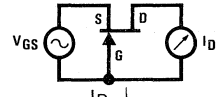


---

g_{fg} (mV) or y_{fg}

Common- Gate Forward Transconductance

The common-gate forward transconductance with the output A–C shorted. This is a complex quantity ($g_{fg} + jb_{fg}$).



$$Y_{fg} = \frac{I_D}{V_{GS}}\Bigg|_{V_{DS}=0}$$

---

g_{fs} (mV) or g_m, Y_{fs}, $Re|Y_{fs}|$

Common-Source Forward Transconductance

The common source forward transconductance with the output A–C shorted. This is a complex quantity ($g_{fs} + jb_{fs}$).

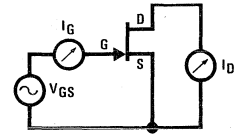
$$Y_{fs} = \frac{I_D}{V_{GS}}\Bigg|_{V_{DS}=0}$$

---

g_{iss} (μV) or Y_{is}

Common-Source Input Conductance

The common-source input conductance with the output A–C shorted. This is a complex quantity ($g_{is} + jb_{is}$).



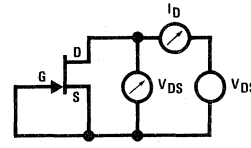
$$Y_{is} = \frac{I_G}{V_{GS}}\Bigg|_{V_{DS}=0}$$

---

g_{oss} (μV) or Y_{os}

Common-Source Output Conductance

The common source output conductance with the input A–C shorted. This is a complex quantity ($g_{os} + jb_{os}$).



$$Y_{os} = \frac{I_D}{V_{DS}}\Bigg|_{V_{GS}=0}$$

G_{pg} (dB)

Common-Gate Power Gain

The common-gate power gain is the ratio of output power to input power.

G_{ps} (dB)

Common-Source Power Gain

The common-source power gain is the ratio of output power to input power.

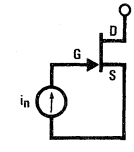
$$G_p = 10 \log_{10} \frac{P_o}{P_i}$$

---

i_n (pA/$\sqrt{Hz}$)

Equivalent Input Noise Current

The equivalent input noise current measured with the input open-circuited under specified operating conditions.



NF (dB)

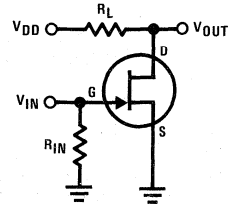
Spot Noise Figure

Noise figure = 10 $\log_{10}$ F were F is noise factor which is the ratio of the total output noise power to the output noise power of the source. Measured at specified operating conditions and source resistance.

$$F = \frac{\text{Total Output Noise Power}}{\text{Source Output Noise Power}}$$

COMMON-SOURCE SWITCHING PARAMETERS

In the following, drive circuit conditions and drain circuit conditions must be specified. The transition times of the input must be negligible compared to the measured times.



$t_{d(ON)}$

Turn-On Delay Time

The time interval during turn-on from the point when the input pulse at the gate reaches 10% of its full amplitude to the point when the drain pulse changes from 0 to 10% of its maximum amplitude.

t_r

Rise Time

The time interval during turn-on in which the drain current pulse changes from 10% to 90% of its maximum amplitude.

$$I_{D(ON)} = \frac{V_{DD} - V_{DS(ON)}}{R_L}$$

$t_{d(OFF)}$

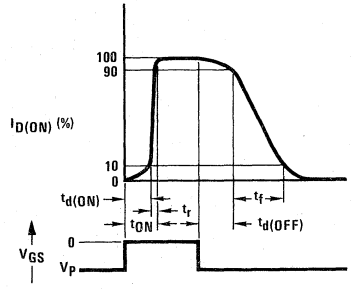
Turn-Off Delay Time

The time interval during turn-off from the point when the turn-off pulse at the gate changes from 100% to 90% of its full amplitude to the time when the drain current has changed from 100% to 90% of its maximum amplitude.

t_f

Fall Time

The time interval during turn-off in which the drain current pulse decreases from 90% to 10% of its maximum amplitude.

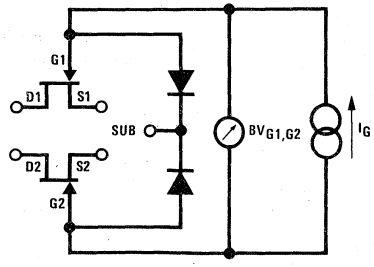


DUAL FET PARAMETERS

$BV_{G1, G2}$ (V) or BV_{G1-2}

Gate to Gate Breakdown Voltage

The breakdown voltage of the gate to gate junctions, measured at a specified current.

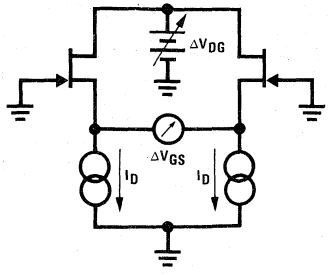


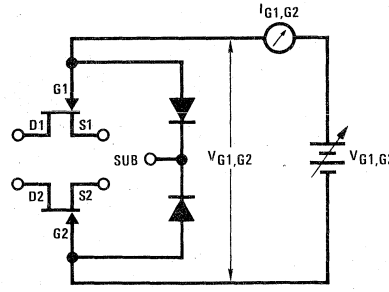
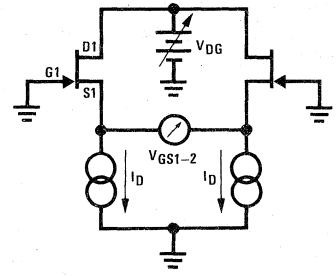
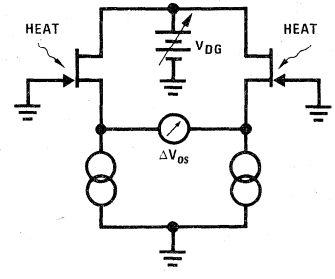
CMRR (dB) or CMR

Common-Mode Rejection Ratio

The common-mode rejection ratio is the ratio of the change in differential gate voltage with a change in the drain to gate voltage.

$$CMRR = 20 \log_{10} \frac{\Delta V_{DG}}{\Delta V_{os}}$$



g_{fs1-2} (%) or g_{fs1}/g_{fs2}	**Common-Source Forward Transconductance Ratio (Match)** The transconductance ratio = g_{fs1}/g_{fs2} x 100 (%) measured at specified drain-gate voltage and drain current.	
$g_{oss\ 1-2}$ (μV) or g_{os1-2}	**Common-Source Output Conductance (Match)** Output conductance match = $\lvert g_{os1}-g_{os2}\rvert$ measured at specified drain-gate voltage and drain current.	
I_{DSS1-2} (%) or I_{DS1-2}, I_{DSS1}/I_{DSS2}	**Drain Saturation Current Ratio (Match)** The drain saturation current ratio = I_{DSS1}/I_{DSS2} x 100% measured at specified drain-source voltages.	
I_{G1-2} (pA)	**Differential Gate Leakage Current** Differential gate leakage current = $\lvert I_{G1}-I_{G2}\rvert$ measured at specified drain-gate voltage and drain current.	
$I_{G1,\ G2}$ (pA)	**Gate to Gate Reverse Leakage Current** The gate to gate reverse leakage measured at a specified voltage monolithic dual with diode isolation shown.	
V_{GS1-2} (mV) or ΔV_{GS}, V_{os}, $\lvert V_{GS1}-V_{GS2}\rvert$	**Differential Gate-Source Voltage** The differential gate-source voltage, measured at a specified drain-gate voltage and drain current.	
ΔV_{GS1-2} (μV/°C) or $\Delta\lvert V_{GS1}-V_{GS2}\rvert/\Delta T$ $\Delta V_{os}/\Delta T$	**Differential Gate-Source Voltage Drift** The differential gate-source voltage drift is the change in the differential gate-source voltage with a change in device temperature at a specified operating condition. $\frac{\Delta V_{os}}{\Delta T} = \left\lvert \frac{(V_{GS1}-V_{GS2})\lvert T_1 - (V_{GS1}-V_{GS2})\lvert T_2}{T_1-T_2} \right\rvert$	

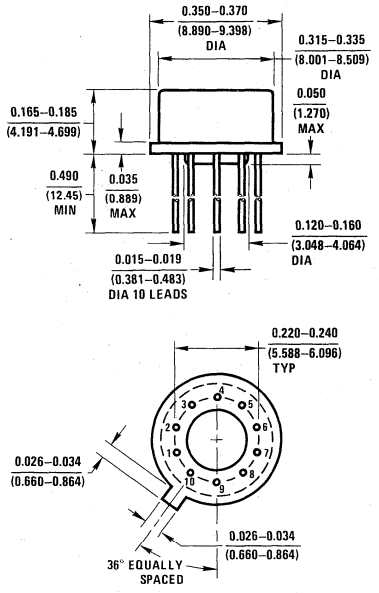
Section 7

Physical Dimensions

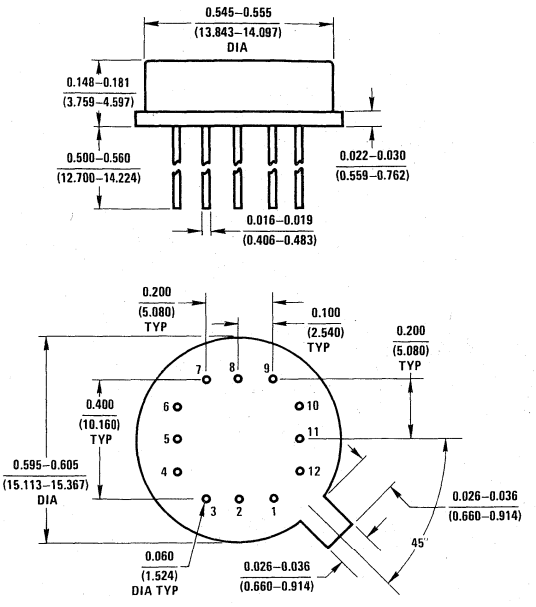
7

Physical Dimensions

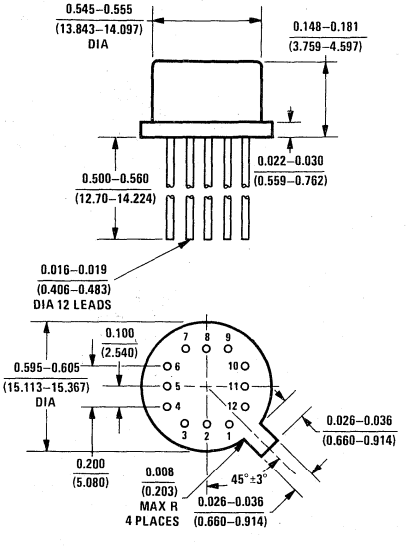
All dimensions expressed as inches / (millimeters)



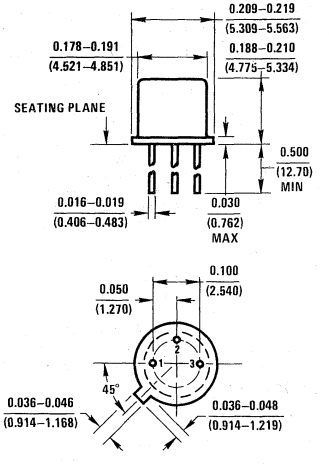
Package 1
10-Lead TO-5 Metal Can Package (H) (Low Profile)
NS Package Number H10A



Package 2
12-Lead TO-8 Metal Can Package (G)
NS Package Number H12B

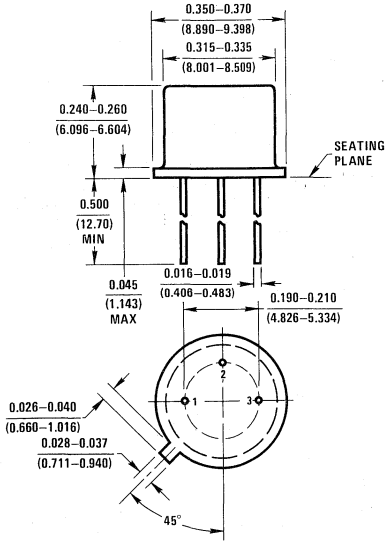


Package 3
12-Lead TO-8 Metal Can Package (G)
(AH2114/AH2114C Only)
NS Package Number H12C



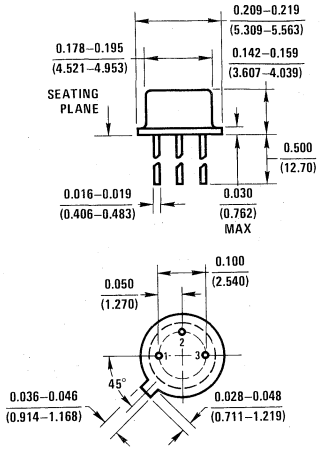
PIN	FET N(02)	FET P (11)
1	S	S
2	D	G
3	G	D

Package 4
3-Lead TO-18 (02, 11) Metal Can Package
NS Package Number H03D



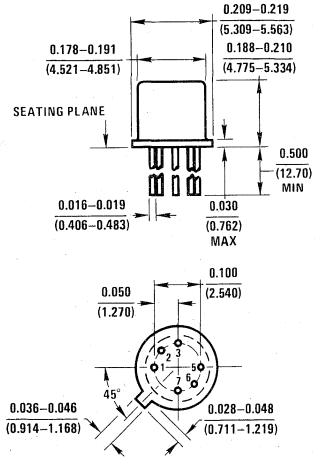
PIN	FET
1	S
2	D
3	G

Package 5
3-Lead TO-39 (09) Metal Can Package (H) (High Profile)
NS Package Number H03G



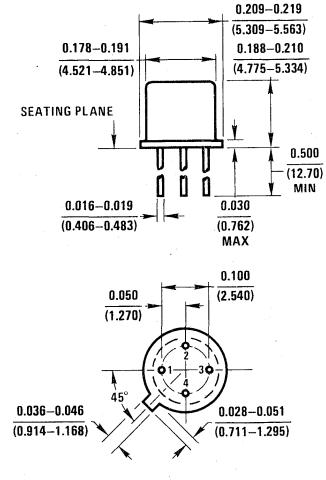
PIN	FET(07)
1	S
2	D
3	G

Package 6
3-Lead TO-52 (07) Metal Can Package
NS Package Number H03J



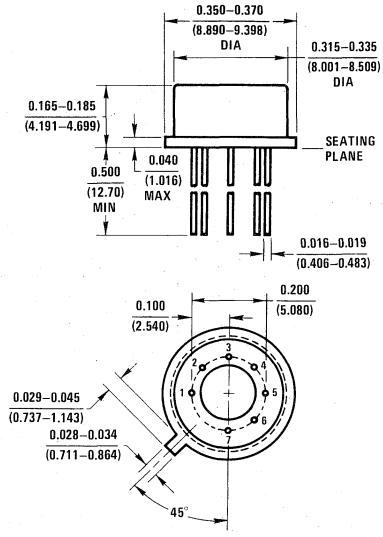
PIN	FET
1	S1
2	D1
3	G1
5	S2
6	D2
7	G2

Package 7
6-Lead TO-71 (12) Metal Can Package
NS Package Number H06A



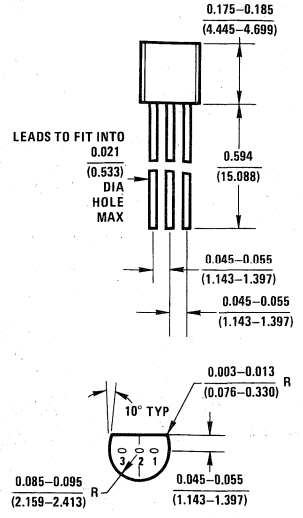
PIN	FET P(23)	FET N(25)
1	S	S
2	G	D
3	D	G

Package 8
4-Lead TO-72 (23, 25) Metal Can Package (H)
NS Package Number H04C



PIN	FET
1	S1
2	D1
3	G1
4	Case
5	S2
6	D2
7	G2

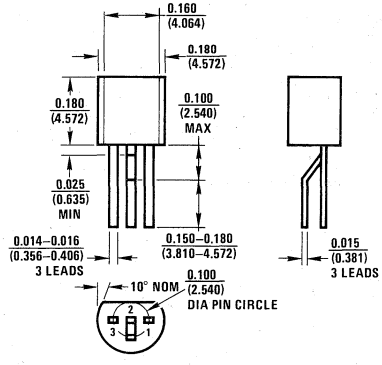
Package 9
6-Lead TO-78 (24) Metal Can Package (H)
NS Package Number H06B



PIN	71	72	74
1	G	G	S
2	D	S	G
3	S	D	D

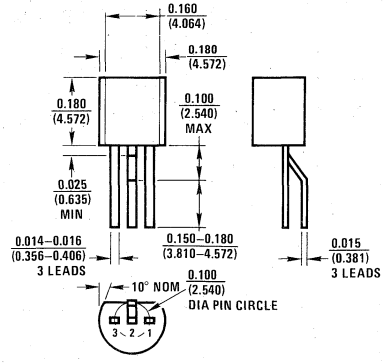
FET case 71 and 72 are interchangeable without compromise in performance except some RF application at VHF

Package 10
3-Lead TO-92 (71, 72, 74) Plastic Package
NS Package Number Z03A



PIN	FET
1	D
2	S
3	G

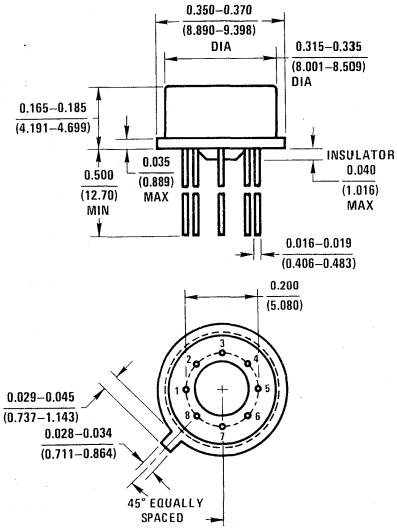
Package 11
3-Lead TO-92 (77) Plastic Package
NS Package Number Z03D



PIN	71	72	74
1	G	G	S
2	D	S	G
3	S	D	D

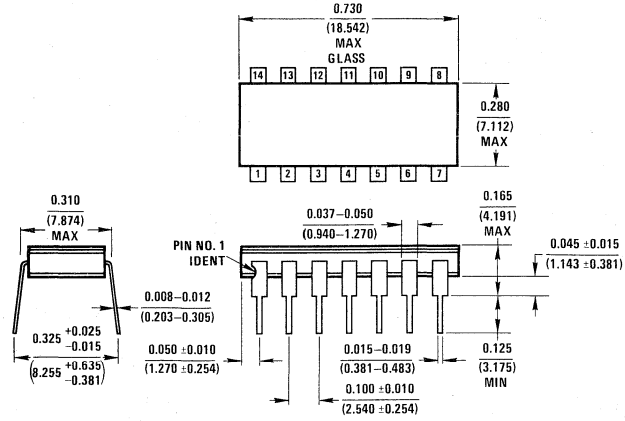
TO-18 lead form available on special order or standard on some products converted from TO-106 package.

Package 12
3-Lead TO-92 (TO-18 Lead Form) Plastic Package
NS Package Number Z03E

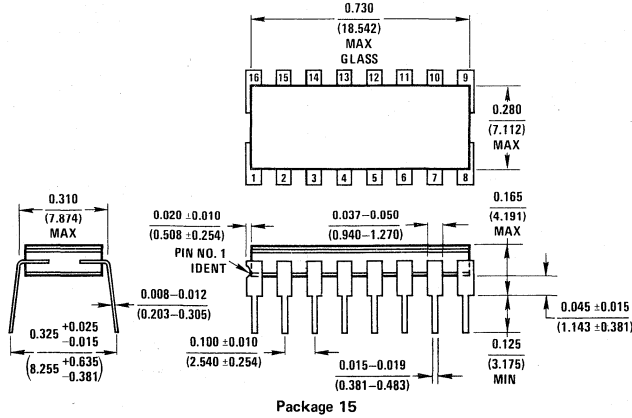


PIN	FET
1	S1
2	D1
3	G1
4	Case
5	S2
6	D2
7	G2
8	Sub

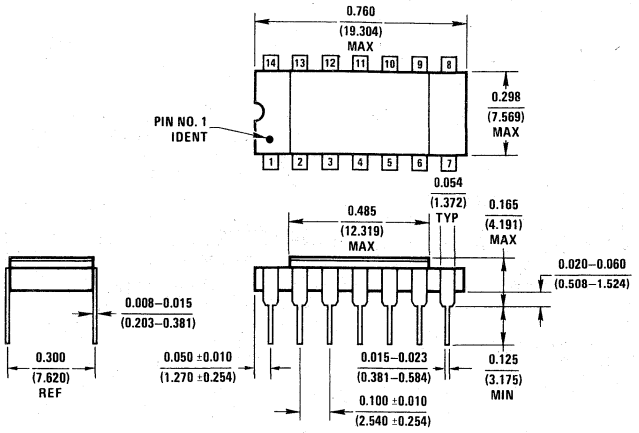
Package 13
8-Lead TO-99 (24 Alternate) Metal Can Package (H)
NS Package Number H08B



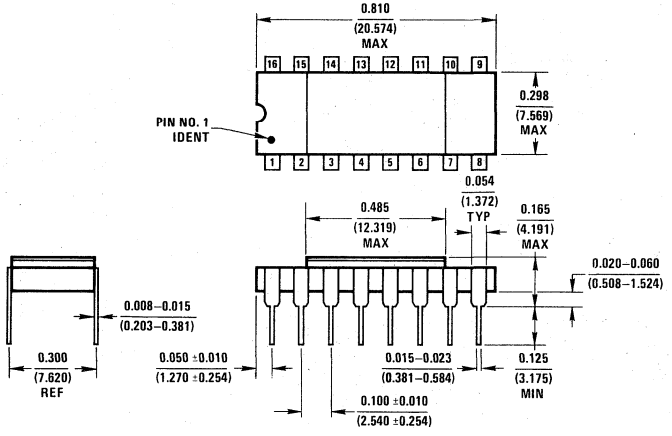
Package 14
14-Lead Cavity DIP (D)
NS Package Number D14A



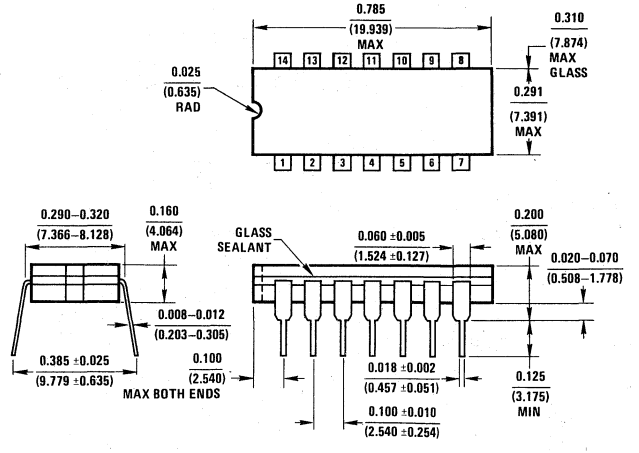
Package 15
16-Lead Cavity DIP (D)
NS Package Number D16A



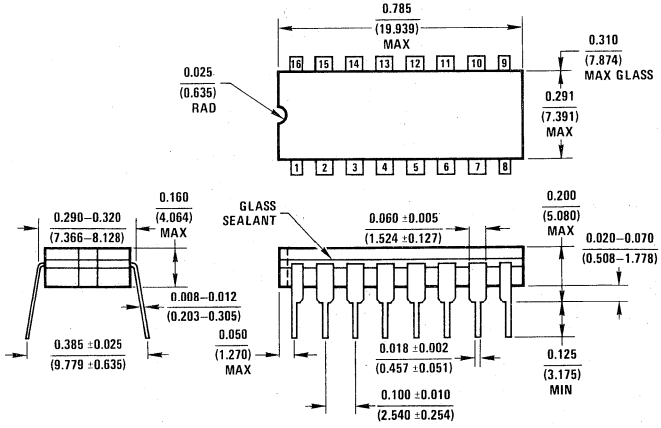
Package 16
14-Lead Side-Brazed Cavity DIP (D)
NS Package Number D14E



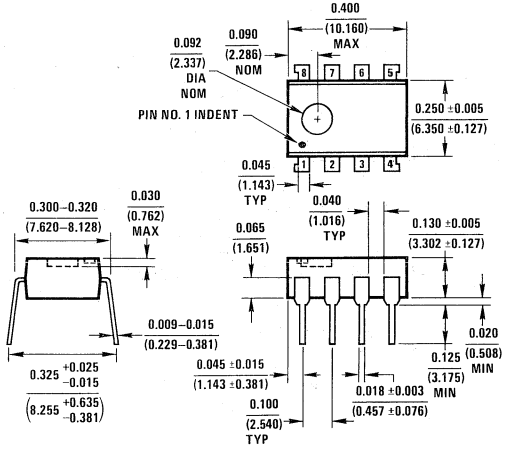
Package 17
16-Lead Side-Brazed Cavity DIP (D)
NS Package Number D16C



Package 18
14-Lead Cavity DIP (J)
NS Package Number J14A

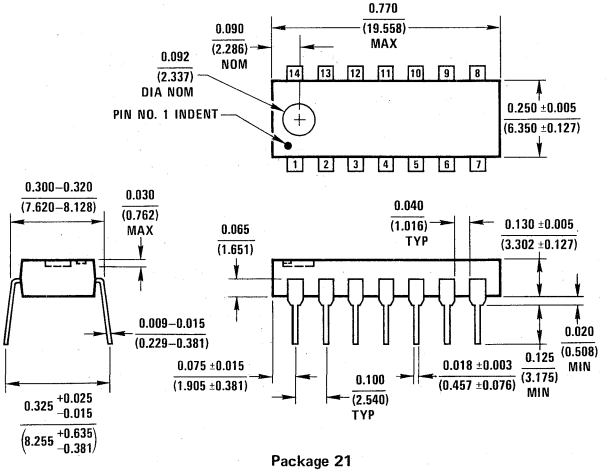


Package 19
16-Lead Cavity DIP (J)
NS Package Number J16A

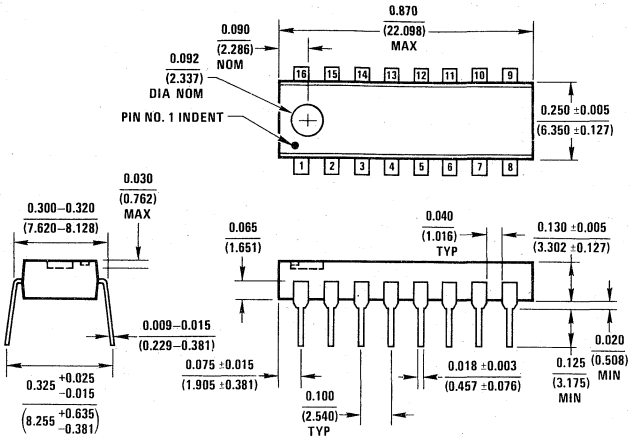


PIN	60	67
1	NC	S1
2	S1	D1
3	D1	NC
4	G1	G1
5	S2	S2
6	D2	D2
7	G2	NC
8	NC	G2

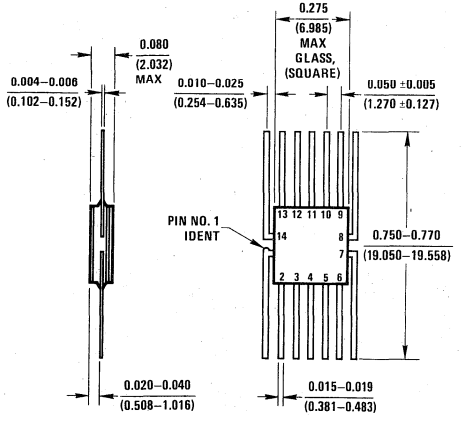
Package 20
8-Lead Molded Mini-DIP (60, 67) (N)
NS Package Number N08A



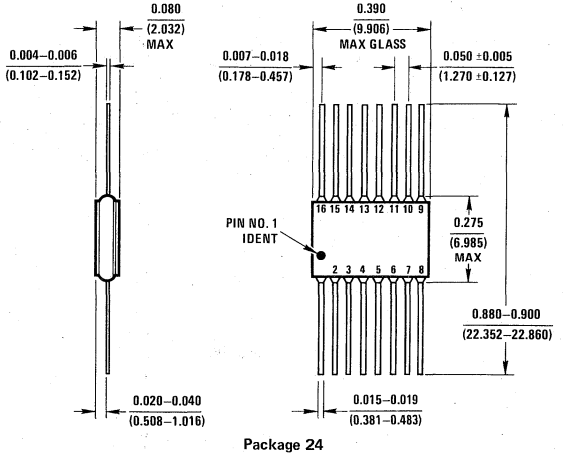
Package 21
14-Lead Molded DIP (N)
NS Package Number N14A



Package 22
16-Lead Molded DIP (N)
NS Package Number N16A



Package 23
14-Lead Flat Package (F)
NS Package Number F14A



Package 24
16-Lead Flat Package (F)
NS Package Number F16A

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